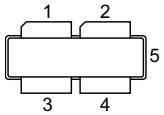
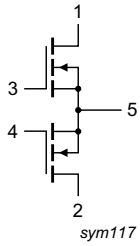
2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF8G10LS-300P	-	earless flanged balanced ceramic package; 4 leads	SOT539B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j\text{-}case)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 65 W	0.29	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C; values per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.2 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 20 V; I_D = 220 mA	1.5	1.9	2.3	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 1000 mA	-	2.0	-	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	2.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 20 V	-	38.1	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	240	nA
g_{fs}	forward transconductance	V_{DS} = 20 V; I_D = 11 A	-	15.0	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 7.7 A	-	0.086	-	Ω

Table 7. RF characteristics

Test signal: 2-carrier W-CDMA; PAR = 7.2 dB at 0.01 % probability on CCDF; 3GPP test model 1; 1 to 64 DPCH; f_1 = 760.5 MHz; f_2 = 765.5 MHz; f_3 = 795.5 MHz; f_4 = 800.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 2000 mA; T_{case} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 65 W	19.5	20.5	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 65 W	-	−12	−8	dB
η_D	drain efficiency	$P_{L(AV)}$ = 65 W	28	32	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 65 W	-	−35	−32	dBc

7. Test information

7.1 Ruggedness in class-AB operation

The BLF8G10LS-300P is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 2000 mA; P_L = 65 W (2-carrier W-CDMA); f = 758 MHz.

7.2 Impedance information

Table 8. Typical impedance

Measured load-pull data per section; I_{Dq} = 1000 mA; V_{DS} = 28 V

f (MHz)	Z_S [1] (Ω)	Z_L [1] (Ω)	$P_{L(3dB)}$ (W)
720	2.3 – j2.8	1.6 – j2.7	204.4
746	2.5 – j3.2	1.7 – j2.6	220.0
757	2.3 – j3.6	1.6 – j2.5	225.2
769	2.6 – j3.6	1.7 – j2.4	227.9
791	2.6 – j3.9	1.5 – j2.8	214.8
805	2.6 – j3.9	1.8 – j2.3	207.2
820	2.7 – j4.2	1.6 – j2.1	228.5
869	2.8 – j4.1	1.2 – j2.1	217.2
881	2.9 – j4.4	1.2 – j2.1	219.9
894	3.3 – j4.7	1.1 – j2.1	215.4
925	3.6 – j5.2	1.2 – j2.1	223.5
942	4.1– j 5.7	1.1 – j2.2	220.5
960	4.7 – j5.9	1.1 – j2.2	218.8

[1] Z_S and Z_L defined in Figure 1.

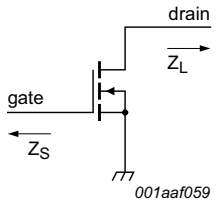
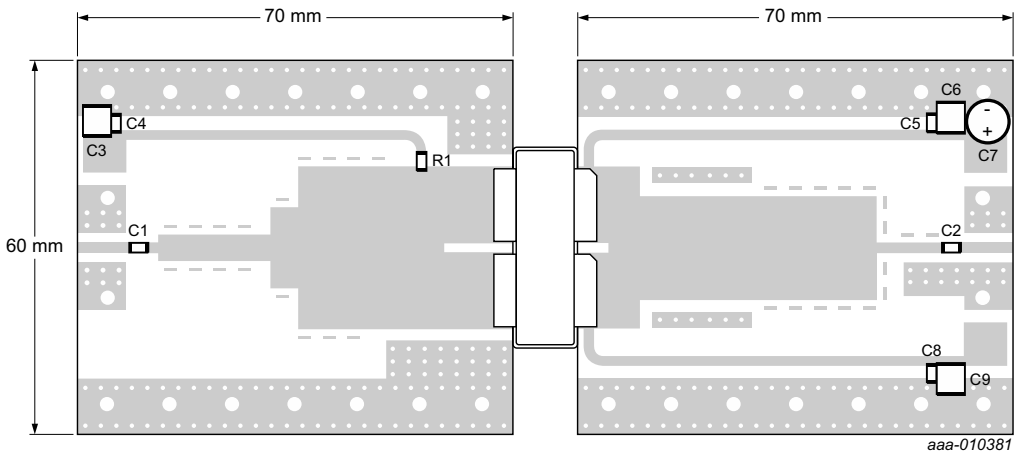


Fig 1. Definition of transistor impedance

7.3 Test circuit



Printed-Circuit Board (PCB): Rogers RO4350; ε_r = 3.66 F/m; thickness = 0.76 mm; thickness copper plating = 35 μm

See Table 9 for list of components.

Fig 2. Component layout

Table 9. List of components

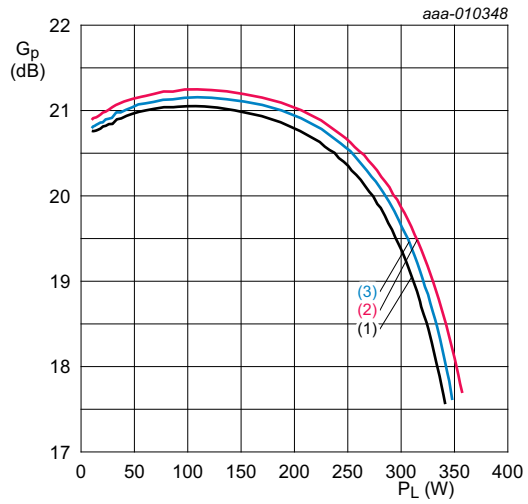
See Figure 2 for component layout.

Component	Description	Value	Remarks
C1, C2	multilayer ceramic chip capacitor	82 pF	ATC 800B
C3, C6, C9	multilayer ceramic chip capacitor	10 μF, 50 V	Murata
C4, C5, C8	multilayer ceramic chip capacitor	82 pF	ATC 100B
C7	electrolytic capacitor	470 μF, 63 V	
R1	chip resistor	4.7 Ω	SMD 1206

7.4 Graphical data

Following are typical RF measurements of the BLF8G10LS-300P in its class-AB test circuit.

7.4.1 CW pulsed



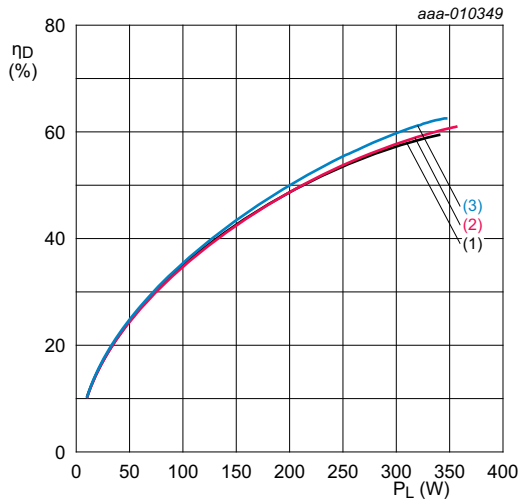
V_{DS} = 28 V; I_{Dq} = 2000 mA; t_p = 100 μs: δ = 10 %.

(1) f = 758 MHz

(2) f = 780.5 MHz

(3) f = 803 MHz

Fig 3. Power gain as a function of output power; typical values



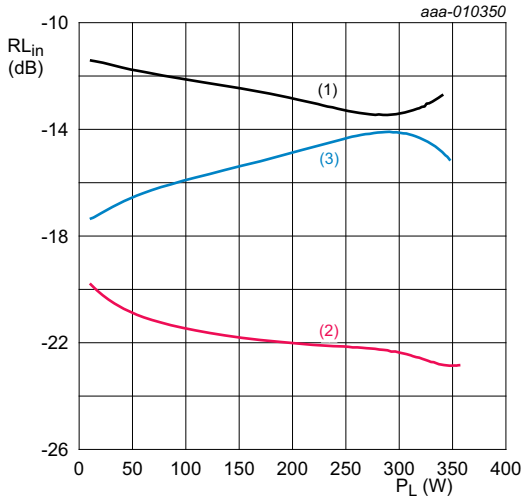
V_{DS} = 28 V; I_{Dq} = 2000 mA; t_p = 100 μs: δ = 10 %.

(1) f = 758 MHz

(2) f = 780.5 MHz

(3) f = 803 MHz

Fig 4. Drain efficiency as a function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 2000 mA; t_p = 100 μs: δ = 10 %.

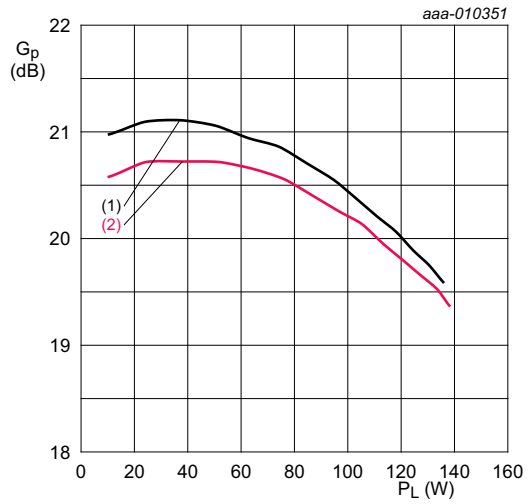
(1) f = 758 MHz

(2) f = 780.5 MHz

(3) f = 803 MHz

Fig 5. Input return loss as a function of output power; typical values

7.4.2 1-Carrier W-CDMA

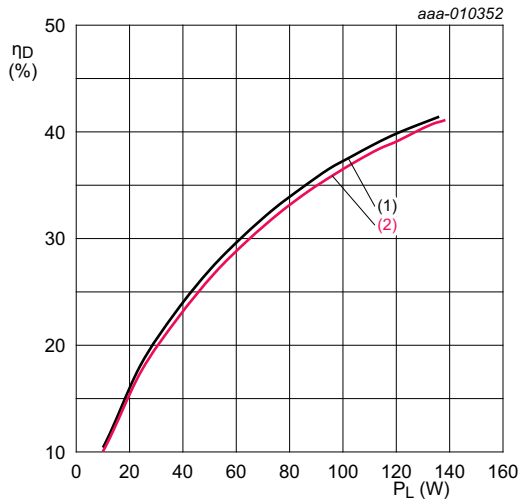


V_{DS} = 28 V; I_{Dq} = 2000 mA.

(1) f = 758 MHz

(2) f = 803 MHz

Fig 6. Power gain as a function of output power; typical values

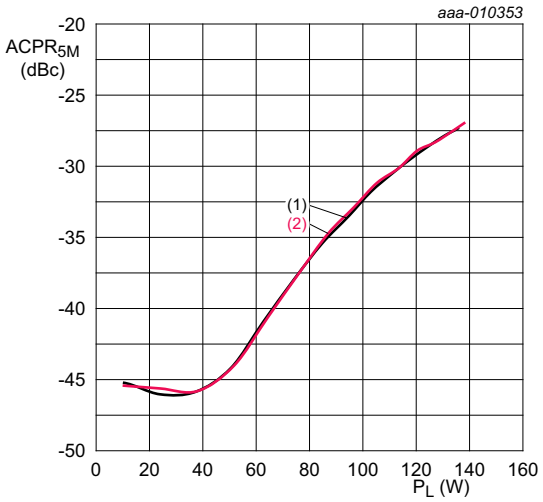


V_{DS} = 28 V; I_{Dq} = 2000 mA.

(1) f = 758 MHz

(2) f = 803 MHz

Fig 7. Drain efficiency as a function of output power; typical values



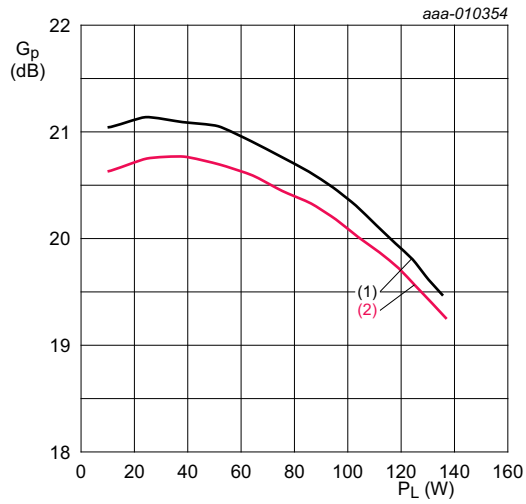
V_{DS} = 28 V; I_{Dq} = 2000 mA.

(1) f = 758 MHz

(2) f = 803 MHz

Fig 8. Adjacent channel power ratio (5 MHz) as a function of output power; typical values

7.4.3 2-Carrier W-CDMA

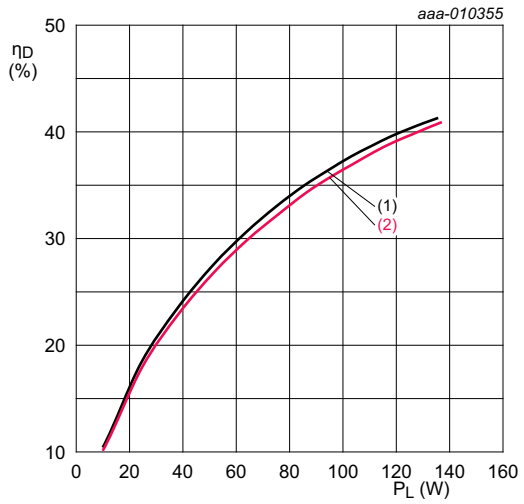


V_{DS} = 28 V; I_{Dq} = 2000 mA.

(1) f = 758 MHz

(2) f = 803 MHz

Fig 9. Power gain as a function of output power; typical values

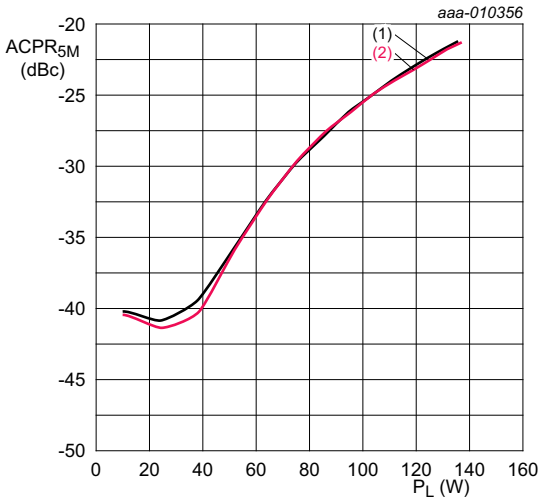


V_{DS} = 28 V; I_{Dq} = 2000 mA.

(1) f = 758 MHz

(2) f = 803 MHz

Fig 10. Drain efficiency as a function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 2000 mA.

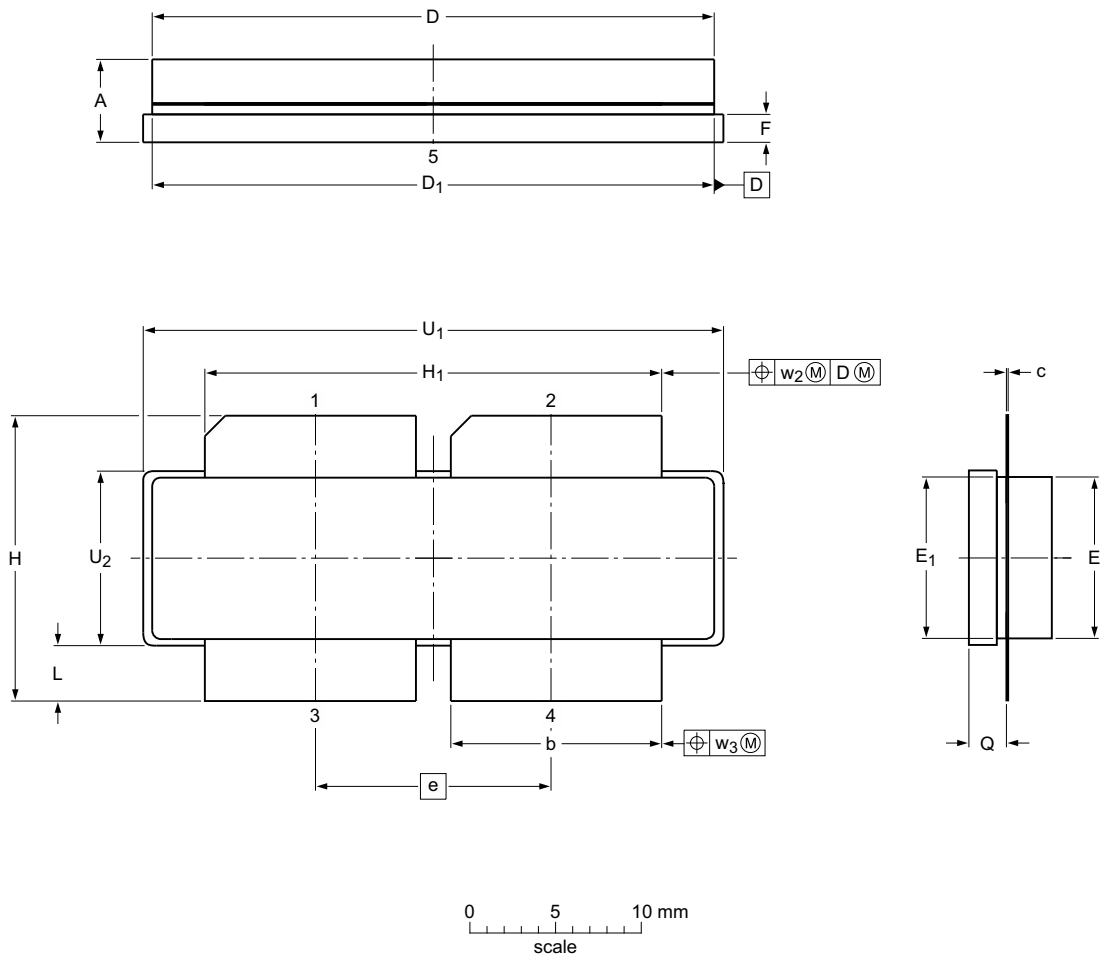
(1) f = 758 MHz

(2) f = 803 MHz

Fig 11. Adjacent channel power ratio (5 MHz) as a function of output power; typical values

8. Package outline

Earless flanged balanced ceramic package; 4 leads **SOT539B**



Dimensions

Unit[1]		A	b	c	D	D_1	E	E_1	e	F	H	H_1	L	Q	U_1	U_2	w_2	w_3
mm	max	4.7	11.81	0.18	31.55	31.52	9.5	9.53	13.72	1.75	17.12	25.53	3.48	2.26	32.39	10.29	0.25	0.25
	nom																	
	min	4.2	11.56	0.10	30.94	30.96	9.3	9.27		1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	max	0.185	0.465	0.007	1.242	1.241	0.374	0.375	0.54	0.069	0.674	1.005	0.137	0.089	1.275	0.405	0.01	0.01
	nom																	
	min	0.165	0.455	0.004	1.218	1.219	0.366	0.365		0.059	0.634	0.995	0.117	0.079	1.265	0.395		

Note
1. millimeter dimensions are derived from the original inch dimensions.

sot539b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT539B						~~12-05-02~~ 13-05-24

Fig 12. Package outline SOT539B

9. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF8G10LS-300P#3	20150901	Product data sheet	-	BLF8G10LS-300P v.2
Modifications:	• The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. • Legal texts have been adapted to the new company name where appropriate.			
BLF8G10LS-300P v.2	20131217	Product data sheet	-	BLF8G10LS-300P v.1
BLF8G10LS-300P v.1	20131118	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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Document identifier: BLF8G10LS-300P#3