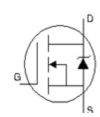
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	——	——	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.075	——	V/°C	Reference to 25°C, I_D = 5mA ②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	12.6	15.8	mΩ	V_{GS} = 10V, I_D = 25A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 50μA
gfs	Forward Trans conductance	41	——	——	S	V_{DS} = 10V, I_D = 25A
R_G	Internal Gate Resistance	——	0.79	——	Ω	
I_{DSS}	Drain-to-Source Leakage Current	——	——	20	μA	V_{DS} = 60V, V_{GS} = 0V
		——	——	250		V_{DS} = 48V,V_{GS} = 0V,T_J =125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge	——	22	30	nC	I_D = 25A
Q_{gs}	Gate-to-Source Charge	——	5.0	——		V_{DS} = 30V
Q_{gd}	Gate-to-Drain Charge	——	6.3	——		V_{GS} = 10V④
Q_{sync}	Total Gate Charge Sync. (Q_g - Q_{gd})	——	28.3	——		
$t_{d(on)}$	Turn-On Delay Time	——	6.3	——	ns	V_{DD} = 39V
t_r	Rise Time	——	40	——		I_D = 25A
$t_{d(off)}$	Turn-Off Delay Time	——	49	——		R_G= 20Ω
t_f	Fall Time	——	47	——		V_{GS} = 10V④
C_{iss}	Input Capacitance	——	1150	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	130	——		V_{DS} = 50V
C_{rss}	Reverse Transfer Capacitance	——	67	——		f = 1.0MHz, See Fig. 5
$C_{oss\ eff.(ER)}$	Effective Output Capacitance (Energy Related)	——	190	——		V_{GS} = 0V, V_{DS} = 0V to 48V⑥
$C_{oss\ eff.(TR)}$	Effective Output Capacitance (Time Related)	——	230	——		V_{GS} = 0V, V_{DS} = 0V to 48V⑤

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions	
I_S	Continuous Source Current (Body Diode)	——	——	43	A	MOSFET symbol showing the integral reverse p-n junction diode. 	
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	170			
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C,I_S = 25A,V_{GS} = 0V ④	
t_{rr}	Reverse Recovery Time	——	22	33	ns	T_J = 25°C	V_{DD} = 51V, I_F = 25A di/dt = 100A/μs④
		——	26	39		T_J = 125°C	
Q_{rr}	Reverse Recovery Charge	——	17	26	nC	T_J = 25°C	
		——	24	36		T_J = 125°C	
I_{RRM}	Reverse Recovery Current	——	1.4	——	A	T_J = 25°C	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)					

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.
② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.23mH, R_G = 25Ω, I_{AS} = 25A, V_{GS} =10V. Part not recommended for use above this value.
③ I_{SD} ≤ 25A, di/dt ≤ 1580A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C.
④ Pulse width ≤ 400μs; duty cycle ≤ 2%.
⑤ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
⑥ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
⑧ R_θ is measured at T_J approximately 90°C.

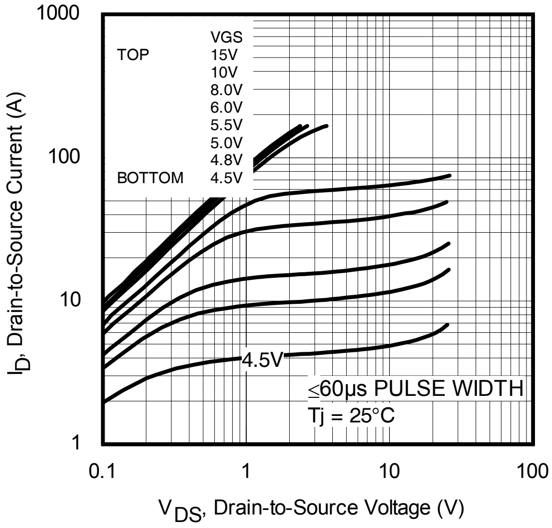


Fig. 1 Typical Output Characteristics

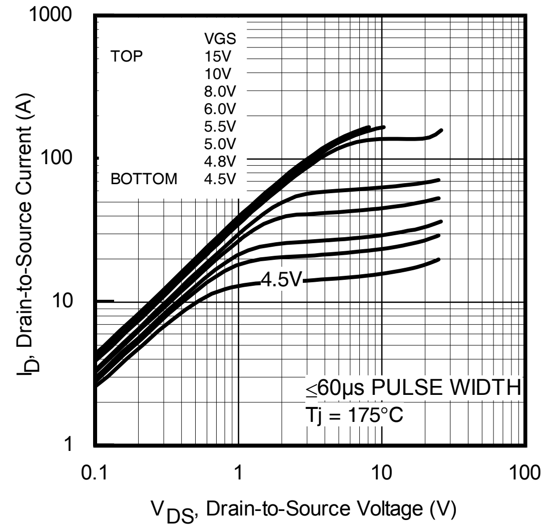


Fig. 2 Typical Output Characteristics

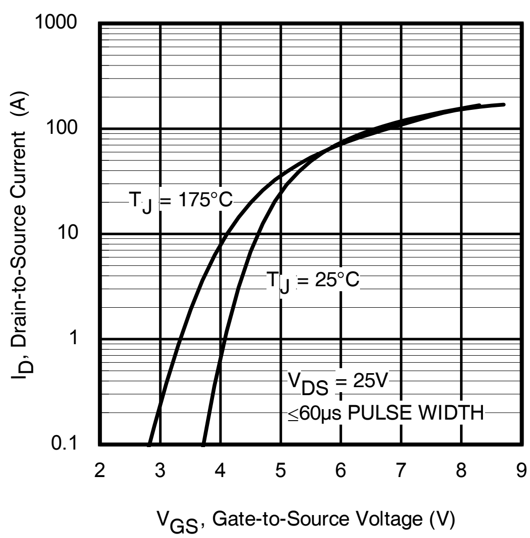


Fig. 3 Typical Transfer Characteristics

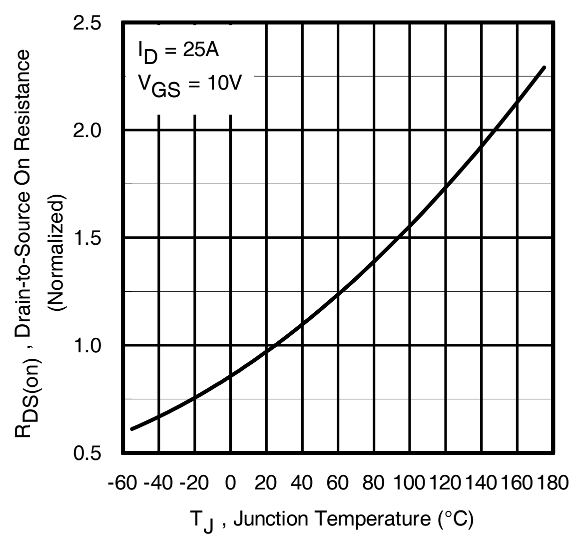


Fig. 4 Normalized On-Resistance vs. Temperature

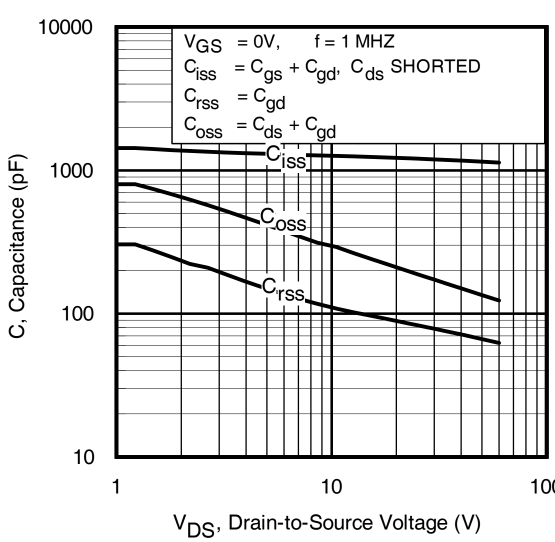


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

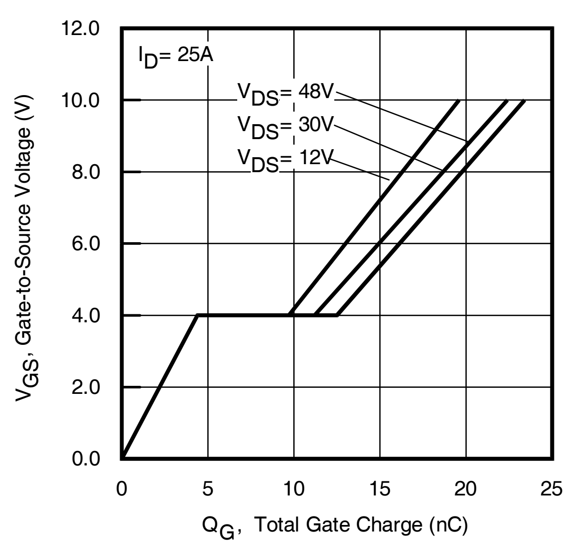


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

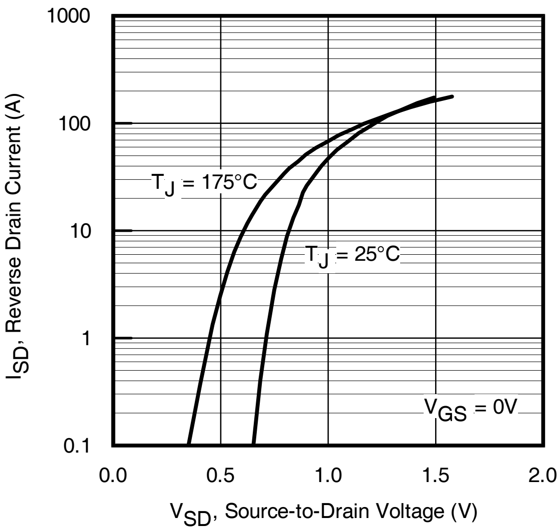


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

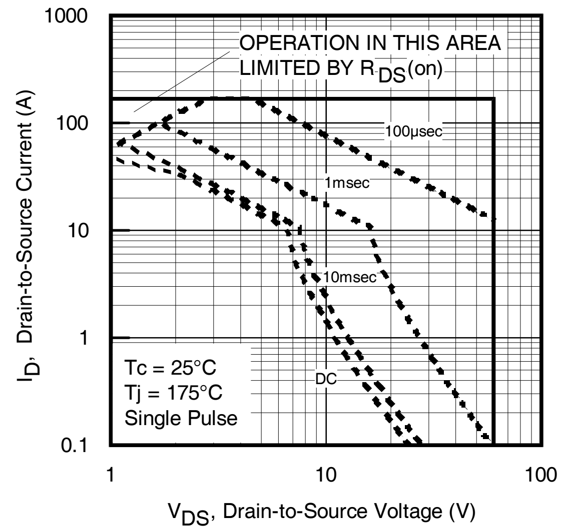
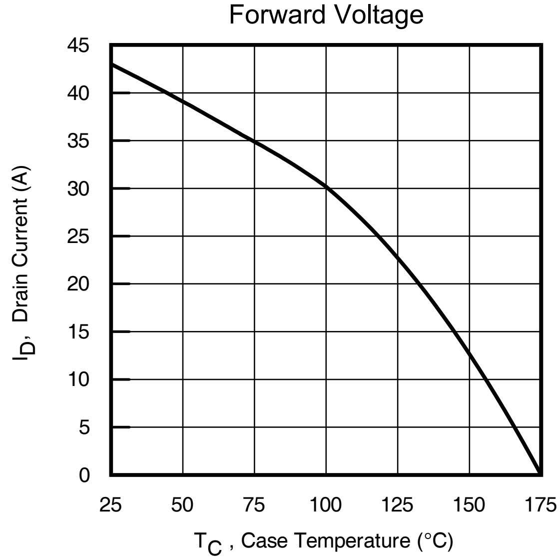


Fig 8. Maximum Safe Operating Area



Fg 9. Maximum Drain Current vs. Case Temperature

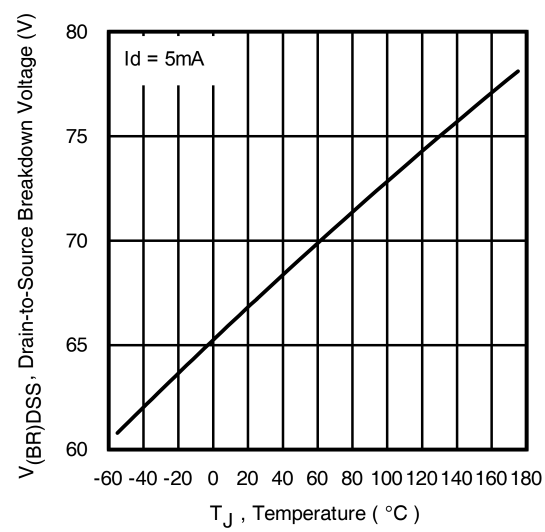


Fig 10. Drain-to-Source Breakdown Voltage

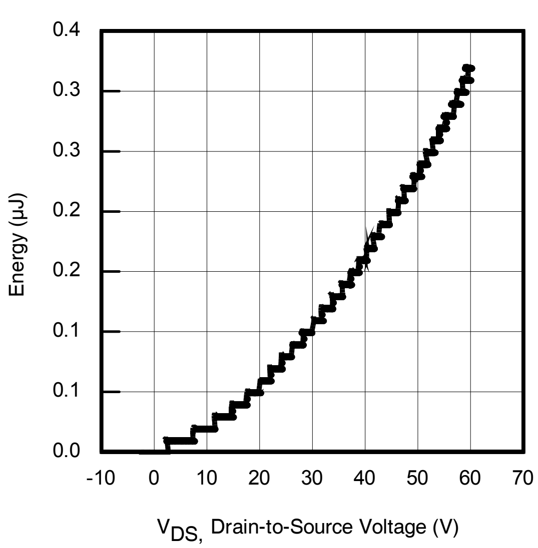


Fig 11. Typical Coss Stored Energy

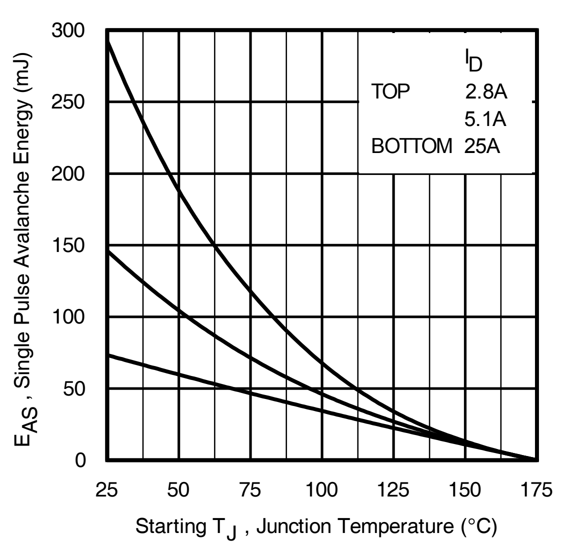


Fig 12. Maximum Avalanche Energy vs. Drain Current

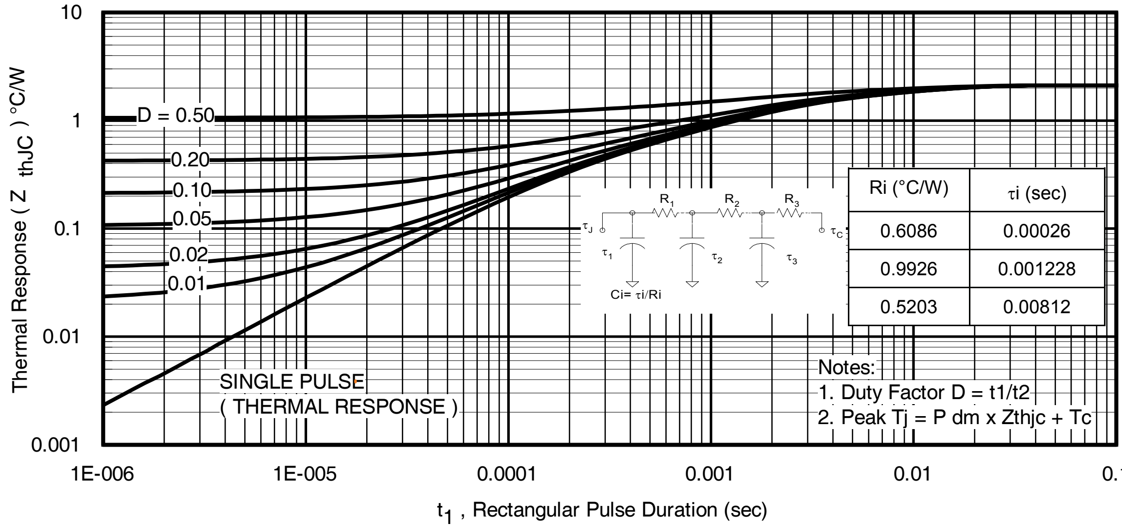


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

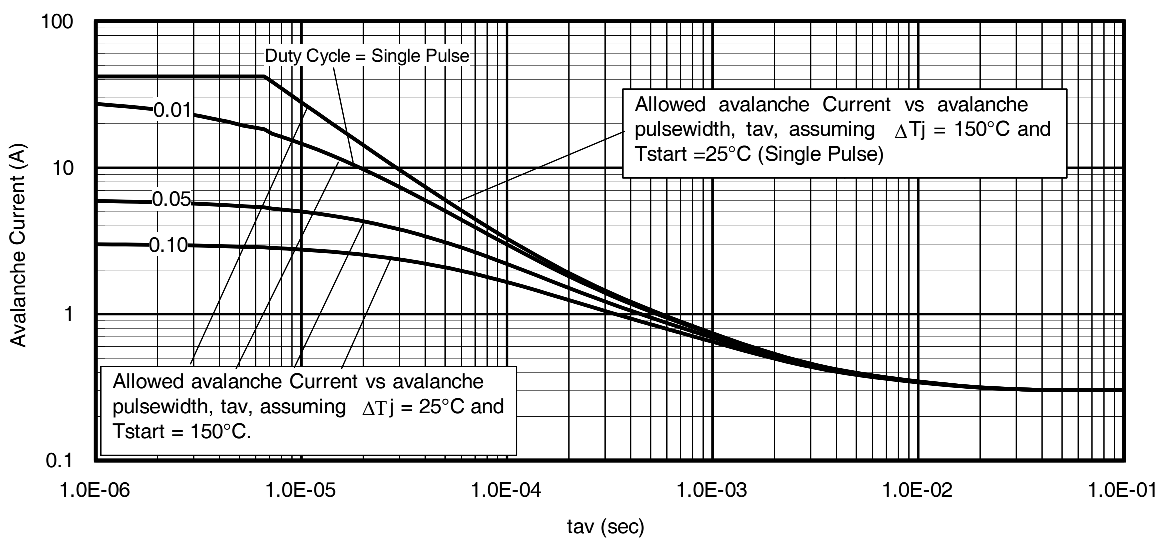


Fig 14. Avalanche Current vs. Pulse width

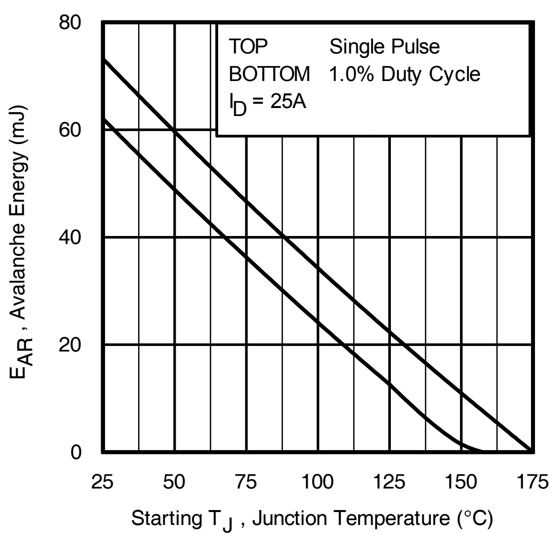


Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.infineon.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 22a, 22b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 13, 14).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

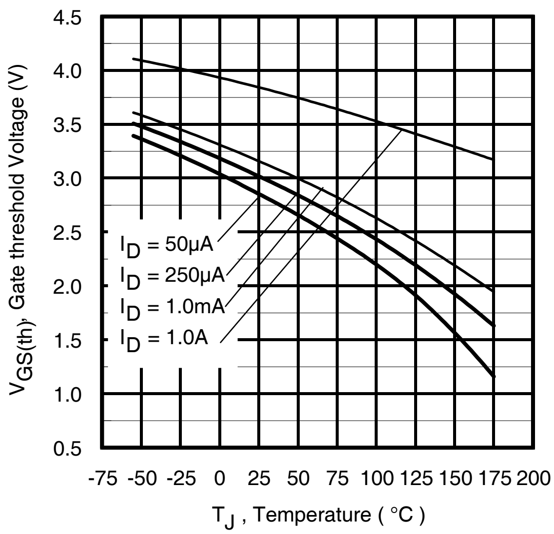


Fig 16. Threshold Voltage vs. Temperature

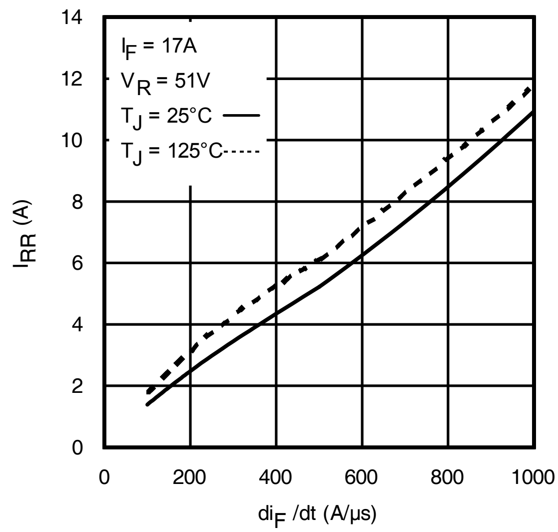


Fig. 17 - Typical Recovery Current vs. dif/dt

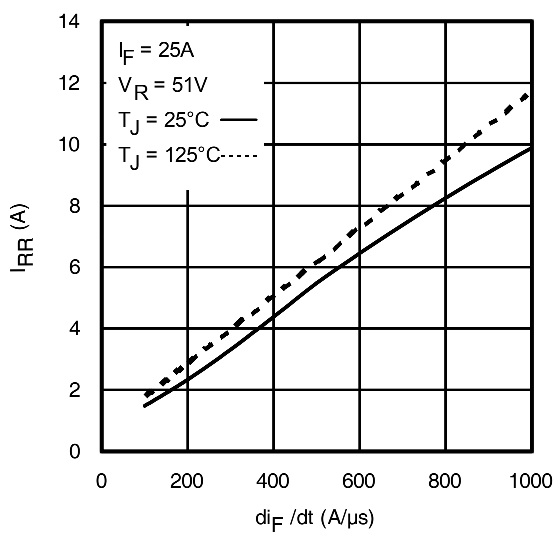


Fig. 18 - Typical Recovery Current vs. dif/dt

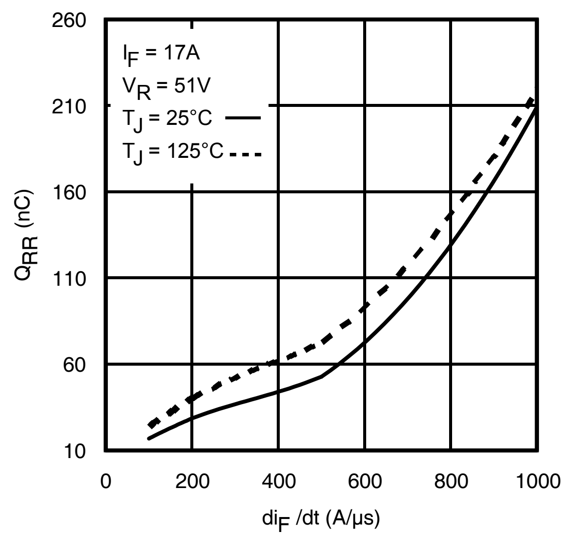


Fig. 19 - Typical Stored Charge vs. dif/dt

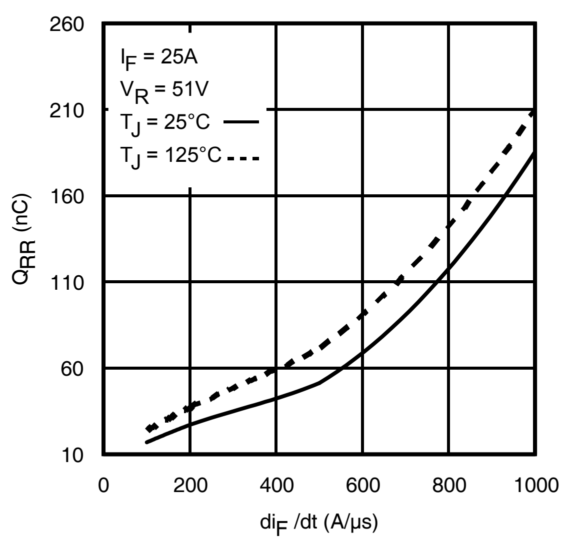


Fig. 20 - Typical Stored Charge vs. dif/dt

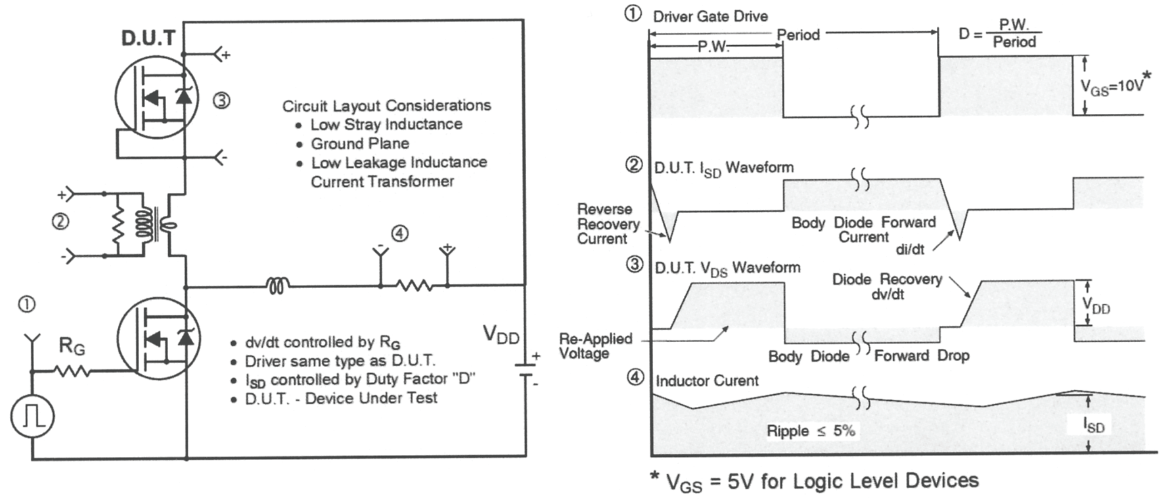


Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

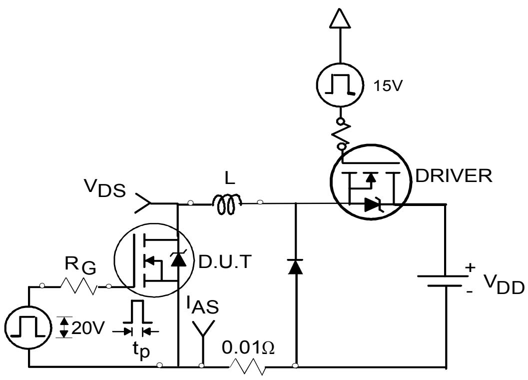


Fig 22a. Unclamped Inductive Test Circuit

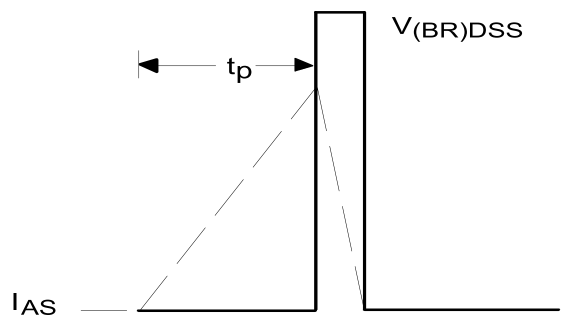


Fig 22b. Unclamped Inductive Waveforms

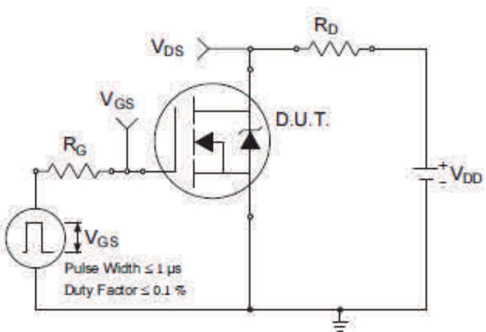


Fig 23a. Switching Time Test Circuit

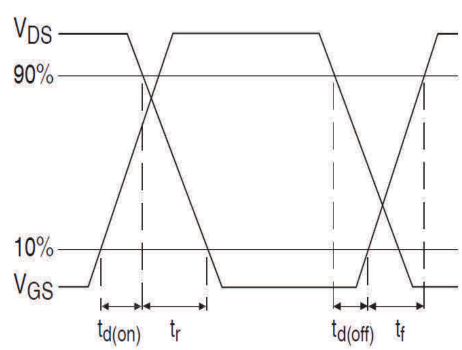


Fig 23b. Switching Time Waveforms

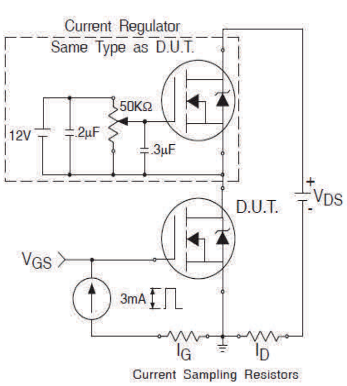


Fig 24a. Gate Charge Test Circuit

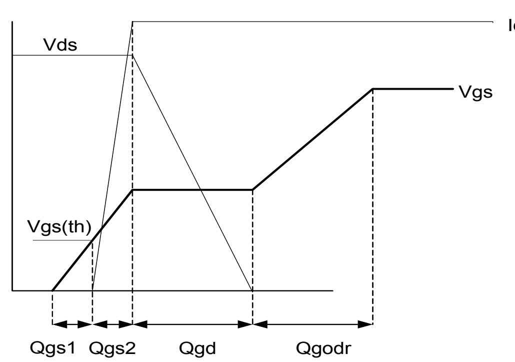
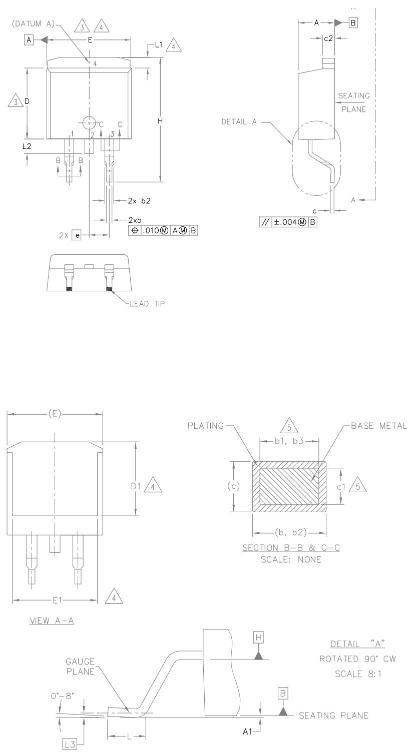


Fig 24b. Gate Charge Waveform

D^2-Pak (TO-263AB) Package Outline (Dimensions are shown in millimeters (inches))



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1, b3 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	–	.270	–	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	–	.245	–	4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	–	1.68	–	.066	4
L2	–	1.78	–	.070	
L3	0.25 BSC		.010 BSC		

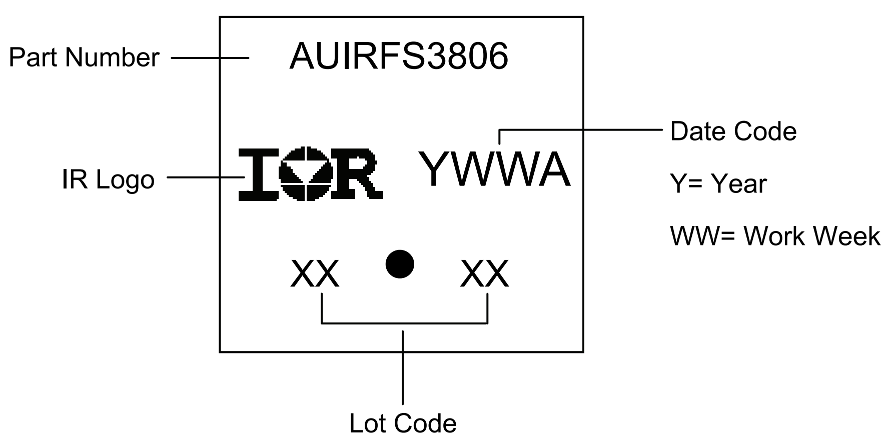
LEAD ASSIGNMENTS

DIODES
1.– ANODE (TWO DIE) / OPEN (ONE DIE)
2, 4.– CATHODE
3.– ANODE

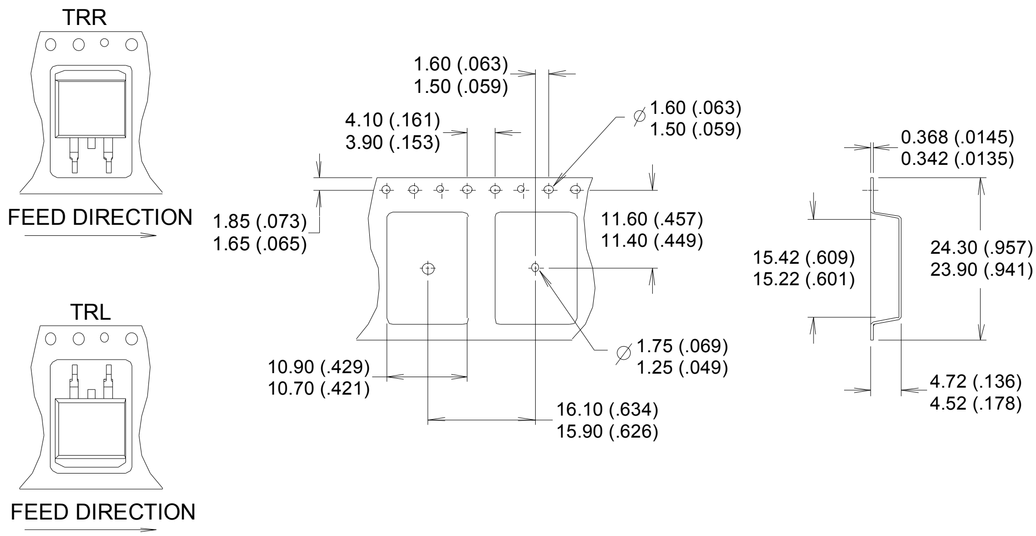
HEXFET
1.– GATE
2, 4.– DRAIN
3.– SOURCE

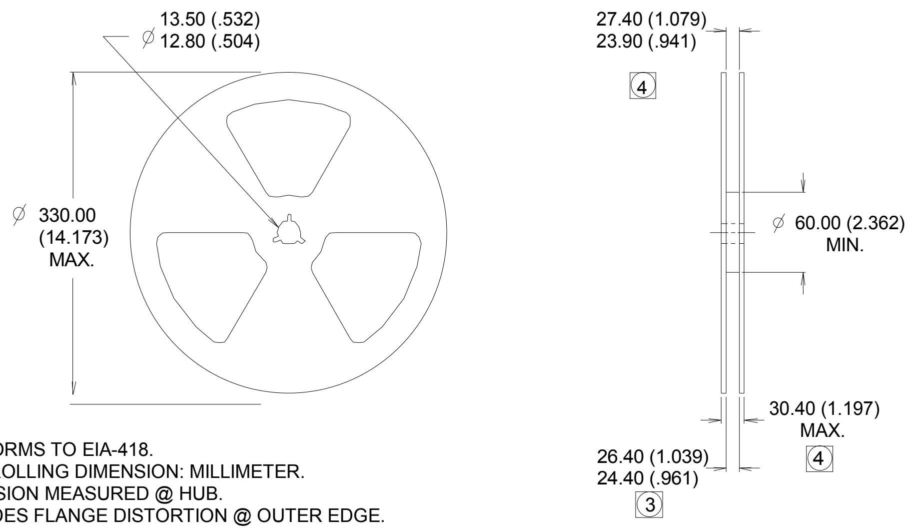
IGBTs, CoPACK
1.– GATE
2, 4.– COLLECTOR
3.– EMITTER

D^2-Pak (TO-263AB) Part Marking Information



D²-Pak (TO-263AB) Tape & Reel Information (Dimensions are shown in millimeters (inches))





NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Qualification Information

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		D^2-Pak	MSL1
ESD	Machine Model	Class M2 (+/- 200V)† AEC-Q101-002	
	Human Body Model	Class H1B (+/- 700V)† AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 2000V)† AEC-Q101-005	
RoHS Compliant		Yes	

† Highest passing voltage.

Revision History

Date	Comments
12/2/2015	• Updated datasheet with corporate template • Corrected ordering table on page 1. • Updated typo on the fig.19 and fig.20, unit of y-axis from "A" to "nC" on page 7. • Corrected typo Coss eff test condition from “60V” to “48V” on page 2.
10/12/2017	• Corrected typo error on part marking on page 8.

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