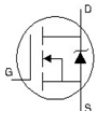
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.036	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	3.5	4.0	mΩ	V_{GS} = 10V, I_D = 95A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
gfs	Forward Trans conductance	106	—	—	S	V_{DS} = 25V, I_D = 60A⑦
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	µA	V_{DS} = 40 V, V_{GS} = 0V
		—	—	250		V_{DS} = 32V,V_{GS} = 0V,T_J =125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V_{GS} = -20V

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Q_g	Total Gate Charge	—	160	200	nC	I_D = 95A
Q_{gs}	Gate-to-Source Charge	—	35	—		V_{DS} = 32V
Q_{gd}	Gate-to-Drain Charge	—	42	60		V_{GS} = 10V④⑦
$t_{d(on)}$	Turn-On Delay Time	—	17	—	ns	V_{DD} = 20V
t_r	Rise Time	—	140	—		I_D = 95A
$t_{d(off)}$	Turn-Off Delay Time	—	72	—		R_G= 2.5Ω
t_f	Fall Time	—	26	—		R_D= 0.21Ω ④⑦
L_S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C_{iss}	Input Capacitance	—	7360	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	1680	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	240	—		f = 1.0MHz, See Fig. 5 ⑦
C_{oss}	Output Capacitance	—	6630	—		V_{GS} = 0V, V_{DS} = 1.0V f = 1.0MHz
C_{oss}	Output Capacitance	—	1490	—		V_{GS} = 0V, V_{DS} = 32V f = 1.0MHz
$C_{oss\ eff.}$	Effective Output Capacitance	—	1540	—		V_{GS} = 0V, V_{DS} = 0V to 32V

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	162⑥	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	650		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C,I_S = 95A,V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	71	110	ns	T_J = 25°C ,I_F = 95A
Q_{rr}	Reverse Recovery Charge	—	180	270	nC	di/dt = 100A/µs ④⑦
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 0.12mH, R_G = 25Ω, I_{AS} = 95A, V_{GS} =10V. (See fig. 12)

③ I_{SD} ≤ 95A, di/dt ≤ 150A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C.

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

⑦ Use IRF1404 data and test conditions.

⑧ This is applied to D^2Pak When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994

⑨ R_θ is measured at T_J approximately 90°C.

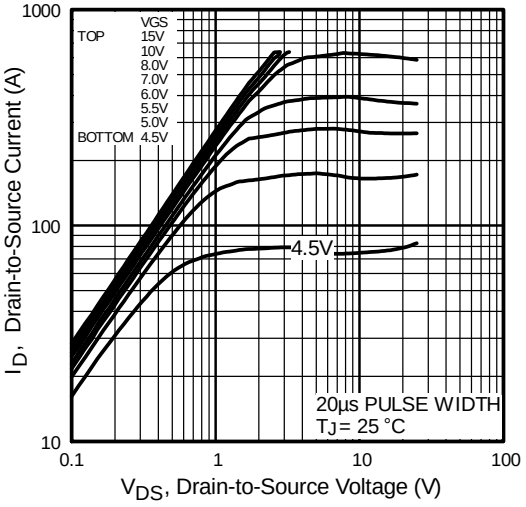


Fig. 1 Typical Output Characteristics

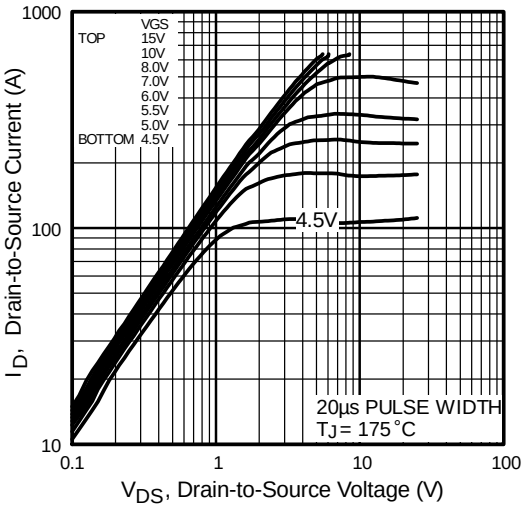


Fig. 2 Typical Output Characteristics

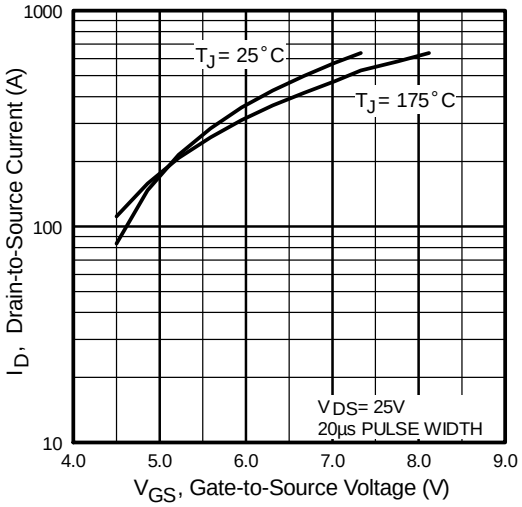


Fig. 3 Typical Transfer Characteristics

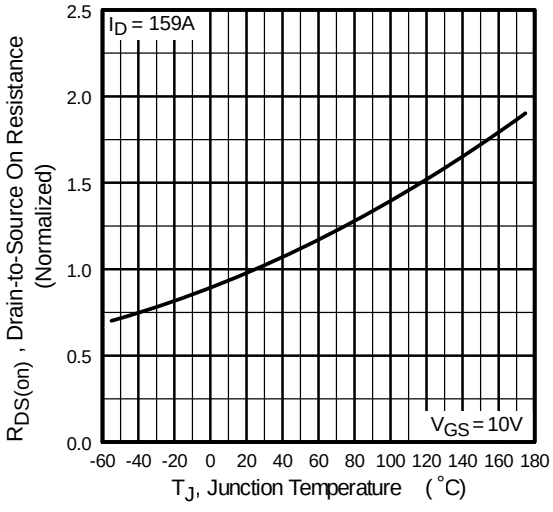


Fig. 4 Normalized On-Resistance Vs. Temperature

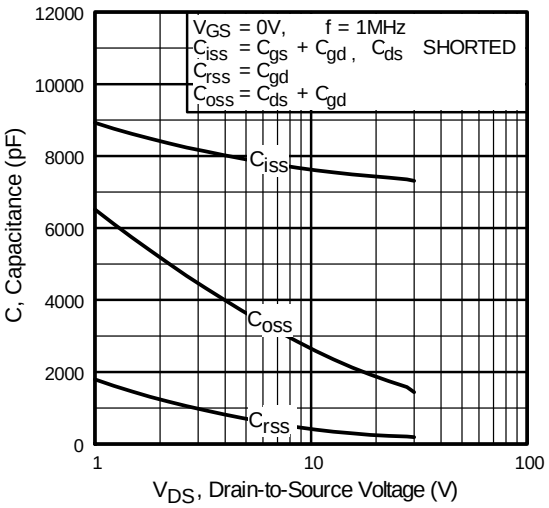


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

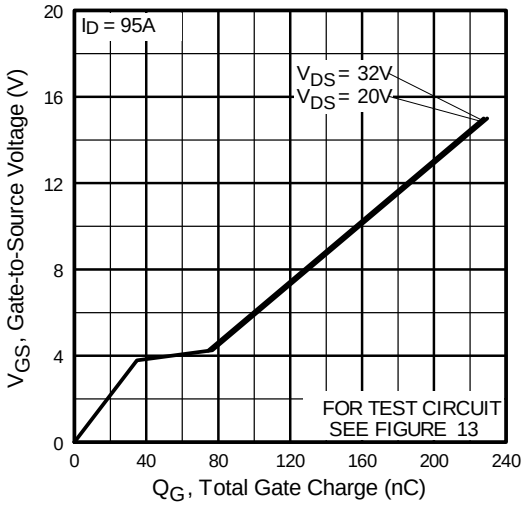


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

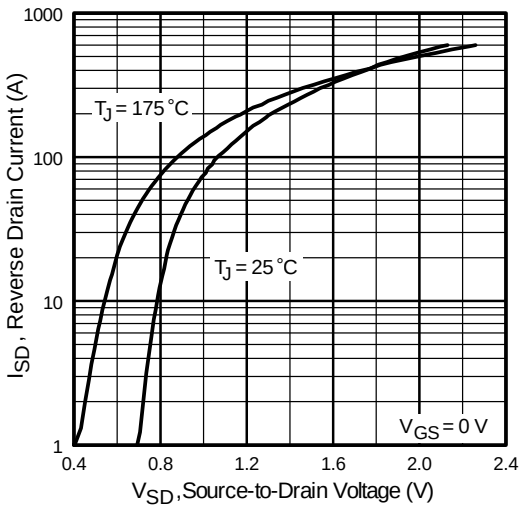


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

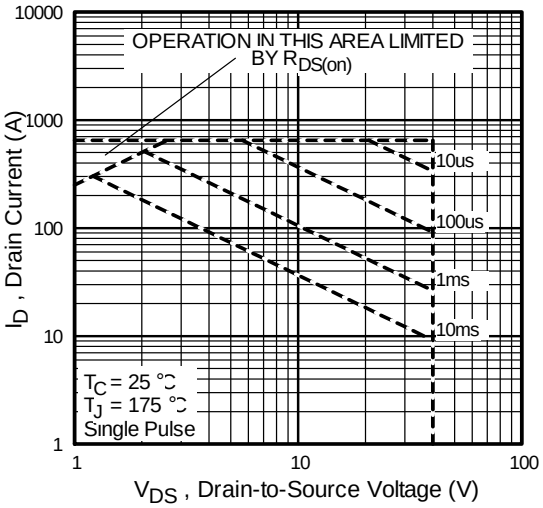


Fig 8. Maximum Safe Operating Area

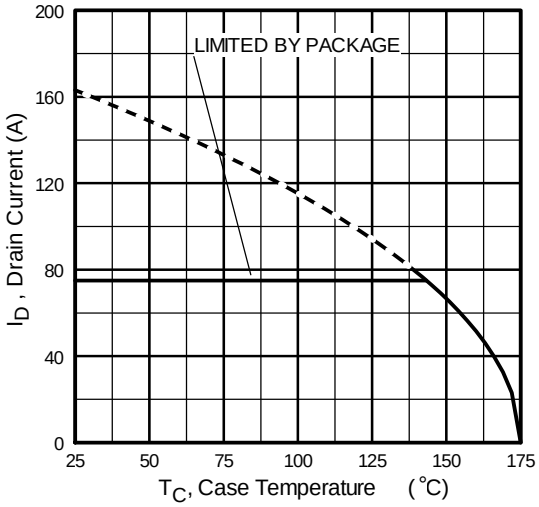


Fig 9. Maximum Drain Current vs. Case Temperature

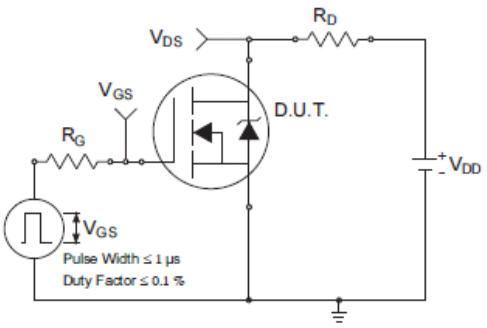


Fig 10a. Switching Time Test Circuit

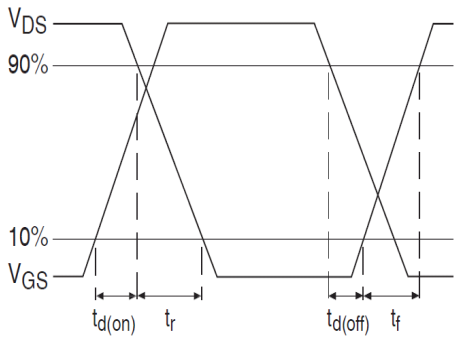


Fig 10b. Switching Time Waveforms

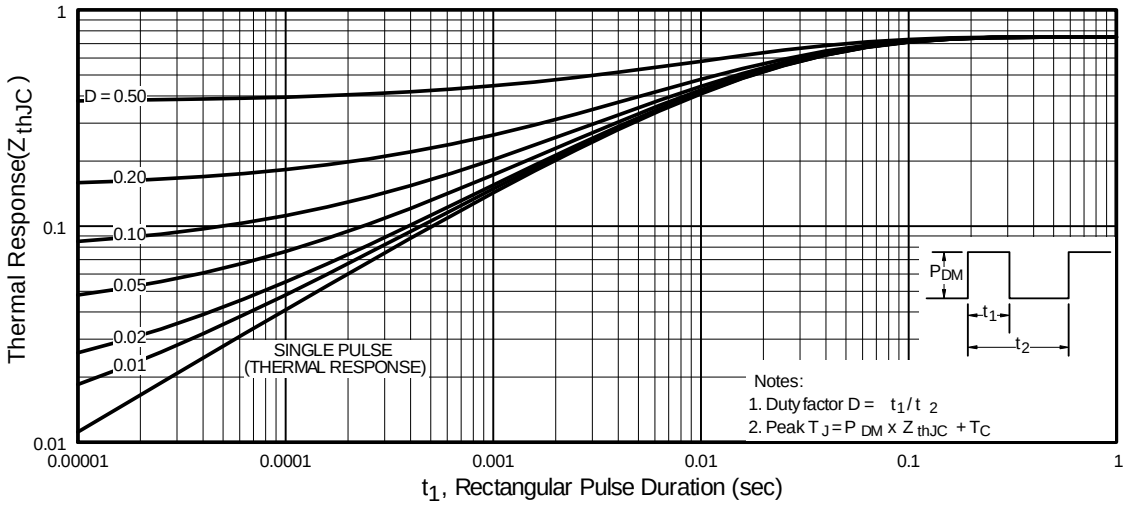


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

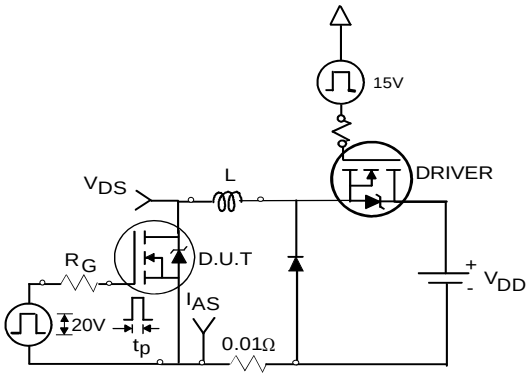


Fig 12a. Unclamped Inductive Test Circuit

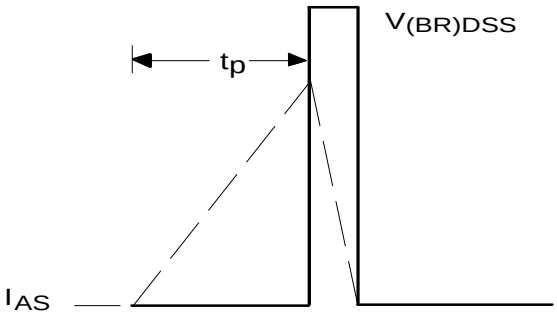


Fig 12b. Unclamped Inductive Waveforms

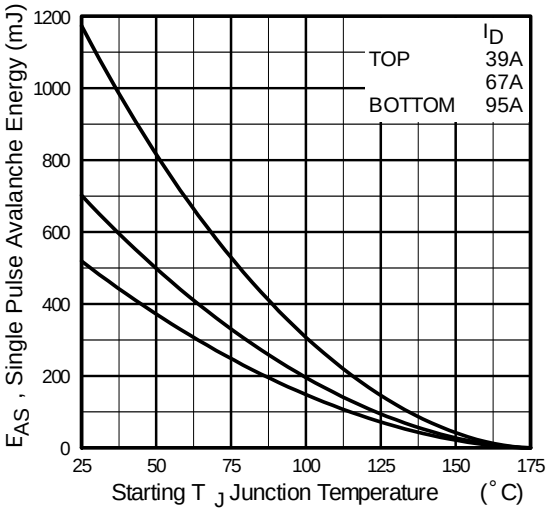


Fig 12c. Maximum Avalanche Energy vs. Drain Current

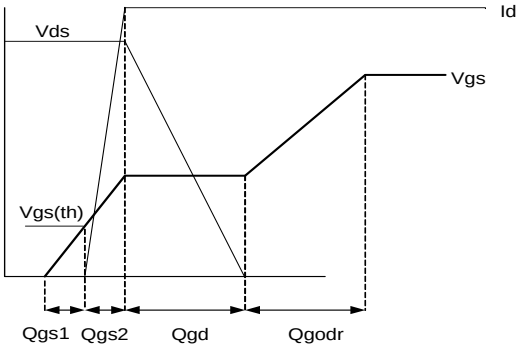


Fig 13a. Gate Charge Waveform

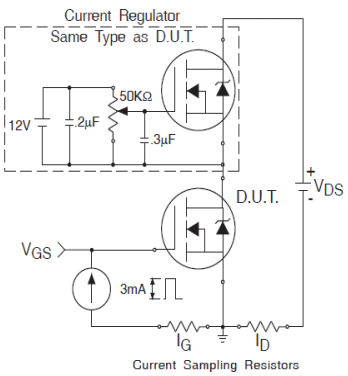


Fig 13b. Gate Charge Test Circuit

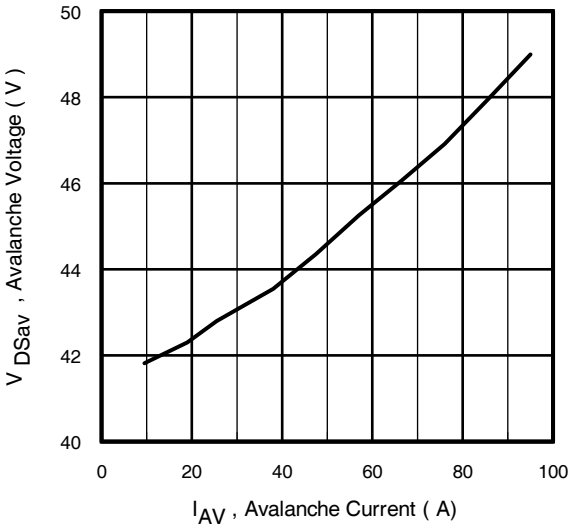


Fig 12d. Typical Drain-to-Source Voltage Vs. Avalanche Current

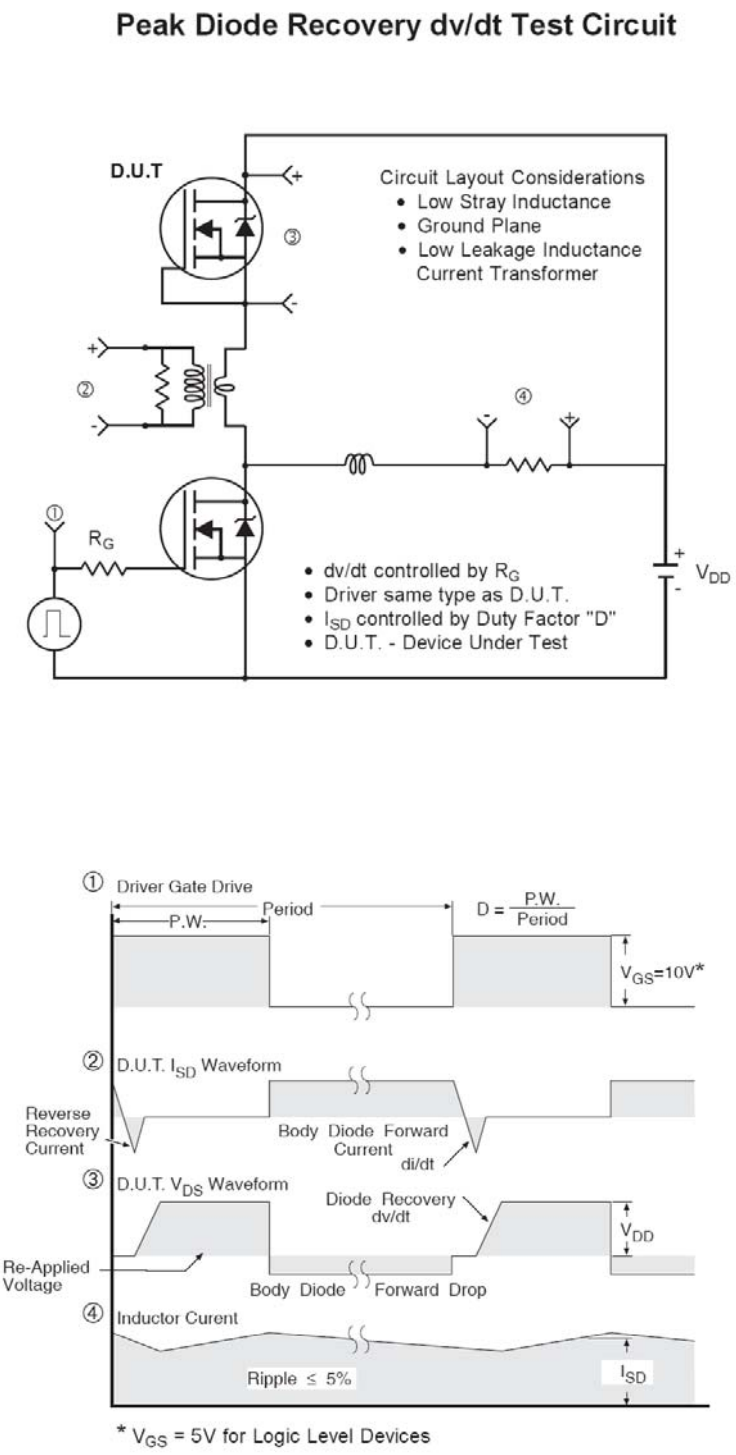
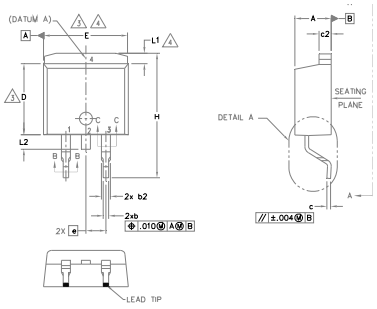


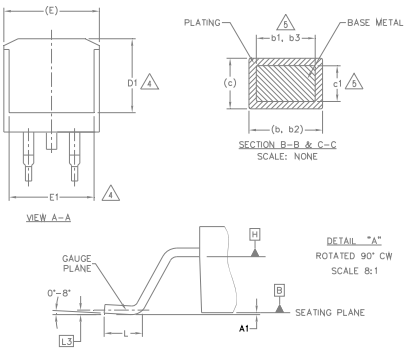
Fig 14. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

D²Pak (TO-263AB) Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1, b3 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	–	.270	–	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	–	.245	–	4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	–	1.68	–	.066	4
L2	–	1.78	–	.070	
L3	0.25 BSC		.010 BSC		

LEAD ASSIGNMENTS

DIODES

1.– ANODE (TWO DIE) / OPEN (ONE DIE)
2, 4.– CATHODE
3.– ANODE

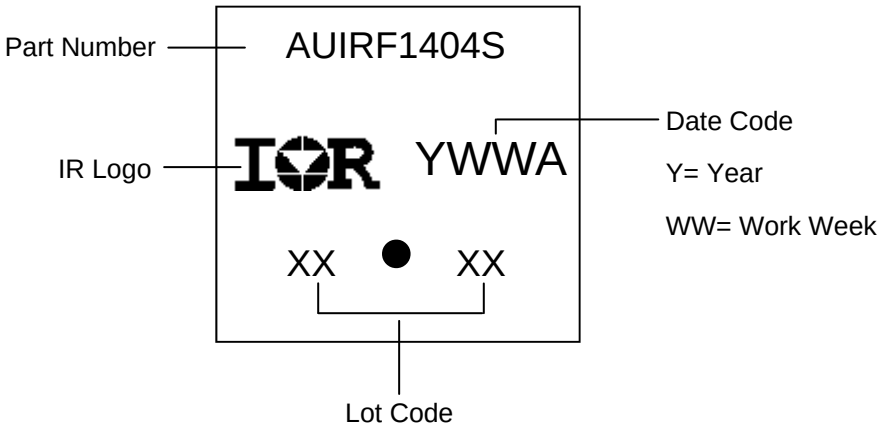
HEXFET

1.– GATE
2, 4.– DRAIN
3.– SOURCE

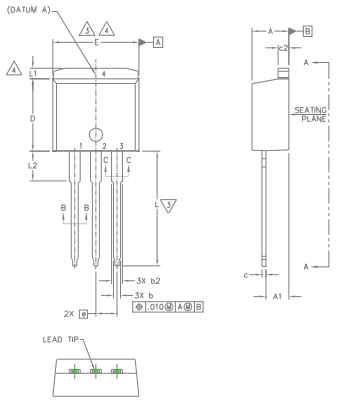
IGBTs, CoPACK

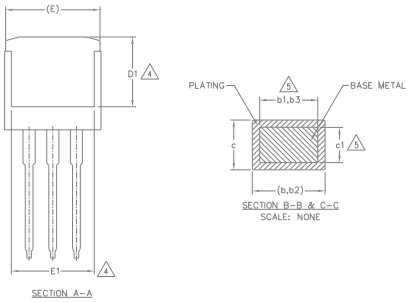
1.– GATE
2, 4.– COLLECTOR
3.– EMITTER

D²Pak (TO-263AB) Part Marking Information



TO-262 Package Outline (Dimensions are shown in millimeters (inches)





NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. – OUTLINE CONFORM TO JEDEC TO–262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

LEAD ASSIGNMENTS

IGBTs, CoPACK

1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR

HEXFET

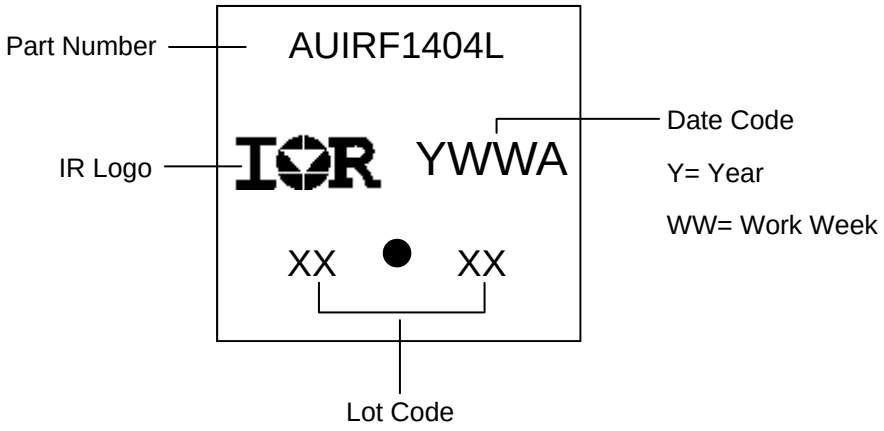
1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

DIODES

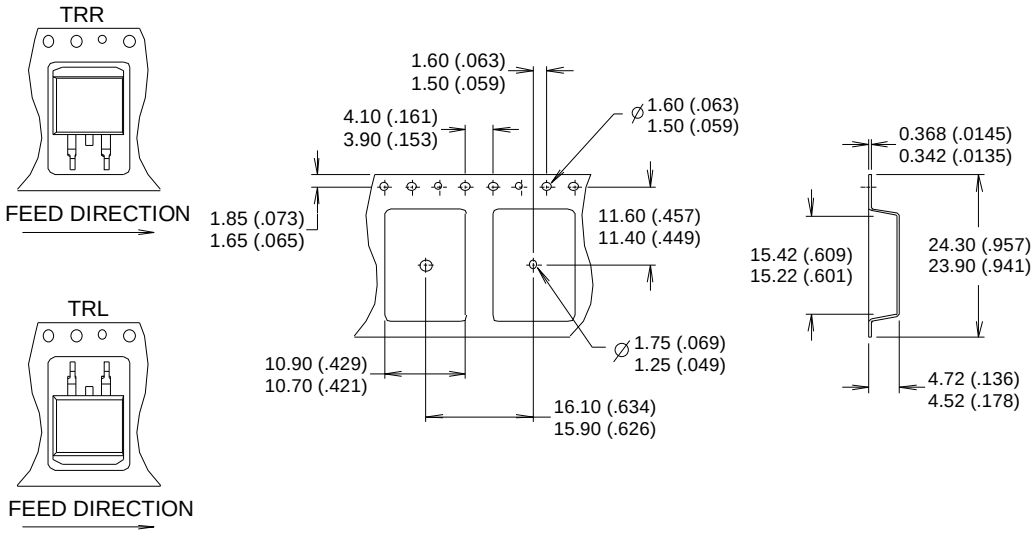
1.– ANODE (TWO DIE) / OPEN (ONE DIE)
2, 4.– CATHODE
3.– ANODE

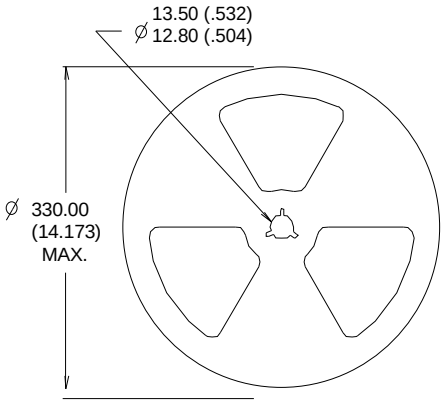
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	–	.270	–	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	–	.245		4
e	2.54 BSC		.100 BSC		
L	13.46	14.10	.530	.555	
L1	–	1.65	–	.065	4
L2	3.56	3.71	.140	.146	

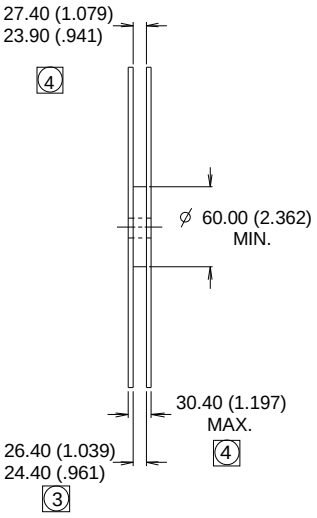
TO-262 Part Marking Information



D²Pak (TO-263AB) Tape & Reel Information (Dimensions are shown in millimeters (inches))







NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Qualification Information

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		TO-262 D^2-Pak	MSL1
ESD	Machine Model	Class M4 (+/- 425V) † AEC-Q101-002	
	Human Body Model	Class H2 (+/- 4000V)† AEC-Q101-001	
	Charged Device Model	Class C5 (+/-1125V)† AEC-Q101-005	
RoHS Compliant		Yes	

† Highest passing voltage.

Revision History

Date	Comments
11/11/2015	• Updated datasheet with corporate template • Corrected ordering table on page 1.

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