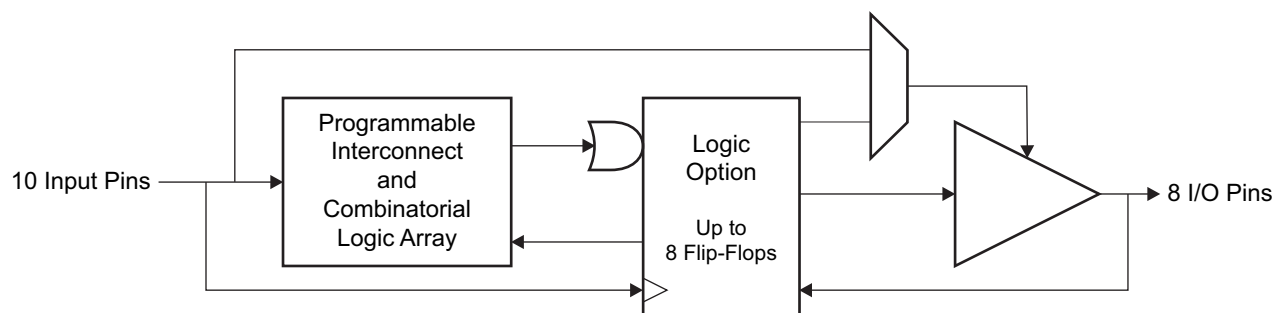




## 2. Block Diagram

Figure 2-1. Block Diagram



## 3. Electrical Characteristics

### 3.1 Absolute Maximum Ratings\*

|                                                                              |                                |
|------------------------------------------------------------------------------|--------------------------------|
| Temperature Under Bias . . . . .                                             | -55°C to +125°C                |
| Storage Temperature . . . . .                                                | -65°C to +150°C                |
| Voltage on Any Pin with<br>Respect to Ground . . . . .                       | -2.0V to +7.0V <sup>(1)</sup>  |
| Voltage on Input Pins with Respect to<br>Ground During Programming . . . . . | -2.0V to +14.0V <sup>(1)</sup> |
| Programming Voltage with<br>Respect to Ground . . . . .                      | -2.0V to +14.0V <sup>(1)</sup> |

\*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is  $V_{CC} + 0.75V$  DC, which may overshoot to 7.0V for pulses of less than 20ns.

### 3.2 Pin Capacitance

Table 3-1. Pin Capacitance (f = 1MHz, T = 25°C<sup>(1)</sup>)

|           | Typ | Max | Units | Conditions     |
|-----------|-----|-----|-------|----------------|
| $C_{IN}$  | 5   | 8   | pF    | $V_{IN} = 0V$  |
| $C_{OUT}$ | 6   | 8   | pF    | $V_{OUT} = 0V$ |

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

### 3.3 DC and AC Operating Conditions

Table 3-2. DC and AC Operating Conditions

|                                 | Industrial     |
|---------------------------------|----------------|
| Operating Temperature (Ambient) | -40°C to +85°C |
| $V_{CC}$ Power Supply           | 5.0V ± 10%     |

## 3.4 DC Characteristics

Table 3-3. DC Characteristics

| Symbol         | Parameter                         | Condition                                                     | Min                       | Typ | Max             | Units         |
|----------------|-----------------------------------|---------------------------------------------------------------|---------------------------|-----|-----------------|---------------|
| $I_{IL}$       | Input or I/O Low Leakage Current  | $0 \leq V_{IN} \leq V_{IL}(\text{Max})$                       |                           | -35 | -100            | $\mu\text{A}$ |
| $I_{IH}$       | Input or I/O High Leakage Current | $3.5 \leq V_{IN} \leq V_{CC}$                                 |                           |     | 10              | $\mu\text{A}$ |
| $I_{CC}$       | Power Supply Current, Standby     | $V_{CC} = \text{Max}$<br>$V_{IN} = \text{Max}$ , Outputs Open | B-10                      | 55  | 95              | mA            |
|                |                                   |                                                               | B-15                      | 50  | 80              |               |
|                |                                   |                                                               | BQL-15                    | 5   | 15              |               |
| $I_{CC2}$      | Clocked Power Supply Current      | $V_{CC} = \text{Max}$ , Outputs Open<br>$f = 15\text{MHz}$    | B-10                      | 60  | 100             | mA            |
|                |                                   |                                                               | B-15                      | 55  | 95              |               |
|                |                                   |                                                               | BQL-15                    | 20  | 40              |               |
| $I_{OS}^{(1)}$ | Output Short Circuit Current      | $V_{OUT} = 0.5\text{ V}$                                      |                           |     | -130            | mA            |
| $V_{IL}$       | Input Low Voltage                 |                                                               | -0.5                      |     | 0.8             | V             |
| $V_{IH}$       | Input High Voltage                |                                                               | 2.0                       |     | $V_{CC} + 0.75$ | V             |
| $V_{OL}$       | Output High Voltage               | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$V_{CC} = \text{Min}$        | $I_{OL} = 24\text{mA}$    |     | 0.5             | V             |
| $V_{OH}$       | Output High Voltage               | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$V_{CC} = \text{Min}$        | $I_{OH} = -4.0\text{ mA}$ | 2.4 |                 | V             |

Note: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30s.

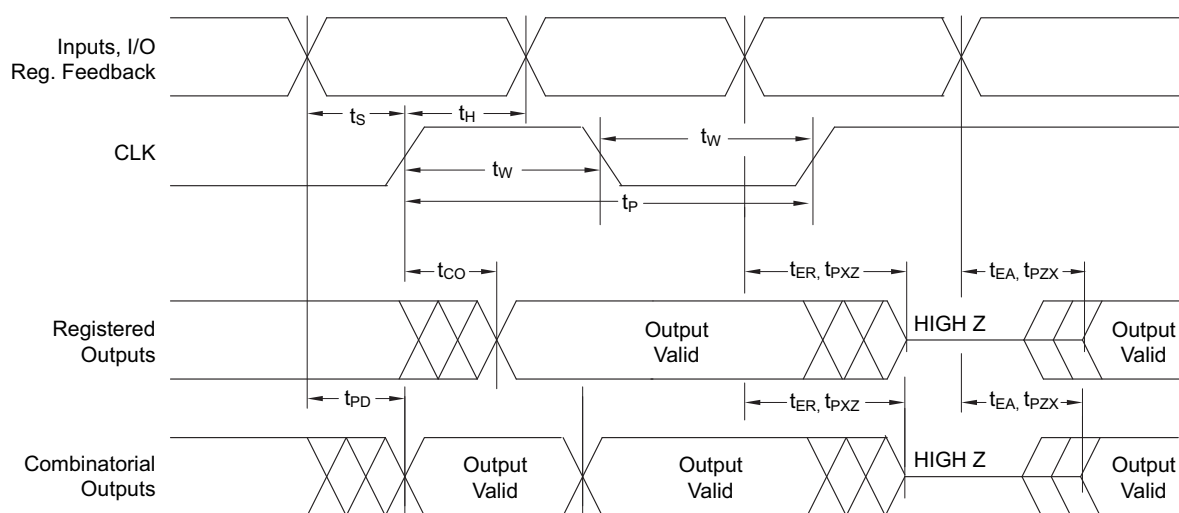
## 3.5 AC Characteristics

**Table 3-4. AC Characteristics<sup>(1)</sup>**

| Symbol    | Parameter                                  |                     | -10 |     | -15 |     | Units |
|-----------|--------------------------------------------|---------------------|-----|-----|-----|-----|-------|
|           |                                            |                     | Min | Max | Min | Max |       |
| $t_{PD}$  | Input or Feedback to Non-Registered Output | 8 outputs switching | 3   | 10  | 3   | 15  | ns    |
| $t_{CF}$  | Clock to Feedback                          |                     |     | 6   |     | 8   | ns    |
| $t_{CO}$  | Clock to Output                            |                     | 2   | 7   | 2   | 10  | ns    |
| $t_S$     | Input or Feedback Setup Time               |                     | 7.5 |     | 12  |     | ns    |
| $t_H$     | Hold Time                                  |                     | 0   |     | 0   |     | ns    |
| $t_P$     | Clock Period                               |                     | 12  |     | 16  |     | ns    |
| $t_W$     | Clock Width                                |                     | 6   |     | 8   |     | ns    |
| $f_{MAX}$ | External Feedback $1/(t_S + t_{CO})$       |                     |     | 68  |     | 45  | MHz   |
|           | Internal Feedback $1/(t_S + t_{CF})$       |                     |     | 74  |     | 50  |       |
|           | No Feedback $1/(t_P)$                      |                     |     | 83  |     | 62  |       |
| $t_{EA}$  | Input to Output Enable — Product Term      |                     | 3   | 10  | 3   | 15  | ns    |
| $t_{ER}$  | Input to Output Disable — Product Term     |                     | 2   | 10  | 2   | 15  | ns    |
| $t_{PZX}$ | $\overline{OE}$ pin to Output Enable       |                     | 2   | 10  | 2   | 15  | ns    |
| $t_{PXZ}$ | $\overline{OE}$ pin to Output Disable      |                     | 1.5 | 10  | 1.5 | 15  | ns    |

Note: 1. See ordering information for valid part numbers and speed grades.

**Figure 3-1. AC Waveforms<sup>(3,6)</sup>**

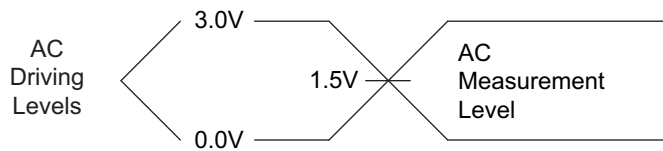


Note 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V 3.0V, unless otherwise specified.

## 3.6 Input Test Waveforms

### 3.6.1 Input Test Waveforms and Measurement Levels

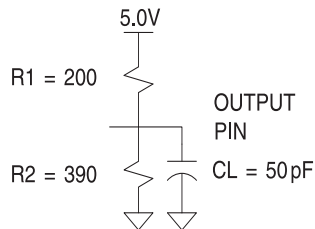
Figure 3-2. Input Test Waveforms and Measurement Levels



$t_R, t_F < 5\text{ns}$  (10% to 90%)

### 3.6.2 Output Test Loads (Commercial)

Figure 3-3. Output Test Loads



$C_L$  includes Test fixture and Probe capacitance

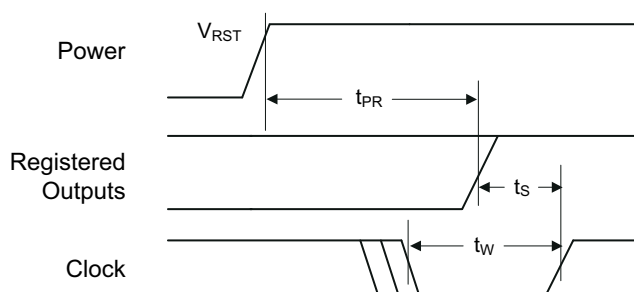
## 3.7 Power-up Reset

The registers in the ATF16V8B(QL) are designed to reset during power-up. At a point delayed slightly from  $V_{CC}$  crossing  $V_{RST}$ , all registers will be reset to the low state. As a result, the registered output state will always be high on power-up.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how  $V_{CC}$  actually rises in the system, the following conditions are required:

1. The  $V_{CC}$  rise must be monotonic,
2. After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and
3. The clock must remain stable during  $t_{PR}$ .

Figure 3-4. Power-up Reset Waveforms



**Table 3-5. Power-up Reset Parameters**

| Parameter | Description            | Typ | Max   | Units |
|-----------|------------------------|-----|-------|-------|
| $t_{PR}$  | Power-up Reset Time    | 600 | 1,000 | ns    |
| $V_{RST}$ | Power-up Reset Voltage | 3.8 | 4.5   | V     |

### 3.8 Preload of Registered Outputs

The ATF16V8B(QL) device registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically by most of the approved programmers after the programming.

## 4. Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF16V8B(QL) fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64-bit User Signature remains accessible.

The security fuse should be programmed last, as its effect is immediate.

## 5. Electronic Signature Word

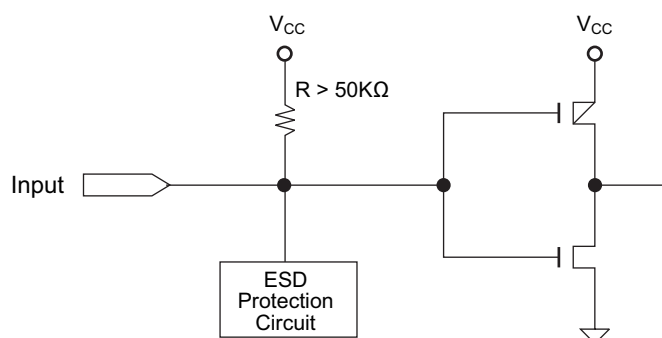
There are 64 bits of programmable memory that are always available to the user, even if the device is secured. These bits can be used for user-specific data.

## 6. Programming/Erasing

Programming/erasing is performed using standard PLD programmers.

## 7. Input and I/O Pull-ups

All ATF16V8B(QL) family members have internal input and I/O pull-up resistors. Therefore, whenever inputs or I/Os are not being driven externally, they will float to  $V_{CC}$ . This ensures that all logic array inputs are at known states. These are relatively weak active pull-ups that can easily be over driven by TTL-compatible drivers (see input and I/O diagrams below).

**Figure 7-1. Input Diagram**

The logic option and functional diagrams describe the ATF16V8B(QL) architecture. Eight configurable macrocells can be configured as a registered output, combinatorial I/O, combinatorial output, or dedicated input. The ATF16V8B(QL) can be configured in one of three different modes. Each mode makes the ATF16V8B(QL) look like a different device. Most PLD compilers can choose the right mode automatically. The user can also force the selection by supplying the compiler with a mode selection. The determining factors would be the usage of register versus combinatorial outputs and dedicated outputs versus outputs with output enable control.

The ATF16V8B(QL) universal architecture can be programmed to emulate many 20-pin PAL devices. These architectural subsets can be found in each of the configuration modes described in the following pages. The user can download the listed subset device JEDEC programming file to the PLD programmer, and the ATF16V8B(QL) can be configured to act like the chosen device. Check with your programmer manufacturer for this capability.

## 9. Software Support

### Table 9-1. Compiler Mode Selection

|                     | Registered | Complex | Simple  | Auto Select |
|---------------------|------------|---------|---------|-------------|
| CUPL, Atmel WinCUPL | G16V8MS    | G16V8MA | G16V8AS | G16V8       |

## 10. Macrocell Configuration

Software compilers support the three different OMC modes as different device types. Most compilers have the ability to automatically select the device type, generally based on the register usage and Output Enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. The different device types can be used to override the automatic device selection by the software. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode:

- **Registered Mode**  
Pin 1 and pin 11 are permanently configured as clock and output enable respectively. These pins cannot be configured as dedicated inputs in the registered mode.
- **Complex Mode**  
Pin 1 and pin 11 become dedicated inputs and use the feedback paths of pin 19 and pin 12 respectively. Because of this feedback path usage, pin 19 and pin 12 do not have the feedback option in this mode.
- **Simple Mode**  
All feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 15 and 16) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

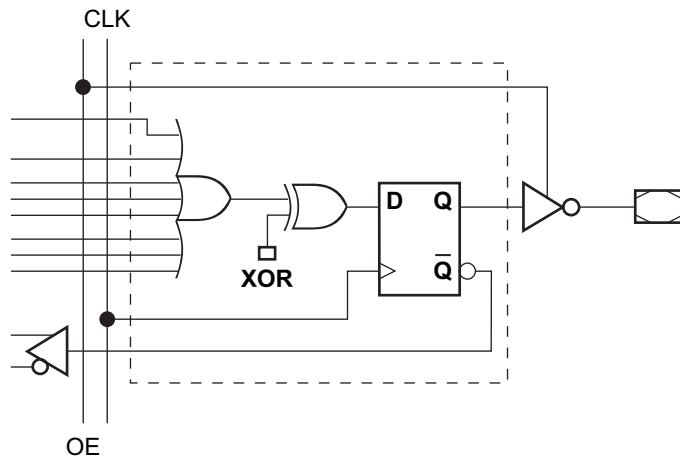
### 10.1 ATF16V8B(QL) Registered Mode

**PAL Device Emulation/PAL Replacement.** The registered mode is used if one or more registers are required. Each macrocell can be configured as either a registered or combinatorial output or I/O, or as an input. For a registered output or I/O, the output is enabled by the  $\overline{OE}$  pin, and the register is clocked by the CLK pin. Eight product terms are allocated to the sum term. For a combinatorial output or I/O, the output enable is controlled by a product term, and seven product terms are allocated to the sum term. When the macrocell is configured as an input, the output enable is permanently disabled.

Any register usage will make the compiler select this mode. The following registered devices can be emulated using this mode:

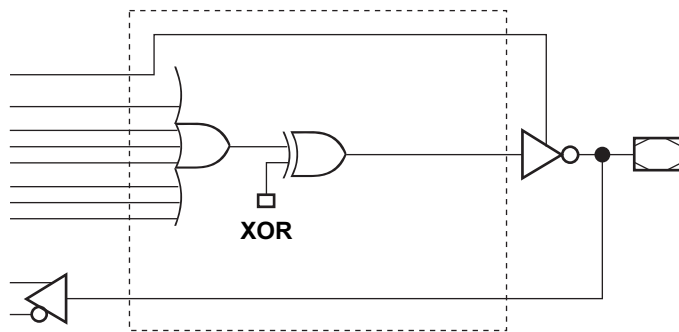
- |        |         |
|--------|---------|
| • 16R8 | • 16RP8 |
| • 16R6 | • 16RP6 |
| • 16R4 | • 16RP4 |

**Figure 10-1. Registered Configuration for Registered Mode<sup>(1)(2)</sup>**



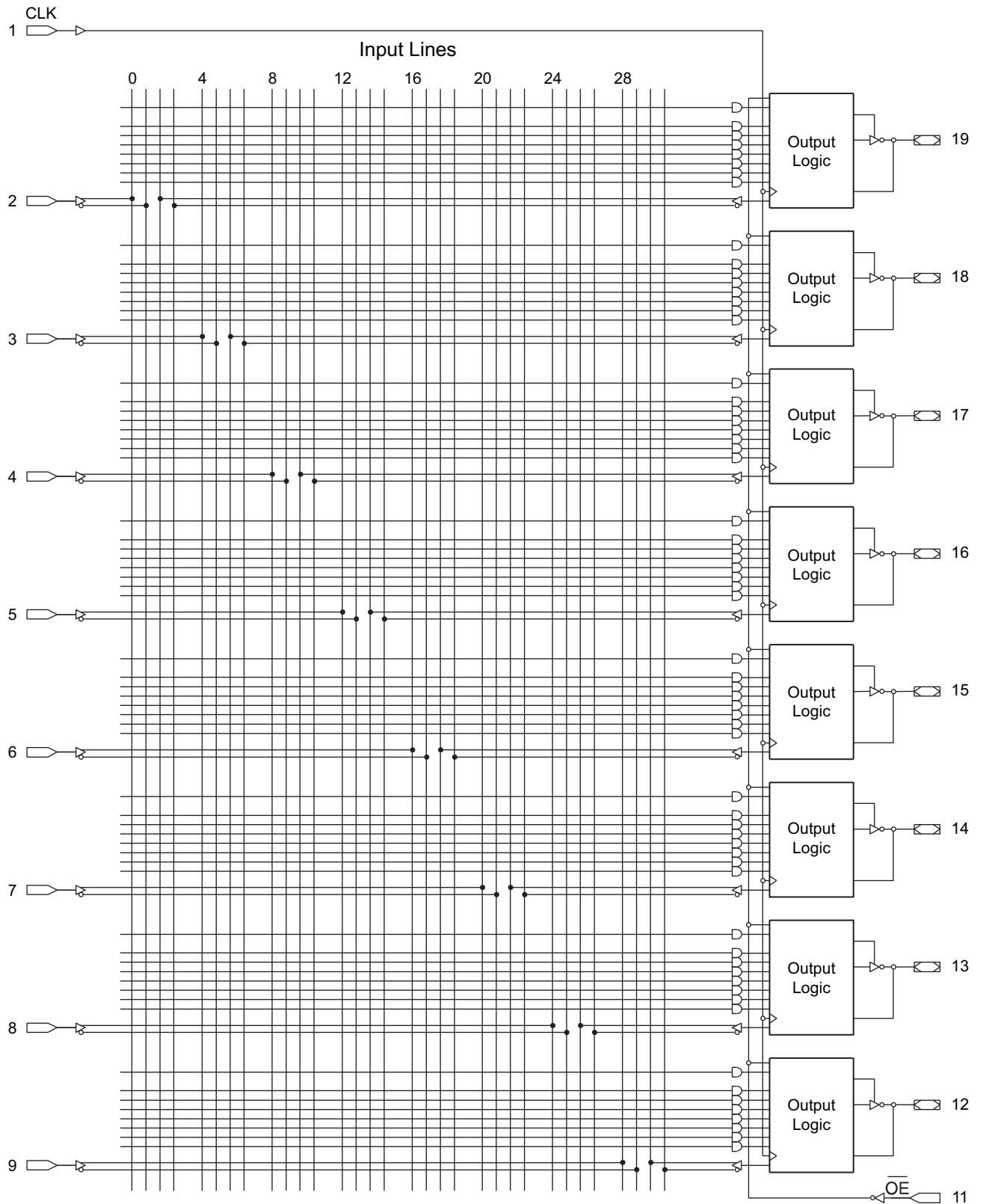
- Notes:
1. Pin 1 controls common CLK for the registered outputs. Pin 11 controls common  $\overline{OE}$  for the registered outputs. Pin 1 and Pin 11 are permanently configured as CLK and  $\overline{OE}$ .
  2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

**Figure 10-2. Combinatorial Configuration for Registered Mode<sup>(1)(2)</sup>**



- Notes:
1. Pin 1 and Pin 11 are permanently configured as CLK and  $\overline{OE}$ .
  2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

**Figure 10-3. Registered Mode Logic Diagram**



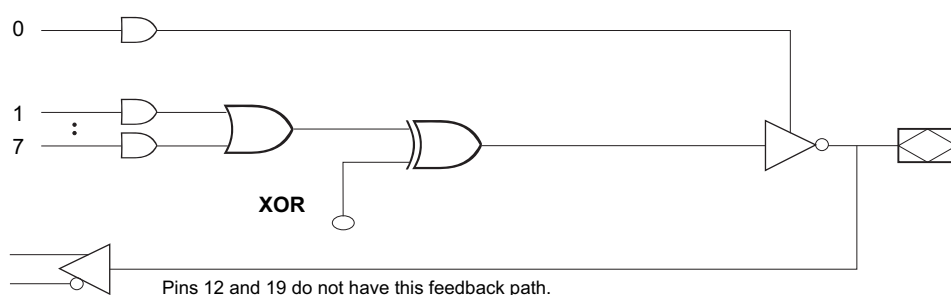
## 10.2 ATF16V8B(QL) Complex Mode

**PAL Device Emulation/PAL Replacement.** In the complex mode, combinatorial output and I/O functions are possible. Pins 1 and 11 are regular inputs to the array. Pins 13 through 18 have pin feedback paths back to the AND-array, which makes full I/O capability possible. Pins 12 and 19 (outermost macrocells) are outputs only. They do not have input capability. In this mode, each macrocell has seven product terms going to the sum term and one product term enabling the output.

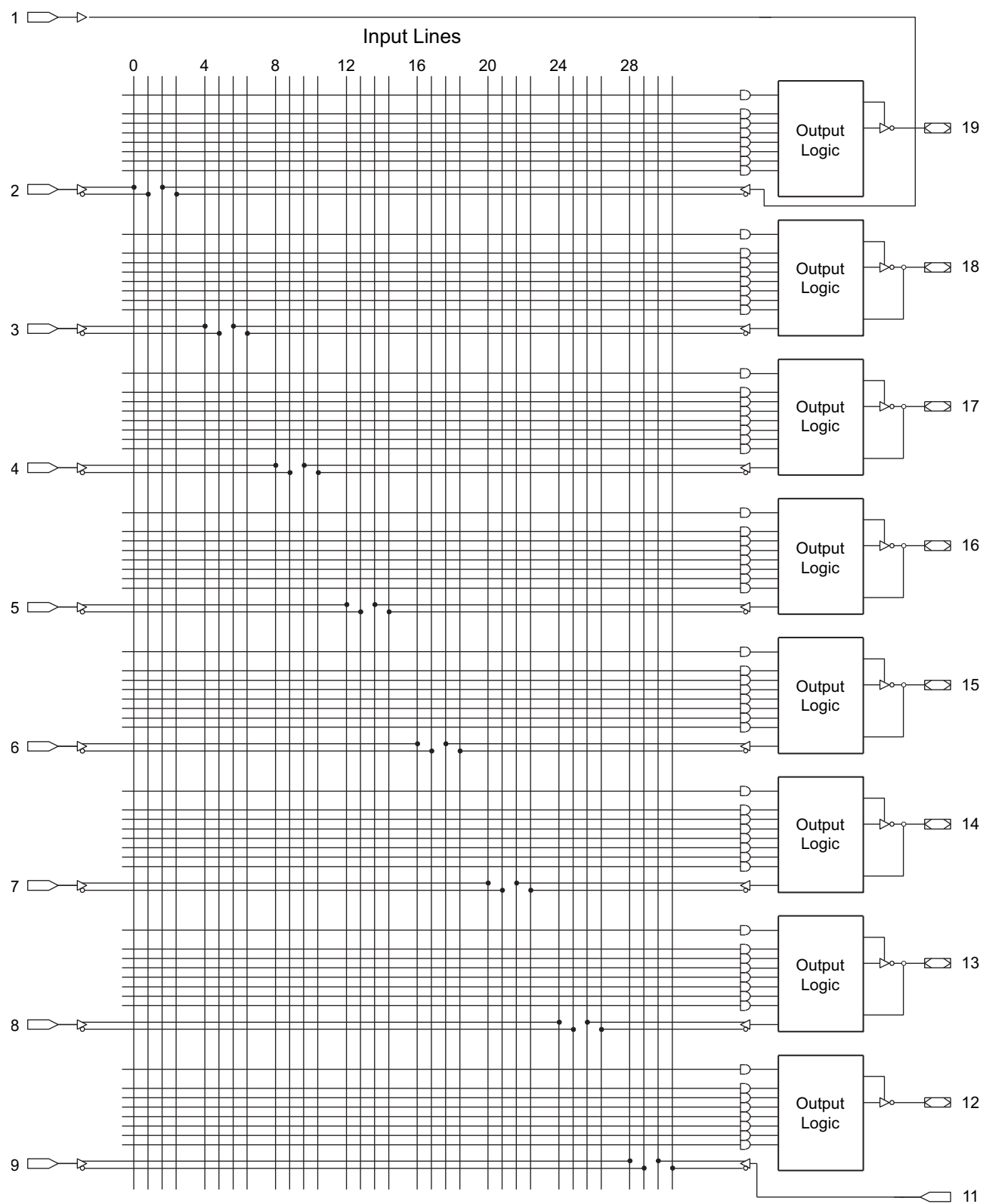
Combinatorial applications with an OE requirement will make the compiler select this mode. The following devices can be emulated using this mode:

- 16L8
- 16H8
- 16P8

**Figure 10-4. Complex Mode Option**



**Figure 10-5. Complex Mode Logic Diagram**



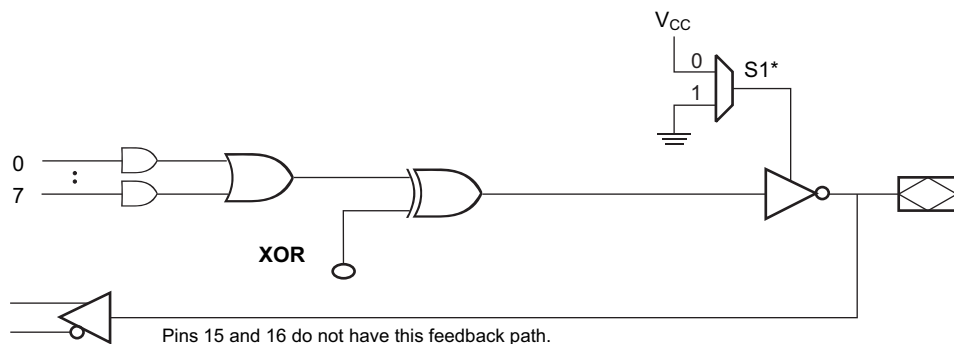
### 10.3 ATF16V8B(QL) Simple Mode

**PAL Device Emulation/PAL Replacement.** In the Simple Mode, 8 product terms are allocated to the sum term. Pins 15 and 16 (center macrocells) are permanently configured as combinatorial outputs. Other macrocells can be either inputs or combinatorial outputs with pin feedback to the AND-array. Pins 1 and 11 are regular inputs.

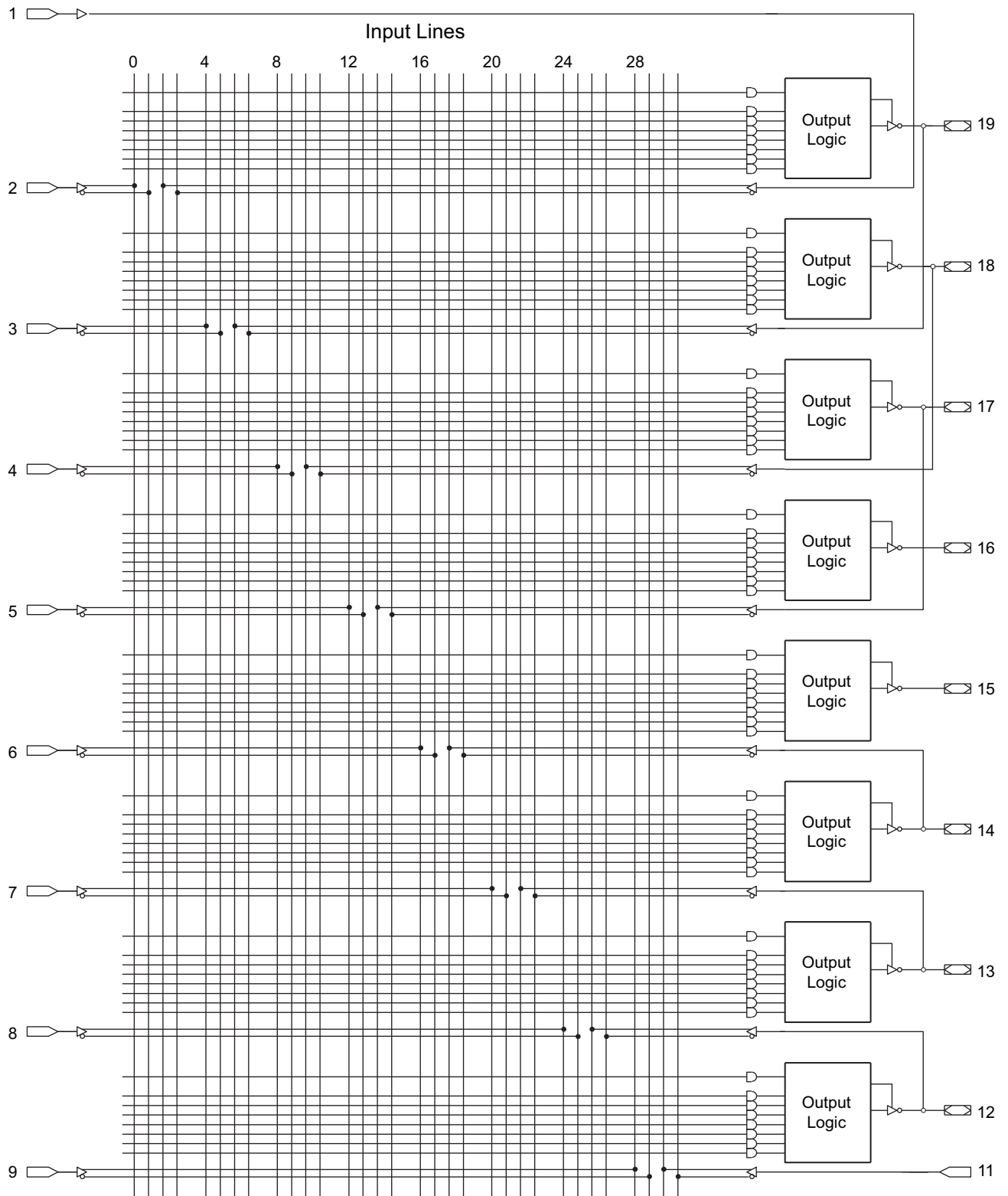
The compiler selects this mode when all outputs are combinatorial without OE control. The following simple PALs can be emulated using this mode:

- |        |        |        |
|--------|--------|--------|
| • 10L8 | • 10H8 | • 10P8 |
| • 12L6 | • 12H6 | • 12P6 |
| • 14L4 | • 14H4 | • 14P4 |
| • 16L2 | • 16H2 | • 16P2 |

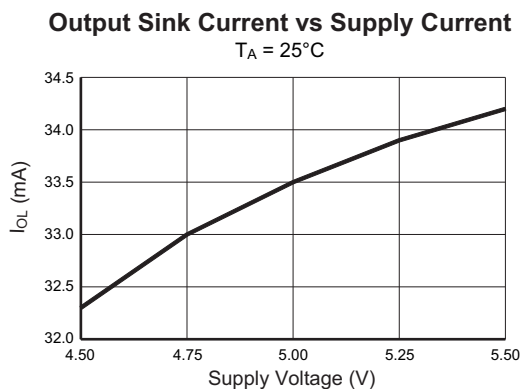
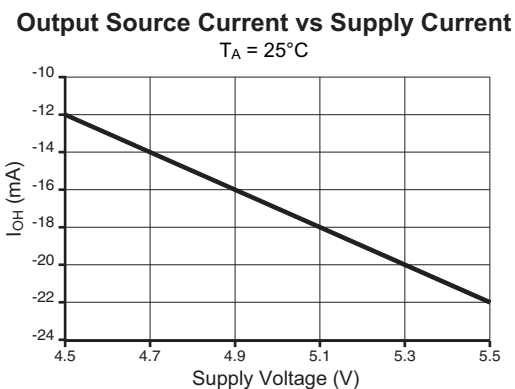
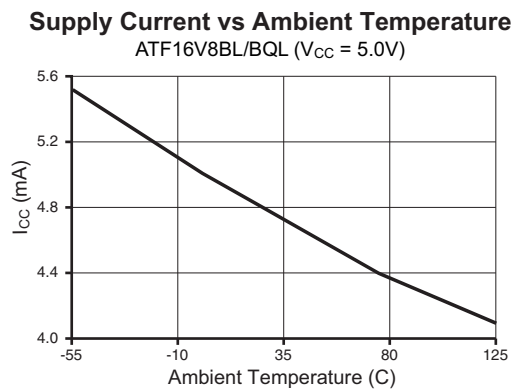
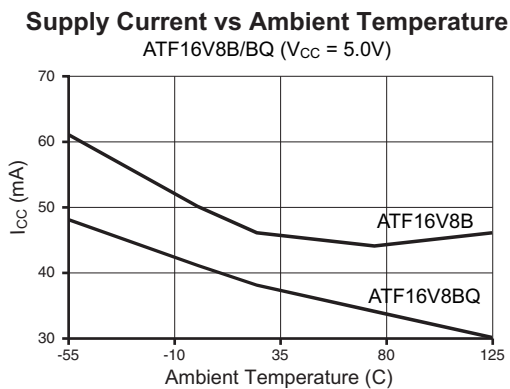
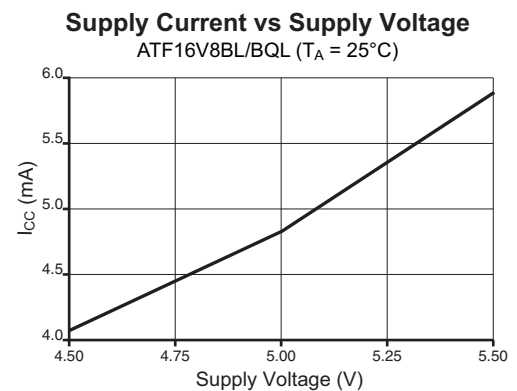
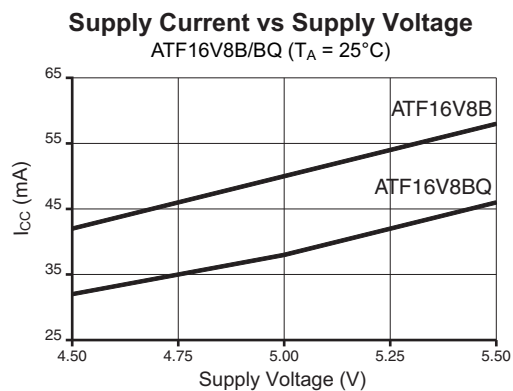
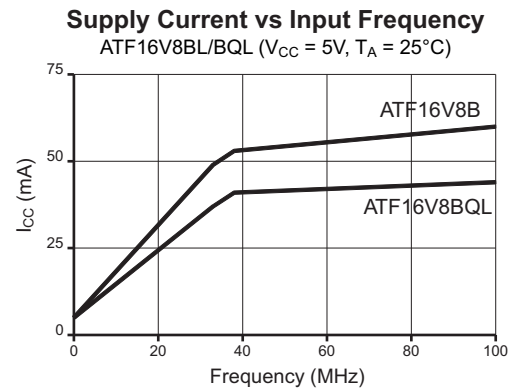
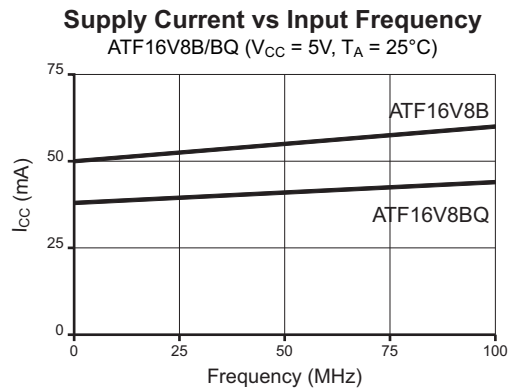
Figure 10-6. Simple Mode Option



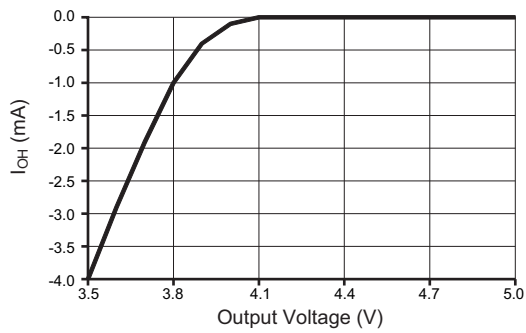
**Figure 10-7. Simple Mode Logic Diagram**



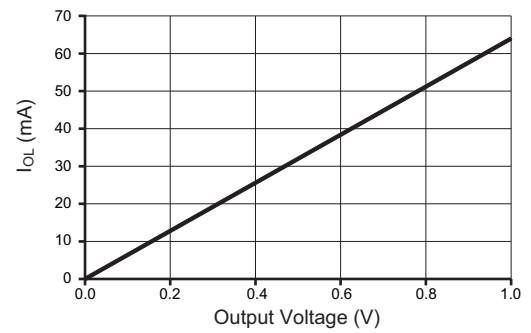
## 11. Test Characterization Data



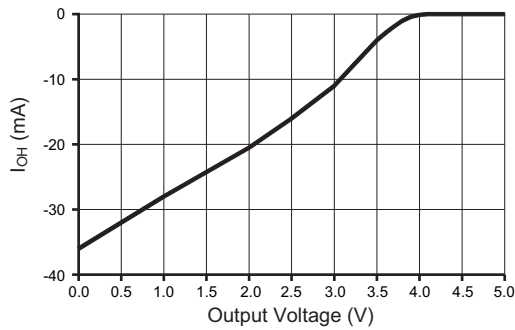
**Output Source Current vs Output Voltage**  
( $V_{CC} = 5.0V$ ,  $T_A = 25^\circ C$ )



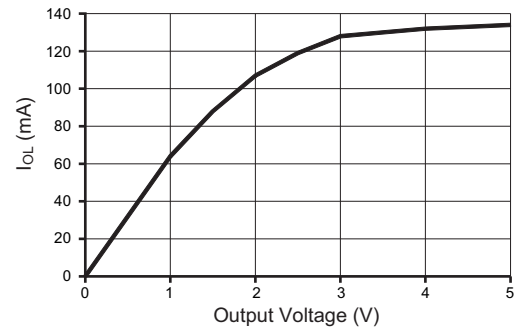
**Output Sink Current vs Output Voltage**  
( $V_{CC} = 5.0V$ ,  $T_A = 25^\circ C$ )



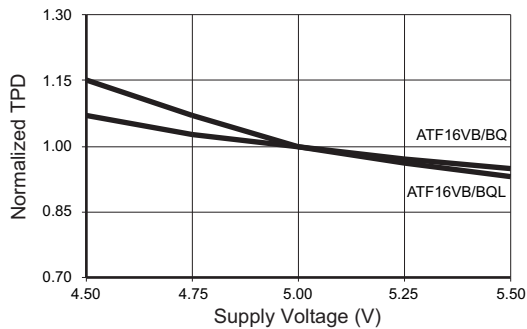
**Output Source Current vs Output Voltage**  
( $V_{CC} = 5.0V$ ,  $T_A = 25^\circ C$ )



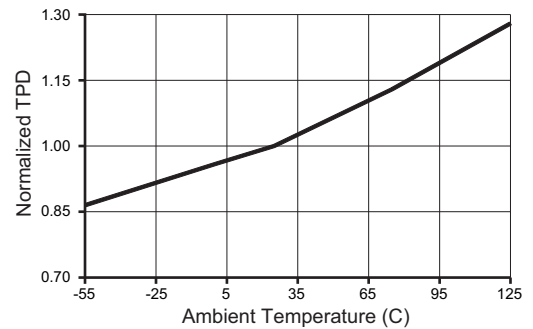
**Output Sink Current vs Output Voltage**  
( $V_{CC} = 5.0V$ ,  $T_A = 25^\circ C$ )



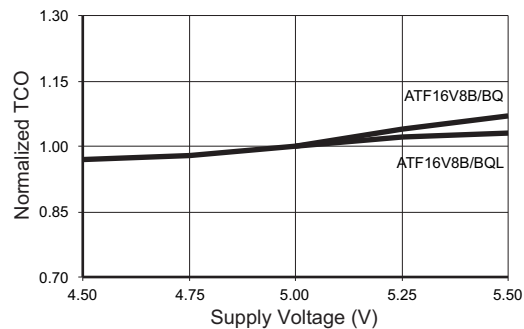
**Normalized TPD vs Supply Voltage**  
( $T_A = 25^\circ C$ )



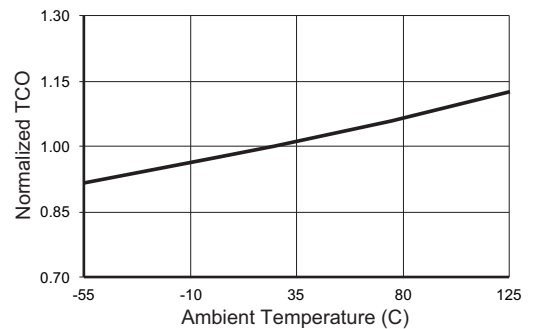
**Normalized TPD vs Ambient Temperature**  
( $V_{CC} = 5.0V$ )

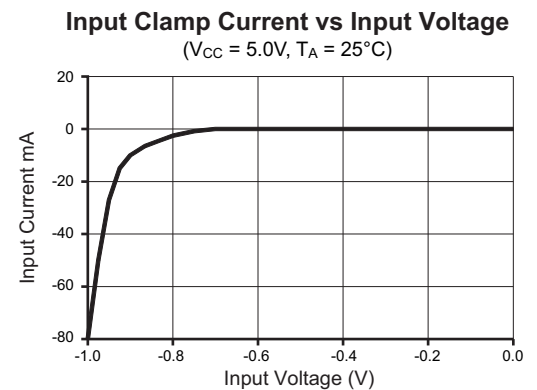
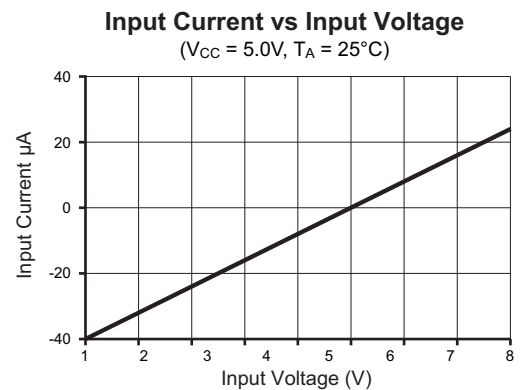
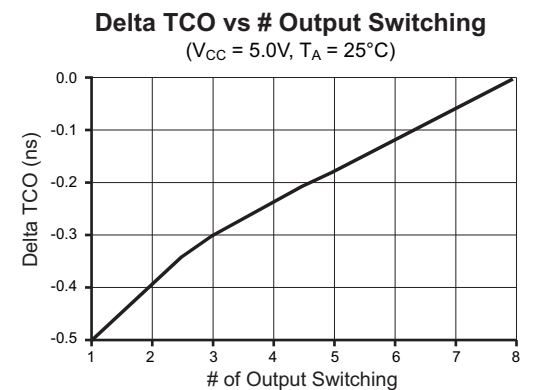
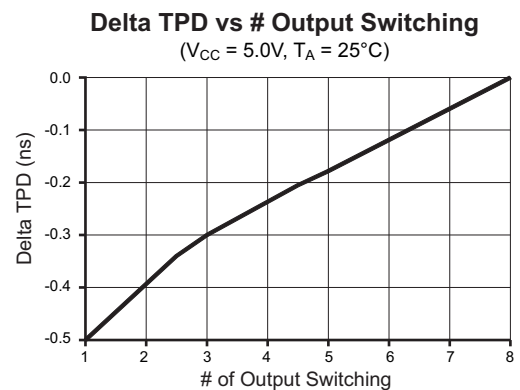
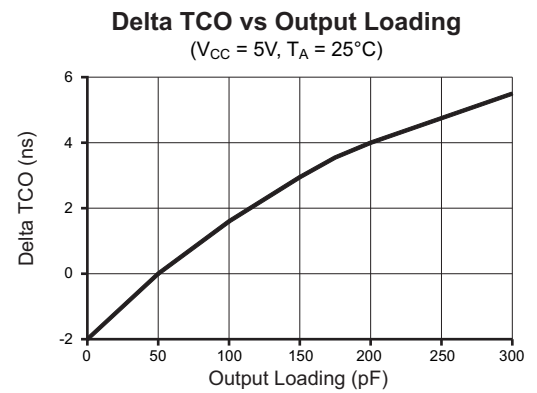
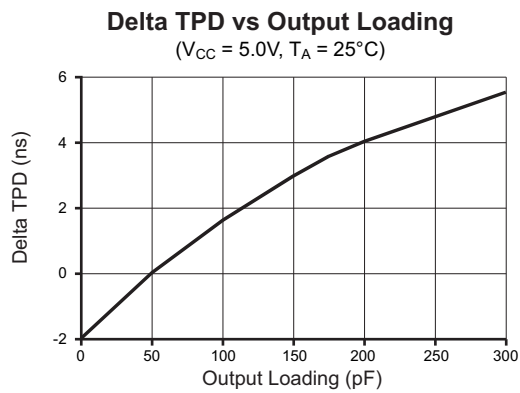
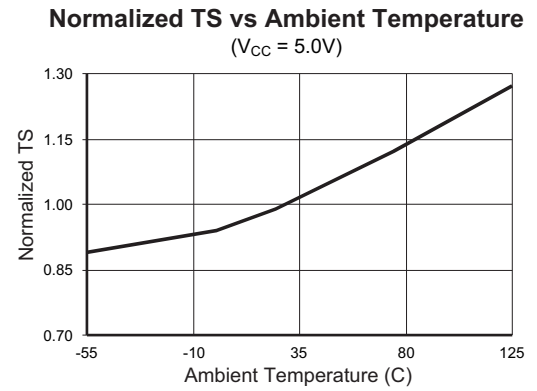
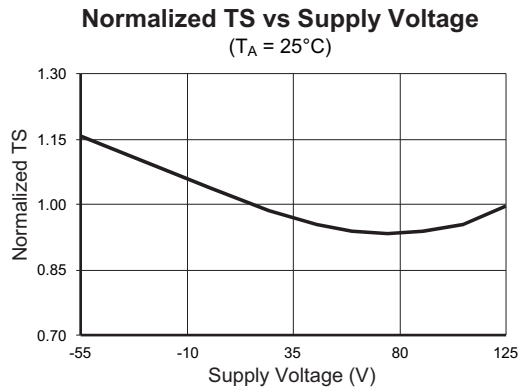


**Normalized TCO vs Supply Voltage**  
( $T_A = 25^\circ C$ )



**Normalized TCO vs Ambient Temperature**  
( $V_{CC} = 5.0V$ )





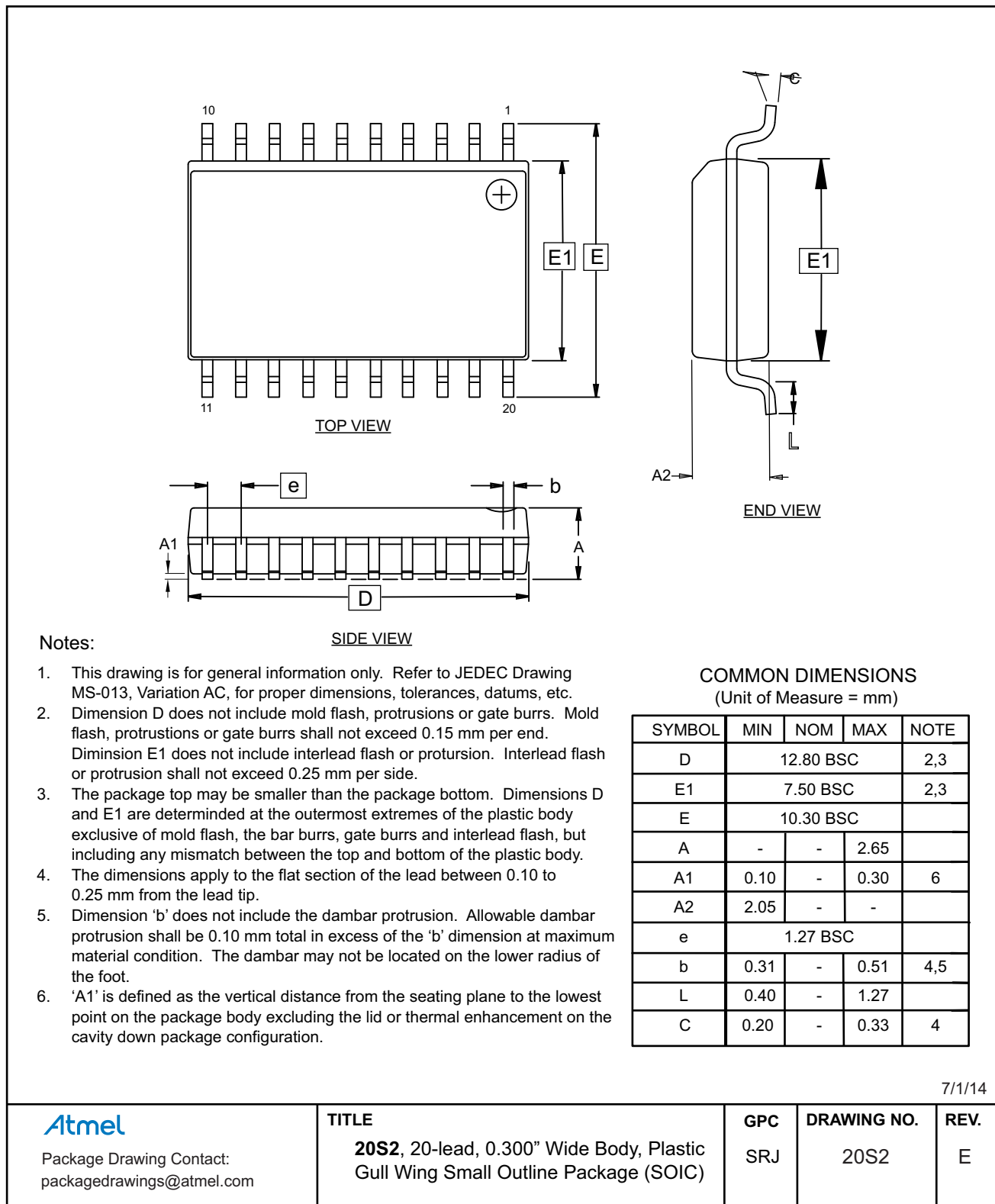
## 12. Ordering Information

| $t_{PD}$<br>(ns) | $t_s$<br>(ns) | $t_{CO}$<br>(ns) | Ordering Code   | Package | Operation Range                                                   |
|------------------|---------------|------------------|-----------------|---------|-------------------------------------------------------------------|
| 10               | 7.5           | 7                | ATF16V8B-10JU   | 20J     | Industrial<br>(Pb/Halide-free/RoHS Compliant)<br>(-40°C to +85°C) |
| 15               | 12            | 10               | ATF16V8B-15SU   | 20S2    |                                                                   |
|                  |               |                  | ATF16V8B-15XU   | 20X     |                                                                   |
|                  |               |                  | ATF16V8B-15PU   | 20P3    |                                                                   |
|                  |               |                  | ATF16V8B-15JU   | 20J     |                                                                   |
| 15               | 12            | 10               | ATF16V8BQL-15SU | 20S2    | Industrial<br>(Pb/Halide-free/RoHS Compliant)<br>(-40°C to +85°C) |
|                  |               |                  | ATF16V8BQL-15XU | 20X     |                                                                   |
|                  |               |                  | ATF16V8BQL-15PU | 20P3    |                                                                   |
|                  |               |                  | ATF16V8BQL-15JU | 20J     |                                                                   |

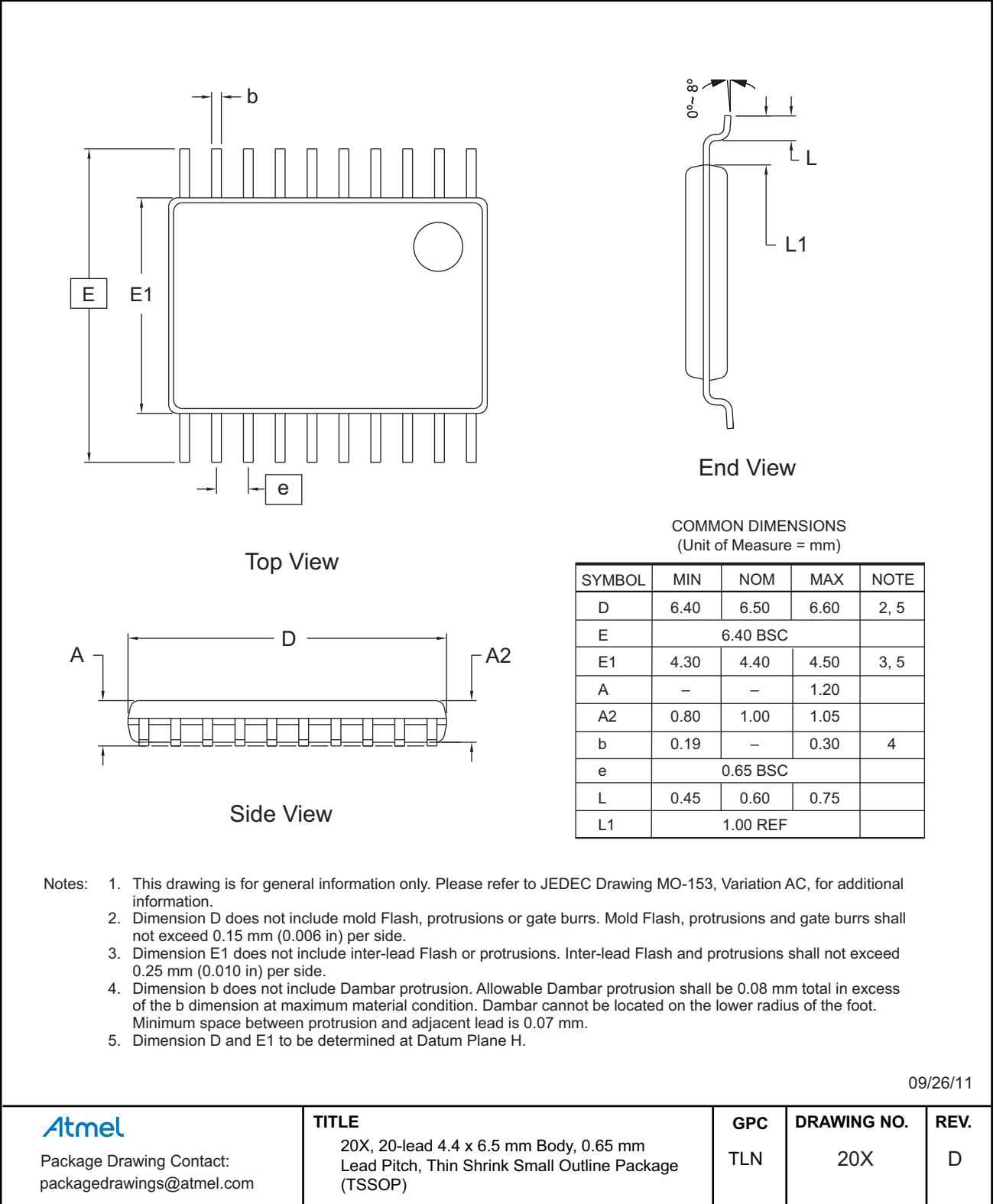
|             | Package Type                                                   |
|-------------|----------------------------------------------------------------|
| <b>20S2</b> | 20-lead, 0.300" wide, Plastic Gull-wing Small Outline (SOIC)   |
| <b>20X</b>  | 20-lead, 4.4mm wide, Plastic Thin Shrink Small Outline (TSSOP) |
| <b>20P3</b> | 20-lead, 0.300" wide, Plastic Dual Inline Package (PDIP)       |
| <b>20J</b>  | 20-lead, Plastic J-leaded Chip Carrier (PLCC)                  |

## 13. Packaging Information

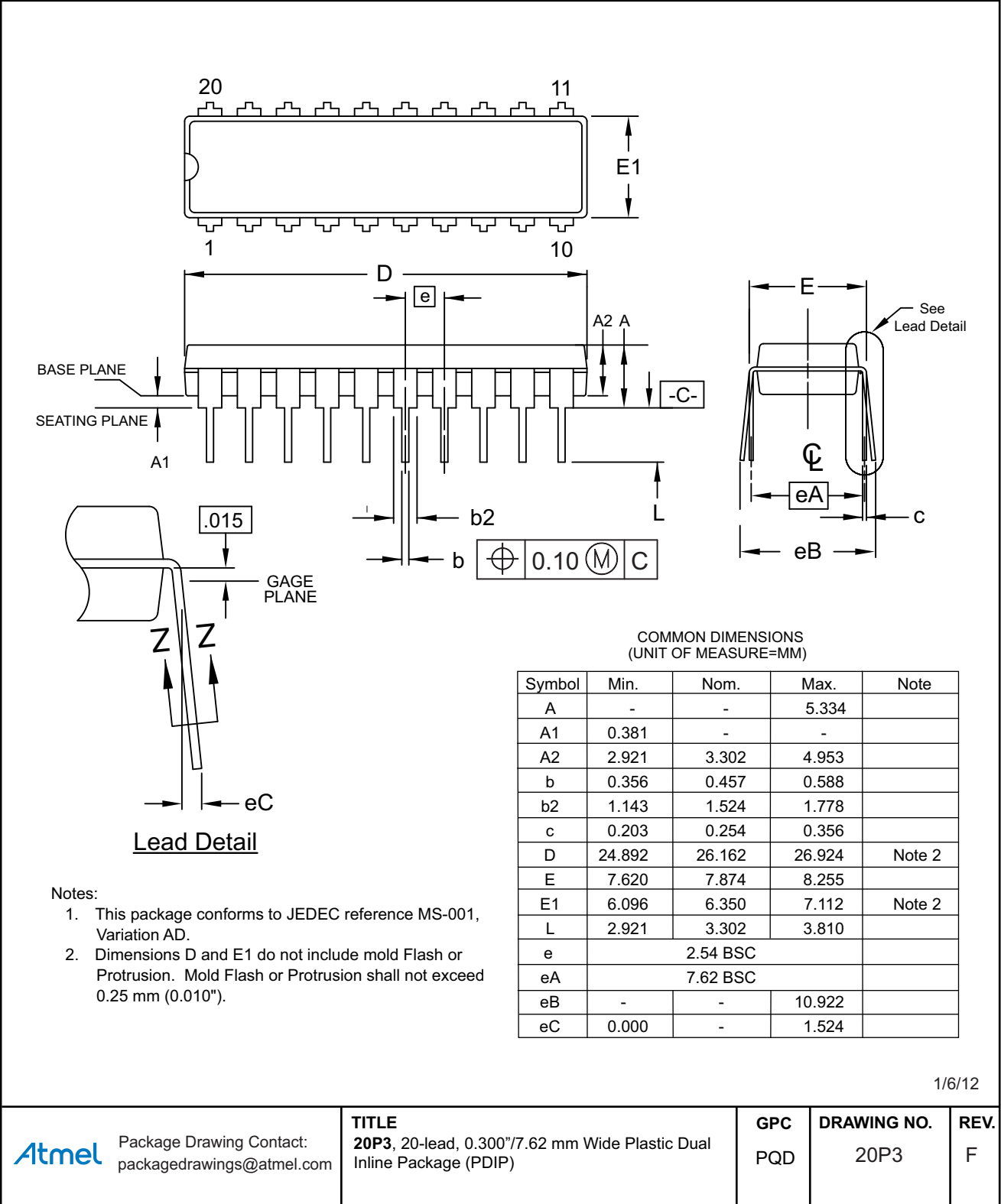
### 13.1 20S2 — 20-lead SOIC



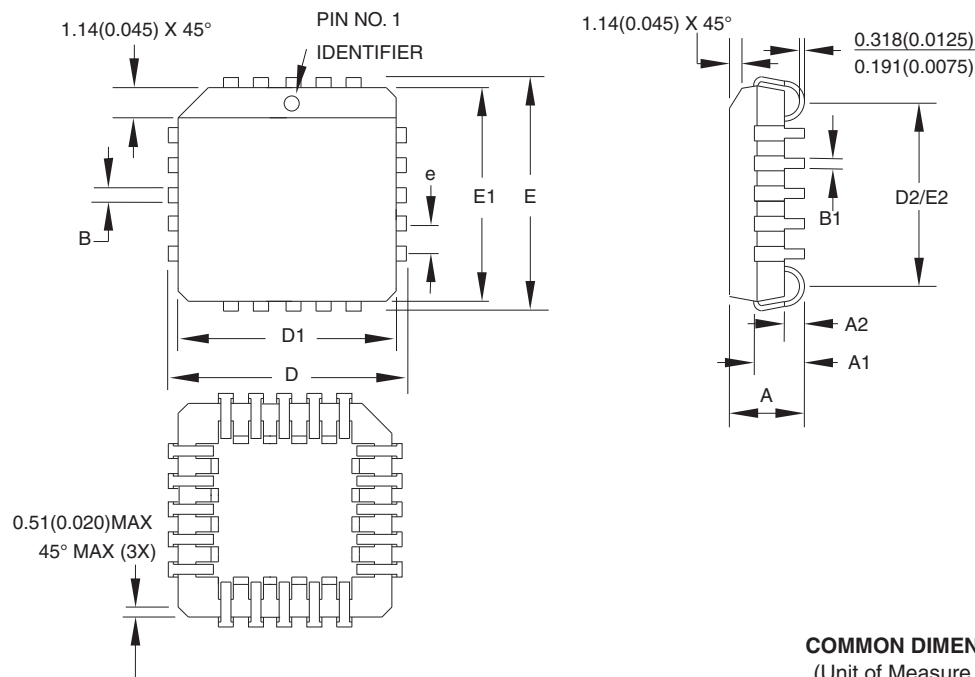
13.2 20X — 20-lead TSSOP



13.3 20P3 — 20-lead PDIP



13.4 20J — 20-lead PLCC



COMMON DIMENSIONS  
(Unit of Measure = mm)

| SYMBOL | MIN       | NOM | MAX    | NOTE   |
|--------|-----------|-----|--------|--------|
| A      | 4.191     | —   | 4.572  |        |
| A1     | 2.286     | —   | 3.048  |        |
| A2     | 0.508     | —   | —      |        |
| D      | 9.779     | —   | 10.033 |        |
| D1     | 8.890     | —   | 9.042  | Note 2 |
| E      | 9.779     | —   | 10.033 |        |
| E1     | 8.890     | —   | 9.042  | Note 2 |
| D2/E2  | 7.366     | —   | 8.382  |        |
| B      | 0.660     | —   | 0.813  |        |
| B1     | 0.330     | —   | 0.533  |        |
| e      | 1.270 TYP |     |        |        |

- Notes: 1. This package conforms to JEDEC reference MS-018, Variation AA  
2. Dimensions D1 and E1 do not include mold protrusion.  
Allowable protrusion is .010"(0.254mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.  
3. Lead coplanarity is 0.004" (0.102mm) maximum

10/04/01



Package Drawing Contact:  
packagedrawings@atmel.com

TITLE  
20J, 20-lead, Plastic J-leaded Chip Carrier (PLCC)

| DRAWING NO. | REV. |
|-------------|------|
| 20J         | B    |



## 14. Revision History

| Doc. Rev. | Date    | Comments                                                                                                                                                                                                               |
|-----------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0364K     | 07/2014 | Removed ATF16V8BQ device and commercial options due to becoming obsolete.<br>Updated package drawings to most current versions and the 20S to 20S2 package drawing.<br>Updated template, Atmel logos, disclaimer page. |
| 0364J     | 07/2005 | Green Package options added in 2005.                                                                                                                                                                                   |
|           | 1999    | ATF16V8B-25 JC/PC/SC/XC/JI/PI/SI/XI and ATF16V8BQL-25 JC/PC/SC/XC/JI/PI/SI/XI were obsoleted in August 1999 and removed from the datasheet.                                                                            |



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