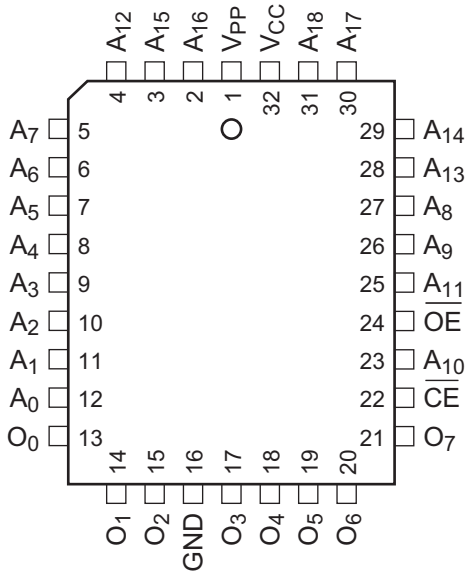
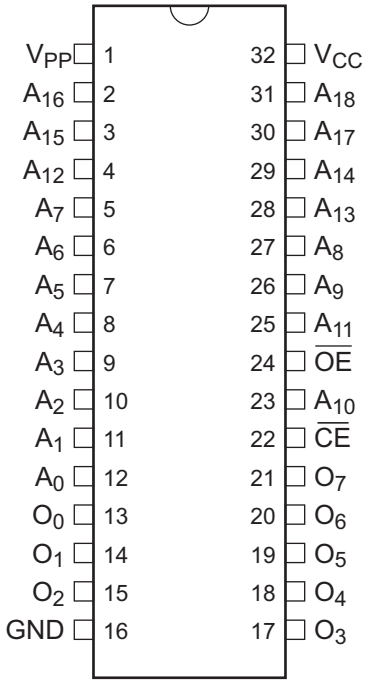
2. Pin Configurations and Pinouts

Pin Name	Function
V_{PP}	Peak to Peak Voltage
A_0 - A_{18}	Address Inputs
O_0 - O_7	Outputs
GND	Ground
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Device Power Supply

32-lead PLCC
Top view



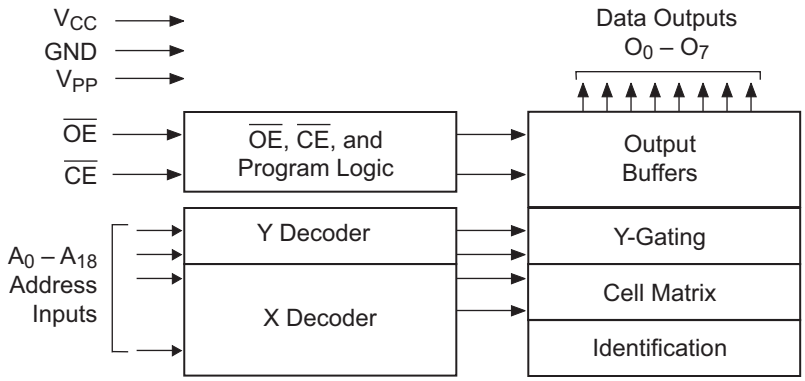
32-lead PDIP
Top view



3. Switching Considerations

Switching between active and standby conditions via the Chip Enable ($\overline{CE}$) pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed datasheet limits, resulting in device nonconformance. At a minimum, a 0.1µF, high-frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and ground terminals of the device — as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

4. Block Diagram



5. Absolute maximum ratings*

Temperature under bias-55°C to +125°C
Storage temperature . . . . . -65°C to +150°C

Voltage on any pin with
respect to ground. . . . . .-2.0V to +7.0V

Voltage on A_9 with
respect to ground . . . . . .-2.0V to +14.0V

V_{PP} supply voltage with
respect to ground. . . . . .-2.0V to +14.0V

*Notice: Stresses beyond those listed under “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6. Elelectrical Characteristics

6.1 DC and AC characteristics

Table 6-1. Operating modes

Mode/Pin	$\overline{CE}$	$\overline{OE}$	Ai	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	Ai	X(1)	D_{OUT}
Output Disable	X	V_{IH}	X	X	High Z
Standby	V_{IH}	X	X	X	High Z
Rapid Program(2)	V_{IL}	V_{IH}	Ai	V_{PP}	D_{IN}
PGM Verify	X	V_{IL}	Ai	V_{PP}	D_{OUT}
PGM Inhibit	V_{IH}	V_{IH}	X	V_{PP}	High Z
Product Identification(4)	V_{IL}	V_{IL}	$A_9 = V_H$(3) $A_0 = V_{IH}$ or V_{IL} $A_1 – A_{18} = V_{IL}$	X	Identification Code

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to programming characteristics.
3. $V_H = 12.0 \pm 0.5V$.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A_9, which is set to V_H, and A_0, which is toggled low (V_{IL}) to select the manufacturer’s identification byte and high (V_{IH}) to select the device code byte.

6.2 DC and AC Operating Conditions for Read Operation

	Atmel AT27C040-70	Atmel AT27C040-90
Industrial Operating Temperature (Case)	-40°C to 85°C	-40°C to 85°C
V_{CC} Power Supply	5V ± 10%	5V ± 10%

6.3 DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1}[2]	V_{PP}[1] Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC1}[1] Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		1	mA
I_{CC}	V_{CC} Active Current	f = 5MHz, I_{OUT} = 0mA, $\overline{CE}$ = V_{IL}		30	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400µA	2.4		V

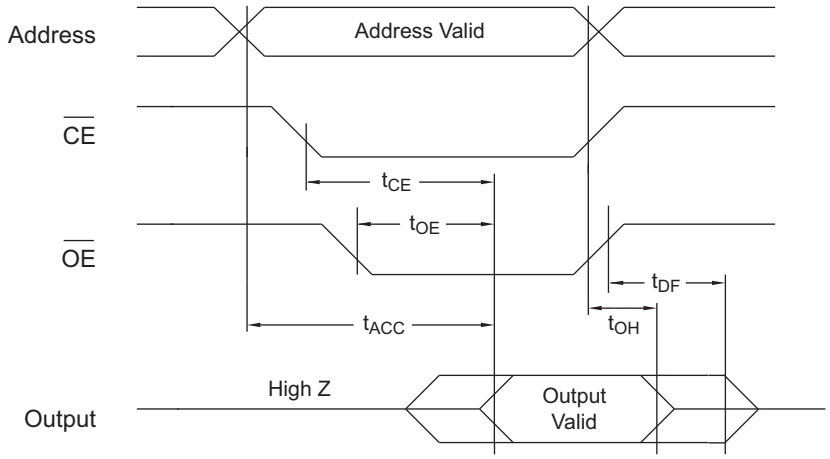
Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP}, and removed simultaneously with or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

6.4 AC Characteristics for Read Operation

			Atmel AT27C040				
			-70		-90		
Symbol	Parameter	Condition	Min	Max	Min	Max	Units
t_{ACC}[1]	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		70		90	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		70		90	ns
t_{OE}[1]	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		30		35	ns
t_{DF}[1]	$\overline{OE}$ or $\overline{CE}$ High to Output Float; whichever occurred first.			20		20	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$; whichever occurred first.		0		0		ns

Note: 1. See AC waveforms for read operation.

Figure 6-1. AC Waveforms for Read Operation[1]



Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled, and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Figure 6-2. Input Test Waveforms and Measurement Levels

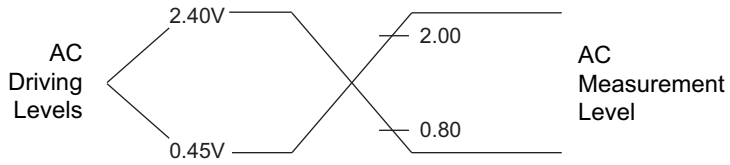


Figure 6-3. Output Test Load

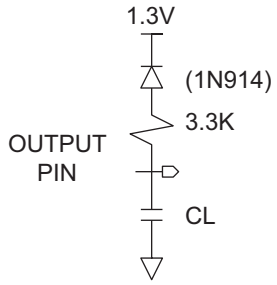


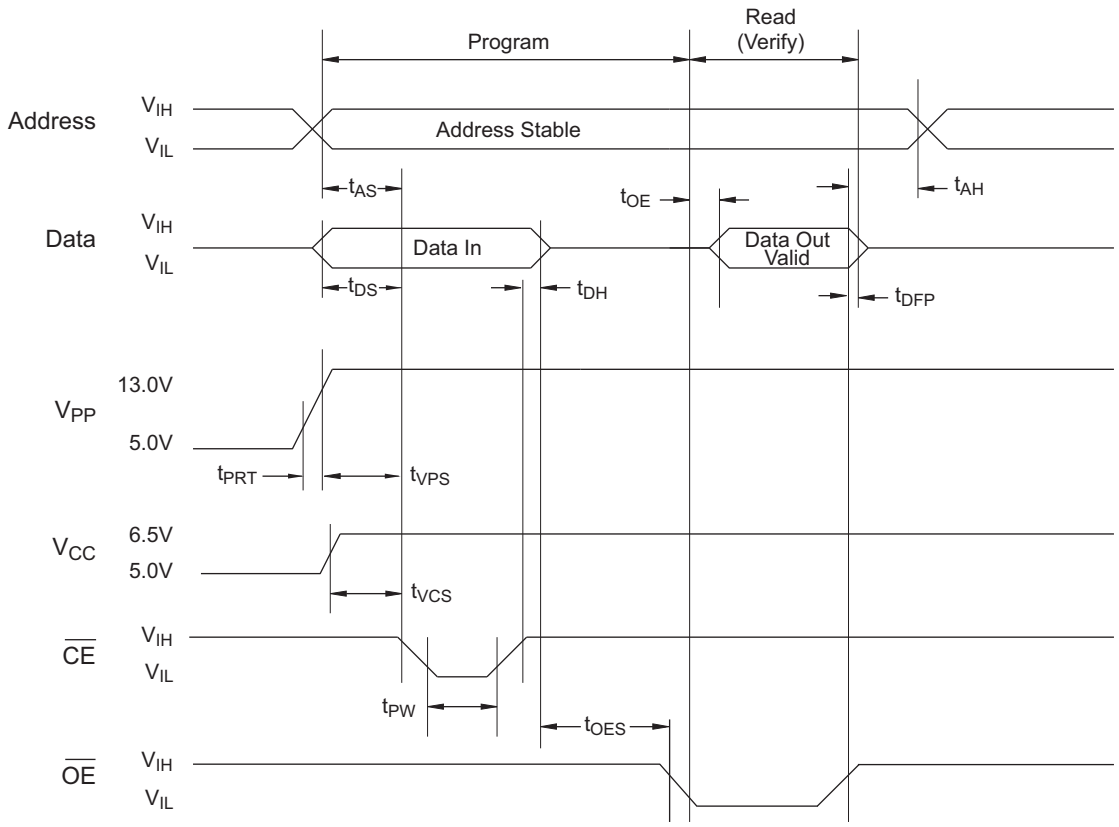
Table 6-2. Pin Capacitance

f = 1MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Figure 6-4. Programming Waveforms[1]



Notes:
1. The input timing reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device, but must be accommodated by the programmer.
3. When programming the AT27C040, a 0.1µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

Table 6-3. DC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V.

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.7	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program And Verify)			40	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE} = V_{IL}$		20	mA
V_{ID}	A_9 Product Identification Voltage		11.5	12.5	V

Table 6-4. AC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions[1]	Limits		Units
			Min	Max	
t_{AS}	Address Setup Time	Input rise and fall times: (10% to 90%) 20ns Input pulse levels: 0.45V to 2.4V Input timing reference level: 0.8V to 2.0V Output timing reference level: 0.8V to 2.0V	2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay[2]		0	130	ns
t_{VPS}	V_{pp} Setup Time		2		µs
t_{VCS}	V_{cc} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width[3]		95	105	µs
t_{OE}	Data Valid from $\overline{OE}$[2]			150	ns
t_{PRT}	V_{PP} Pulse Rise Time During Programming		50		ns

Notes:
1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}.
2. This parameter is only sampled, and is not 100% tested. Output float is defined as the point where data is no longer driven. See timing diagram.
3. Program pulse width tolerance is 100µs ± 5%.

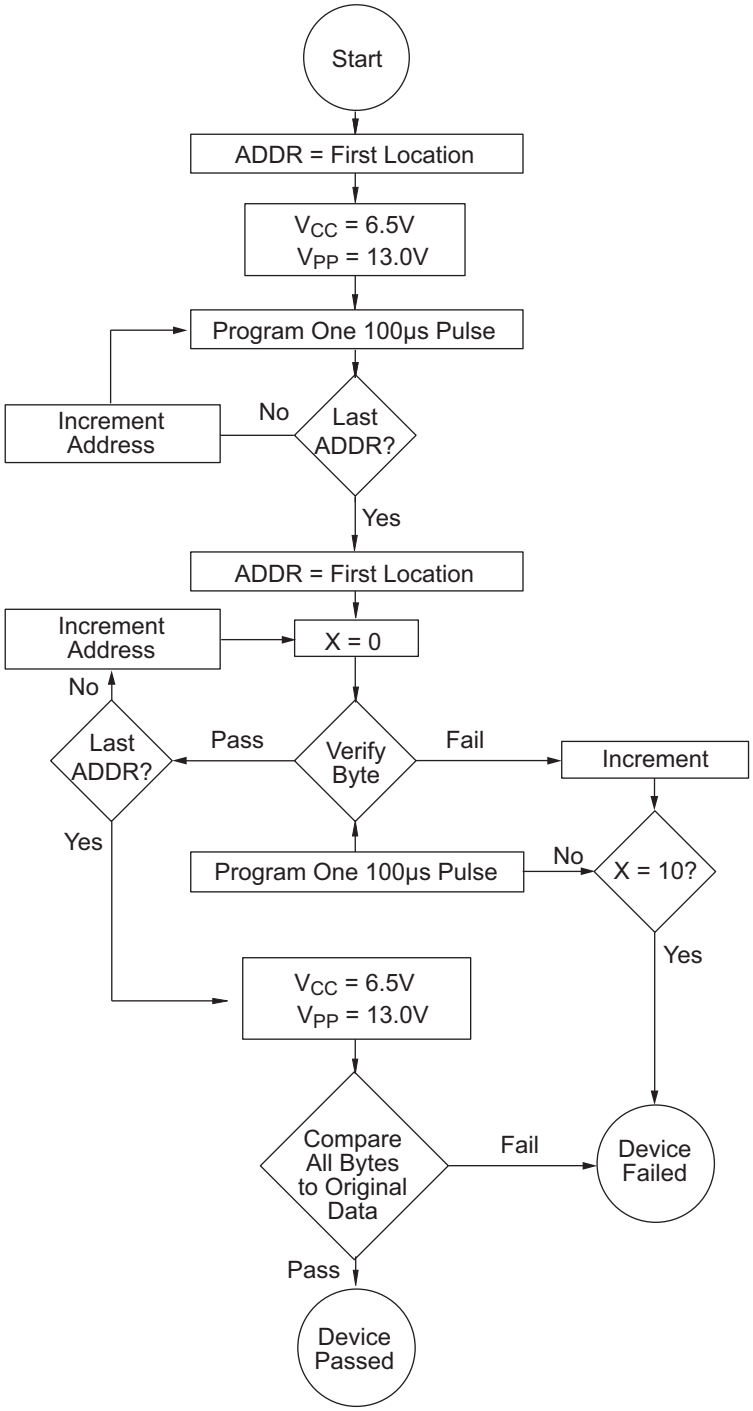
Table 6-5. Atmel AT27C040 Integrated Product Identification Code

Codes	Pins									Hex Data
	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	1	0	1	1	0B

7. Rapid programming algorithm

A 100µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to ten successive 100µs pulses are applied with a verification after each pulse. If the byte fails to verify after ten pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.

Figure 7-1. Rapid Programming Algorithm



8. Ordering Information

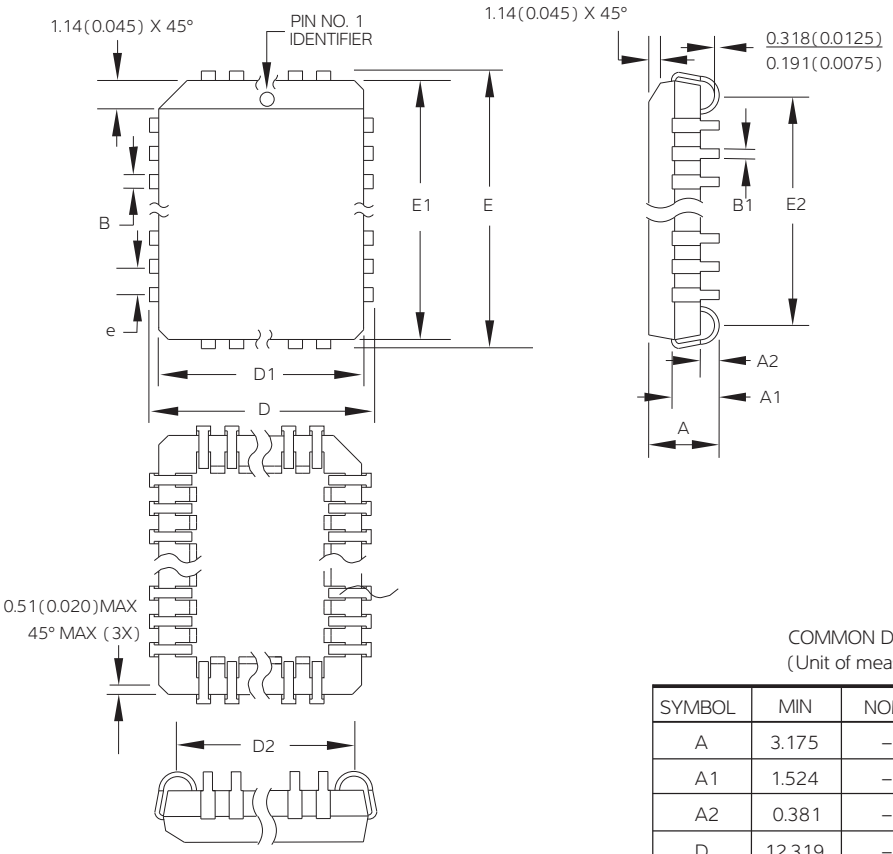
Green Package Option (Pb/Halide-free)

Atmel Ordering Code	Package	t_{ACC} (ns)	I_{CC} (mA)		Lead Finish	Operation Range
			Active	Standby		
AT27C040-70JU	32J	70	30	0.1	Matte Tin	Industrial (-40°C to 85°C)
AT27C040-70PU	32P6					
AT27C040-90JU	32J	90	30	0.1	Matte Tin	Industrial (-40°C to 85°C)
AT27C040-90PU	32P6					

Package Type	
32J	32-lead, plastic, J-leaded Chip Carrier (PLCC)
32P6	32-lead, 0.600" wide, plastic, Dual Inline (PDIP)

9. Package information

9.1 32J — 32-lead PLCC



COMMON DIMENSIONS
(Unit of measure = mm)

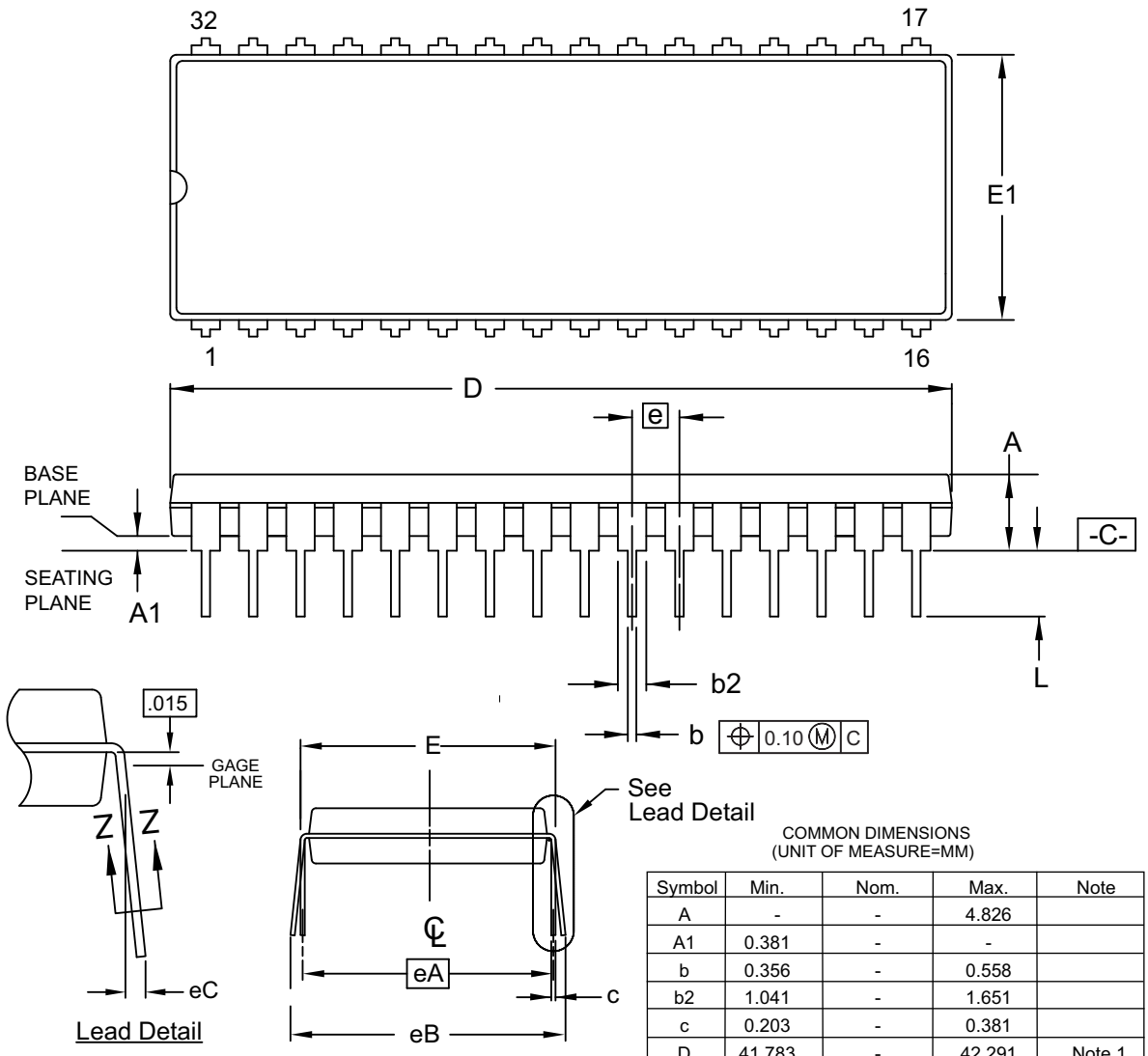
SYMBOL	MIN	NOM	MAX	NOTE
A	3.175	–	3.556	
A1	1.524	–	2.413	
A2	0.381	–	–	
D	12.319	–	12.573	
D1	11.354	–	11.506	Note 2
D2	9.906	–	10.922	
E	14.859	–	15.113	
E1	13.894	–	14.046	Note 2
E2	12.471	–	13.487	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-016, Variation AE.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.10mm) maximum.

10/04/01

Package Drawing Contact: packagedrawings@atmel.com	TITLE	DRAWING NO.	REV.
	32J, 32-lead, Plastic J-leaded Chip Carrier (PLCC)	32J	B

9.2 32P6 — 32-lead PDIP



COMMON DIMENSIONS
(UNIT OF MEASURE=MM)

Symbol	Min.	Nom.	Max.	Note
A	-	-	4.826	
A1	0.381	-	-	
b	0.356	-	0.558	
b2	1.041	-	1.651	
c	0.203	-	0.381	
D	41.783	-	42.291	Note 1
E	15.240	-	15.875	
E1	13.462	-	13.970	Note 1
L	3.048	-	3.556	
e	2.54 BSC			
eA	15.24 BSC			
eB	-	-	17.78	
eC	0.000	-	1.524	

Notes:
1. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

11/28/11

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** **32P6**, 32-lead, 0.600"/15.24 mm Wide Plastic Dual Inline Package (PDIP)	**GPC** PLU	**DRAWING NO.** 32P6	**REV.** C

10. Revision History

Doc. Rev.	Date	Comments
0189J	10/2012	Update 32P6 package outline drawing. Update template and Atmel logo.
0189I	04/2011	Remove TSOP package. Add lead finish to ordering information.
0189H	12/2007	Datasheet revision.

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