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8/08—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

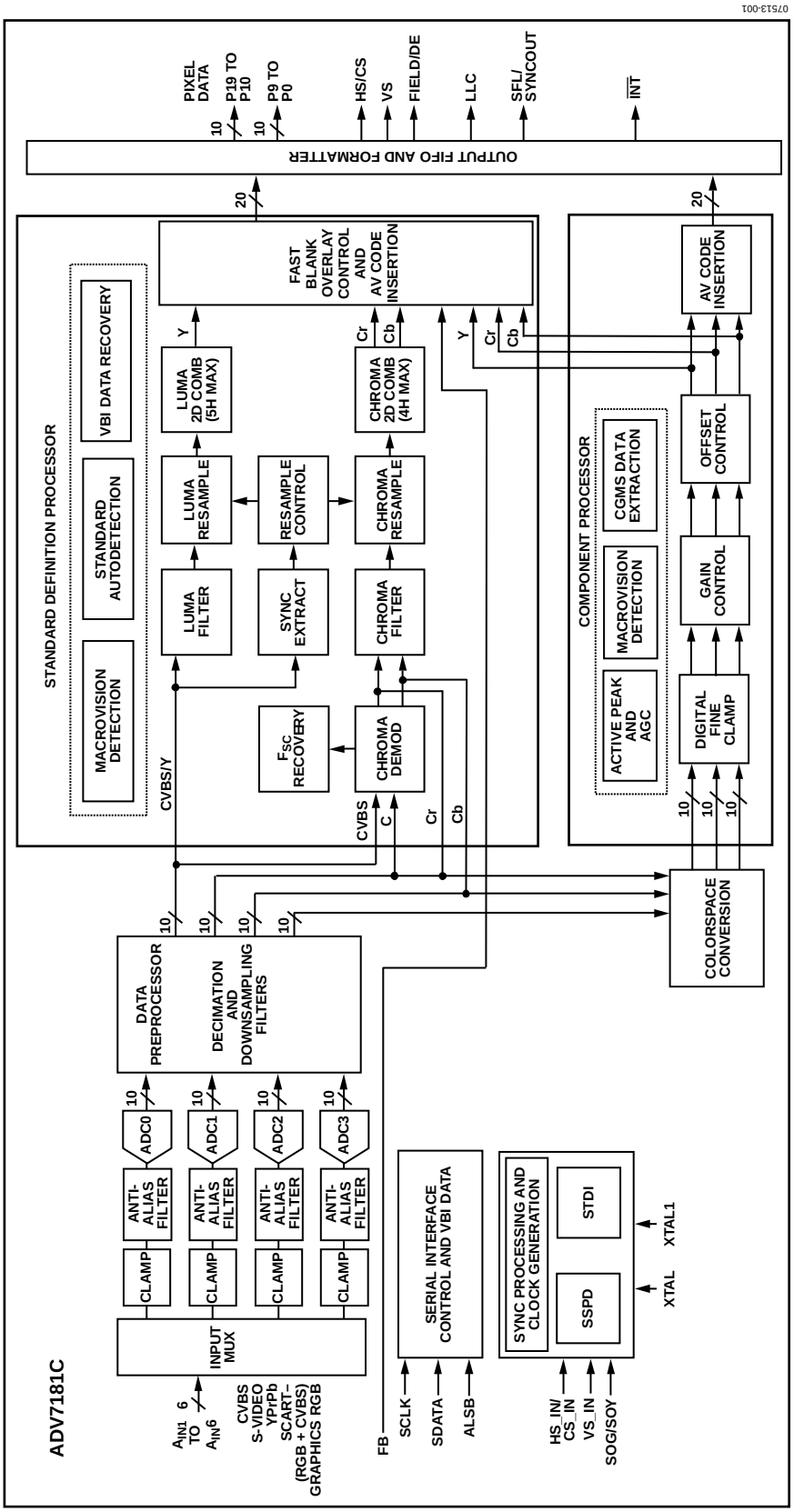


Figure 1.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

AVDD = 3.15 V to 3.45 V, DVDD = 1.65 V to 2.0 V, DVDDIO = 3.0 V to 3.6 V, PVDD = 1.71 V to 1.89 V, nominal input range 1.6 V. T_{MIN} to T_{MAX} = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter[1, 2]	Symbol	Test Conditions	Min	Typ	Max	Unit
STATIC PERFORMANCE[3, 4]						
Resolution (Each ADC)	N				10	Bits
Integral Nonlinearity	INL	BSL at 27 MHz (10-bit level)		±0.6	±2.5	LSB
		BSL at 54 MHz (10-bit level)		−0.6/+0.7		LSB
		BSL at 74 MHz (10-bit level)		±1.4		LSB
		BSL at 110 MHz (8-bit level)		±0.9		LSB
Differential Nonlinearity	DNL	At 27 MHz (10-bit level)		−0.2/+0.25	−0.99/+2.5	LSB
		At 54 MHz (10-bit level)		−0.2/+0.25		LSB
		At 74 MHz (10-bit level)		±0.9		LSB
		At 110 MHz (8-bit level)		−0.2/+1.5		LSB
DIGITAL INPUTS[5]						
Input High Voltage[6]	V_{IH}		2			V
		HS_IN, VS_IN low trigger mode	0.7			V
Input Low Voltage[7]	V_{IL}				0.8	V
		HS_IN, VS_IN low trigger mode			0.3	V
Input Current	I_{IN}		−10		+10	µA
Input Capacitance[5]	C_{IN}				10	pF
DIGITAL OUTPUTS						
Output High Voltage[8]	V_{OH}	I_{SOURCE} = 0.4 mA	2.4			V
Output Low Voltage[8]	V_{OL}	I_{SINK} = 3.2 mA			0.4	V
High Impedance Leakage Current	I_{LEAK}	Pin 1			60	µA
		All other output pins			10	µA
Output Capacitance[5]	C_{OUT}				20	pF
POWER REQUIREMENTS[5]						
Digital Core Power Supply	DVDD		1.65	1.8	2	V
Digital I/O Power Supply	DVDDIO		3.0	3.3	3.6	V
PLL Power Supply	PVDD		1.71	1.8	1.89	V
Analog Power Supply	AVDD		3.15	3.3	3.45	V
Digital Core Supply Current	IDVDD	CVBS input sampling at 54 MHz		105		mA
		Graphics RGB sampling at 75 MHz		90		mA
		SCART RGB FB sampling at 54 MHz		106		mA
Digital I/O Supply Current	IDVDDIO	CVBS input sampling at 54 MHz		4		mA
		Graphics RGB sampling at 75 MHz		38		mA
PLL Supply Current	IPVDD	CVBS input sampling at 54 MHz		11		mA
		Graphics RGB sampling at 75 MHz		12		mA
Analog Supply Current[9]	IAVDD	CVBS input sampling at 54 MHz		99		mA
		Graphics RGB sampling at 75 MHz		166		mA
		SCART RGB FB sampling at 54 MHz		200		mA
Power-Down Current	IPWRDN			2.25		mA
Green Mode Power-Down	IPWRDNG	Synchronization bypass function		16		mA
Power-Up Time	TPWRUP			20		ms

[1] The minimum/maximum specifications are guaranteed over this range.
[2] All specifications are obtained using the Analog Devices, Inc., recommended programming scripts.
[3] All ADC linearity tests performed at input range of full scale – 12.5%, and at zero scale + 12.5%.
[4] Maximum INL and DNL specifications obtained with part configured for component video input.
[5] Guaranteed by characterization.
[6] To obtain specified V_{IH} level on Pin 22, program Register 0x13 (WO) with a value of 0x04. If Register 0x13 is programmed with a value of 0x00, then V_{IH} on Pin 22 is 1.2 V.
[7] To obtain specified V_{IL} level on Pin 22, program Register 0x13 (WO) with a value of 0x04. If Register 0x13 is programmed with a value of 0x00, then V_{IL} on Pin 22 is 0.4 V.
[8] V_{OH} and V_{OL} levels obtained using default drive strength value (0xD5) in Register Subaddress 0xF4.
[9] For CVBS current measurement only, ADC0 is powered up. For RGB current measurements only, ADC0, ADC1, and ADC2 are powered up. For SCART FB current measurements, all ADCs are powered up.

VIDEO SPECIFICATIONS

AVDD = 3.15 V to 3.45 V, DVDD = 1.65 V to 2.0 V, DVDDIO = 3.0 V to 3.6 V, PVDD = 1.71 V to 1.89 V. T_{MIN} to T_{MAX} = −40°C to +85°C, unless otherwise noted.

Table 2.

Parameter[1, 2]	Symbol	Test Conditions	Min	Typ	Max	Unit
NONLINEAR SPECIFICATIONS						
Differential Phase	DP	CVBS input, modulated 5 step		0.5		Degrees
Differential Gain	DG	CVBS input, modulated 5 step		0.5		%
Luma Nonlinearity	LNL	CVBS input, 5 step		0.5		%
NOISE SPECIFICATIONS						
SNR Unweighted		Luma ramp	54	56		dB
SNR Unweighted		Luma flat field	58	60		dB
Analog Front-End Crosstalk				60		dB
LOCK TIME SPECIFICATIONS						
Horizontal Lock Range			−5		+5	%
Vertical Lock Range			40		70	Hz
f_{SC} Subcarrier Lock Range				±1.3		kHz
Color Lock in Time				60		Lines
Sync Depth Range[3]			20		200	%
Color Burst Range			5		200	%
Vertical Lock Time				2		Fields
Horizontal Lock Time				100		Lines
CHROMA SPECIFICATIONS						
Hue Accuracy	HUE			1		Degrees
Color Saturation Accuracy	CL_AC			1		%
Color AGC Range			5		400	%
Chroma Amplitude Error				0.5		%
Chroma Phase Error				0.4		Degrees
Chroma Luma Intermodulation				0.2		%
LUMA SPECIFICATIONS						
Luma Brightness Accuracy		CVBS, 1 V input		1		%
Luma Contrast Accuracy		CVBS, 1 V input		1		%

[1] The minimum/maximum specifications are guaranteed over this range.
[2] Guaranteed by characterization.
[3] Nominal synchronization depth is 300 mV at 100% synchronization depth range.

TIMING CHARACTERISTICS

AVDD = 3.15 V to 3.45 V, DVDD = 1.65 V to 2.0 V, DVDDIO = 3.0 V to 3.6 V, PVDD = 1.71 V to 1.89 V. T_{MIN} to T_{MAX} = −40°C to +85°C, unless otherwise noted.

Table 3.

Parameter[1, 2]	Symbol	Test Conditions	Min	Typ	Max	Unit
SYSTEM CLOCK AND CRYSTAL						
Crystal Nominal Frequency				28.63636		MHz
Crystal Frequency Stability					±50	ppm
Horizontal Sync Input Frequency			14.8		110	kHz
LLC Frequency Range			12.825		110	MHz
I^2C PORT[3]						
SCLK Frequency					400	kHz
SCLK Minimum Pulse Width High	t_1		0.6			µs
SCLK Minimum Pulse Width Low	t_2		1.3			µs
Hold Time (Start Condition)	t_3		0.6			µs
Setup Time (Start Condition)	t_4		0.6			µs
SDA Setup Time	t_5		100			ns
SCLK and SDA Rise Time	t_6				300	ns
SCLK and SDA Fall Time	t_7				300	ns
Setup Time for Stop Condition	t_8			0.6		µs
RESET FEATURE						
Reset Pulse Width			5			ms
CLOCK OUTPUTS						
LLC Mark Space Ratio	t_9:t_{10}		45:55		55:45	% duty cycle
DATA AND CONTROL OUTPUTS						
Data Output Transition Time SDR (SDP)[4]	t_{11}	Negative clock edge to start of valid data			3.6	ns
Data Output Transition Time SDR (SDP)[4]	t_{12}	End of valid data to negative clock edge			2.4	ns
Data Output Transition Time SDR (CP)[5]	t_{13}	End of valid data to negative clock edge			2.8	ns
Data Output Transition Time SDR (CP)[5]	t_{14}	Negative clock edge to start of valid data			0.1	ns
Data Output Transition Time DDR (CP)[5, 6]	t_{15}	Positive clock edge to end of valid data	1.9			ns
Data Output Transition Time DDR (CP)[5, 6]	t_{16}	Start of valid data to positive clock edge	1.7			ns
Data Output Transition Time DDR (CP)[5, 6]	t_{17}	Negative clock edge to end of valid data	1.4			ns
Data Output Transition Time DDR (CP)[5, 6]	t_{18}	Start of valid data to negative clock edge	1.7			ns

[1] The minimum/maximum specifications are guaranteed over this range.
[2] Guaranteed by characterization.
[3] TTL input values are 0 V to 3 V, with rise/fall times of ≤3 ns, measured between the 10% and 90% points.
[4] SDP timing figures obtained using default drive strength value (0xD5) in Register Subaddress 0xF4.
[5] CP timing figures obtained using maximum drive strength value (0x3F) in Register Subaddress 0xF4.
[6] Guaranteed by characterization up to 75 MHz pixel clock.

Timing Diagrams

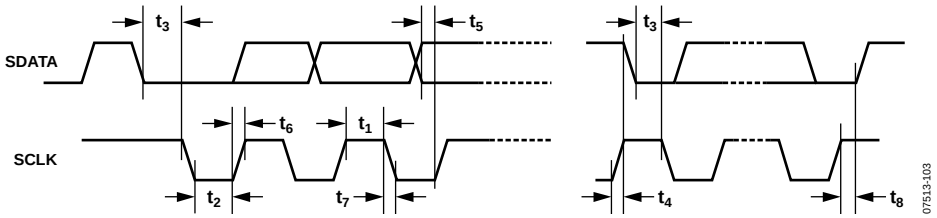


Figure 2. I²C Timing

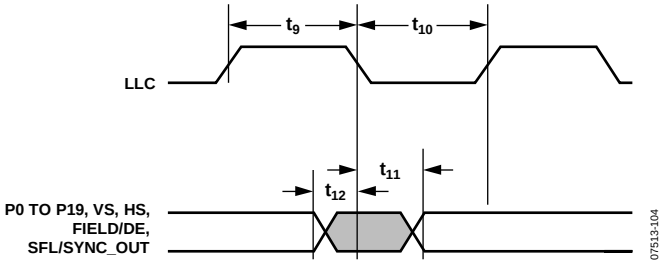


Figure 3. Pixel Port and Control SDR Output Timing (SD Core)

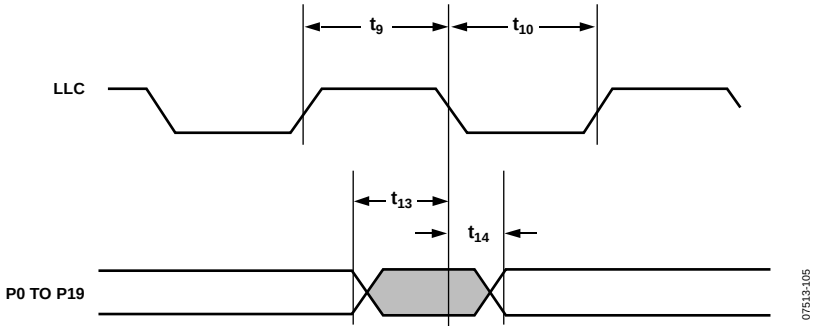


Figure 4. Pixel Port and Control SDR Output Timing (CP Core)

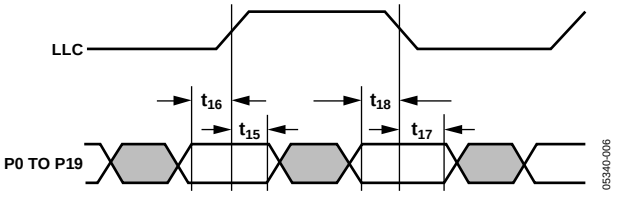


Figure 5. Pixel Port and Control DDR Output Timing (CP Core)

ANALOG SPECIFICATIONS

AVDD = 3.15 V to 3.45 V, DVDD = 1.65 V to 2.0 V, DVDDIO = 3.0 V to 3.6 V, PVDD = 1.71 V to 1.89 V. T_{MIN} to T_{MAX} = −40°C to +85°C, unless otherwise noted. Recommended analog input video signal range: 0.5 V to 1.6 V, typically 1 V p-p.

Table 4.

Parameter[1, 2]	Test Conditions	Min	Typ	Max	Unit
CLAMP CIRCUITRY					
External Clamp Capacitor			0.1		µF
Input Impedance; Except Pin 34 (FB)	Clamps switched off		10		MΩ
Input Impedance of Pin 34 (FB)			20		kΩ
CML			1.86		V
ADC Full-Scale Level			CML + 0.8		V
ADC Zero-Scale level			CML – 0.8		V
ADC Dynamic Range			1.6		V
Clamp Level (When Locked)	CVBS input		CML – 0.292		V
	SCART RGB input (R, G, B signals)		CML – 0.4		V
	S-Video input (Y signal)		CML – 0.292		V
	S-Video input (C signal)		CML – 0		V
	Component input (Y, Pr, Pb signals)		CML – 0.3		V
	PC RGB input (R, G, B signals)		CML – 0.3		V
Large Clamp Source Current	SDP only		0.75		mA
Large Clamp Sink Current	SDP only		0.9		mA
Fine Clamp Source Current	SDP only		17		µA
Fine Clamp Sink Current	SDP only		17		µA

[1] The minimum/maximum specifications are guaranteed over this range.
[2] Guaranteed by characterization.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
AVDD to AGND	4 V
DVDD to DGND	2.2 V
PVDD to AGND	2.2 V
DVDDIO to DGND	4 V
DVDDIO to AVDD	−0.3 V to +0.3 V
PVDD to DVDD	−0.3 V to +0.3 V
DVDDIO to PVDD	−0.3 V to +2 V
DVDDIO to DVDD	−0.3 V to +2 V
AVDD to PVDD	−0.3 V to +2 V
AVDD to DVDD	−0.3 V to +2 V
Digital Inputs Voltage to DGND	DGND − 0.3 V to DVDDIO + 0.3 V
Digital Outputs Voltage to DGND	DGND − 0.3 V to DVDDIO + 0.3 V
Analog Inputs to AGND	AGND − 0.3 V to AVDD + 0.3 V
Operating Temperature Range	−40°C to +85°C
Maximum Junction Temperature ($T_{J\ MAX}$)	125°C
Storage Temperature Range	−65°C to +150°C
Infrared Reflow, Soldering (20 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL PERFORMANCE

To reduce power consumption when using the part, turn off any unused ADCs.

It is imperative that the recommended scripts be used for the following high current modes: SCART, 720p, 1080i, and all RGB graphic standards. Using the recommended scripts ensures correct thermal performance. These scripts are available from a local FAE.

The junction temperature must always stay below the maximum junction temperature ($T_{J\ MAX}$) of 125°C. The junction temperature can be calculated by

$$T_J = T_{A\ MAX} + (\theta_{JA} \times W_{MAX})$$

where:

$T_{A\ MAX}$ = 85°C.

θ_{JA} = 45.5°C/W.

W_{MAX} = ((AVDD × IAVDD) + (DVDD × IDVDD) + (DVDDIO × IDVDDIO) + (PVDD × IPVDD)).

THERMAL SPECIFICATIONS

Table 6.

Parameter	Test Conditions	Value
Junction-to-Case Thermal Resistance, θ_{JC}	4-layer PCB with solid ground plane	9.2°C/W typical
Junction-to-Ambient Thermal Resistance, θ_{JA}	4-layer PCB with solid ground plane (still air)	45.5°C/W typical

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

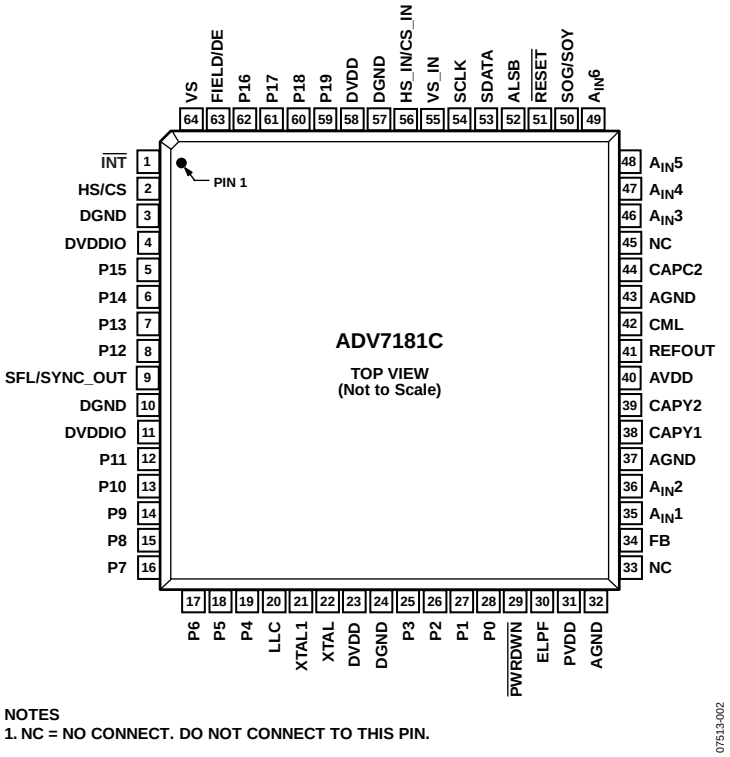


Figure 6. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	$\overline{\text{INT}}$	O	Interrupt. This pin can be active low or active high. When SDP/CP status bits change, this pin is triggered. The set of events that triggers an interrupt is under user control.
2	HS/CS	O	HS: Horizontal Synchronization Output Signal (SDP and CP Modes). CS: Digital Composite Synchronization Signal (CP Mode).
3, 10, 24, 57	DGND	G	Digital Ground.
4, 11	DVDDIO	P	Digital I/O Supply Voltage (3.3 V).
28 to 25, 19 to 12, 8 to 5, 62 to 59	P0 to P19	O	Video Pixel Output Port. Refer to Table 10 for output configuration modes.
9	SFL/SYNC_OUT	O	SFL: Subcarrier Frequency Lock. This pin contains a serial output stream that can be used to lock the subcarrier frequency when this decoder is connected to any Analog Devices digital video encoder. SYNC_OUT: Sliced Synchronization Output Signal Available Only in CP Mode.
20	LLC	O	Line-Locked Output Clock. This pin is for the pixel data (the range is 12.825 MHz to 110 MHz).
21	XTAL1	O	This pin should be connected to the 28.63636 MHz crystal or left as a no connect if an external 3.3 V, 28.63636 MHz clock oscillator source is used to clock the ADV7181C. In crystal mode, the crystal must be a fundamental crystal.
22	XTAL	I	Input pin for 28.63636 MHz crystal, or can be overdriven by an external 3.3 V, 28.63636 MHz clock oscillator source to clock the ADV7181C.
23, 58	DVDD	P	Digital Core Supply Voltage (1.8 V).
29	$\overline{\text{PWRDWN}}$	I	A Logic 0 on this pin places the ADV7181C in a power-down mode.
30	ELPF	O	The recommended external loop filter must be connected to this ELPF pin.
31	PVDD	P	PLL Supply Voltage (1.8 V).
32, 37, 43	AGND	G	Analog Ground.

Pin No.	Mnemonic	Type[1]	Description
33, 45	NC		No Connect. These pins are not connected internally.
34	FB	I	Fast Switch Overlay Input. This pin switches between CVBS and RGB analog signals.
35, 36, 46, 47, 48, 49	$A_{IN}1$ to $A_{IN}6$	I	Analog Video Input Channels.
38, 39	CAPY1, CAPY2	I	ADC Capacitor Network. See Figure 9 for a recommended capacitor network for this pin.
40	AVDD	P	Analog Supply Voltage (3.3 V).
41	REFOUT	O	Internal Voltage Reference Output. See Figure 9 for a recommended capacitor network for this pin.
42	CML	O	Common-Mode Level Pin (CML) for the Internal ADCs. See Figure 9 for a recommended capacitor network for this pin.
44	CAPC2	I	ADC Capacitor Network. See Figure 9 for a recommended capacitor network for this pin.
50	SOG/SOY	I	Sync on Green/Sync on Luma Input. Used in embedded synchronization mode.
51	$\overline{\text{RESET}}$	I	System Reset Input, Active Low. A minimum low reset pulse width of 5 ms is required to reset the ADV7181C circuitry.
52	ALSB	I	This pin selects the I^2C address for the ADV7181C control and VBI readback ports. ALSB set to Logic 0 sets the address for a write to Control Port 0x40 and the readback address for VBI Port 0x21. ALSB set to a Logic 1 sets the address for a write to Control Port 0x42 and the readback address for VBI Port 0x23.
53	SDATA	I/O	I^2C Port Serial Data Input/Output Pin.
54	SCLK	I	I^2C Port Serial Clock Input. Maximum clock rate of 400 kHz.
55	VS_IN	I	VS Input Signal. Used in CP mode for 5-wire timing mode.
56	HS_IN/CS_IN	I	This pin can be configured in CP mode to be either a digital HS input signal or a digital CS input signal used to extract timing in a 5-wire or 4-wire RGB mode.
63	FIELD/DE	O	Field Synchronization Output Signal (All Interlaced Video Modes). This pin also can be enabled as a data enable signal (DE) in CP mode to allow direct connection to a HDMI/DVI Tx IC.
64	VS	O	Vertical Synchronization Output Signal (SDP and CP Modes).

[1] G = ground, I = input, O = output, I/O = input/output, and P = power.

DETAILED FUNCTIONALITY

ANALOG FRONT END

The analog front-end section contains four high quality 10-bit ADCs, and the six analog input channel mux enables multisource connection without the requirement of an external mux. It also contains

- Four current and voltage clamp control loops to ensure that any dc offsets are removed from the video signal
- SCART functionality and SD RGB overlay on CVBS that are controlled by fast blank input
- Four internal antialias filters to remove out-of-band noise on standard definition input video signals

SDP PIXEL DATA OUTPUT MODES

The SDP pixel data output modes are the following:

- 8-/10-bit ITU-R BT.656 4:2:2 YCrCb with embedded time codes and/or HS, VS, and FIELD
- 16-/20-bit YCrCb with embedded time codes and/or HS, VS, and FIELD

CP PIXEL DATA OUTPUT MODES

CP pixel data output modes include single data rate (SDR) and double data rate (DDR) as follows:

- SDR 8-/10-bit 4:2:2 YCrCb for 525i, 625i
- SDR 16-/20-bit 4:2:2 YCrCb for all standards
- DDR 8-/10-bit 4:2:2 YCrCb for all standards
- DDR 12-bit 4:4:4 RGB for graphics inputs

COMPOSITE AND S-VIDEO PROCESSING

Composite and S-Video processing features offer support for NTSC M/J, NTSC 4.43, PAL B/D/I/G/H, PAL60, PAL M, PAL N, and SECAM (B, D, G, K, and L) standards in the form of CVBS and S-Video as well as super-adaptive, 2D, 5-line comb filters for NTSC and PAL give superior chrominance and luminance separation for composite video. They also include full automatic detection and autoswitching of all worldwide standards (PAL, NTSC, and SECAM) and automatic gain control with white peak mode to ensure the video is always processed without loss of the video processing range. Other features are

- Adaptive Digital Line Length Tracking (ADLLT™)
- Proprietary architecture for locking to weak, noisy, and unstable sources from VCRs and tuners
- IF filter block to compensate for high frequency luma attenuation due to tuner SAW filter
- Chroma transient improvement (CTI)
- Luminance digital noise reduction (DNR)
- Color controls including hue, brightness, saturation, contrast, and Cr and Cb offset controls
- Certified Macrovision® copy protection detection on composite and S-Video for all worldwide formats (PAL/NTSC/SECAM)
- 4× oversampling (54 MHz) for CVBS, S-Video, and YUV modes
- Line-locked clock output (LLC)
- Letterbox detection support
- Free-run output mode to provide stable timing when no video input is present
- Vertical blanking interval data processor, including teletext, video programming system (VPS), vertical interval time codes (VITC), closed captioning (CC) and extended data service (EDS), wide screen signaling (WSS), copy generation management system (CGMS), and compatibility with GemStar™ 1×/2× electronic program guide
- Clocked from a single 28.63636 MHz crystal
- Subcarrier frequency lock (SFL) output for downstream video encoder
- Differential gain typically 0.5%
- Differential phase typically 0.5°

COMPONENT VIDEO PROCESSING

Component video processing supports formats including 525i, 625i, 525p, 625p, 720p, 1080i, and many other HDTV formats, as well as automatic adjustments that include gain (contrast) and offset (brightness), and manual adjustment controls. Other features supported by component video processing are

- Analog component YPrPb/RGB video formats with embedded synchronization or with separate HS, VS, or CS
- Color space conversion matrix to support YCrCb-to-DDR RGB and RGB-to-YCrCb conversions
- Standard identification (STDI) enables system level component format detection
- Synchronization source polarity detector (SSPD) to determine the source and polarity of the synchronization signals that accompany the input video
- Certified Macrovision copy protection detection on component formats (525i, 625i, 525p, and 625p)
- Free-run output mode to provide stable timing when no video input is present
- Arbitrary pixel sampling support for nonstandard video sources

RGB GRAPHICS PROCESSING

RGB graphics processing offers a 110 MSPS conversion rate that supports RGB input resolutions up to 1024 × 768 at 70 Hz (XGA), automatic or manual clamp and gain controls for graphics modes, and contrast and brightness controls. Other features include

- 32-phase DLL to allow optimum pixel clock sampling
- Automatic detection of synchronization source and polarity by SSPD block
- Standard identification enabled by the STDI block
- RGB that can be color space converted to YCrCb and decimated to a 4:2:2 format for video centric back-end IC interfacing
- Data enable (DE) output signal supplied for direct connection to HDMI/DVI Tx IC
- Arbitrary pixel sampling support for nonstandard video sources
- RGB graphics supported on 12-bit DDR format

GENERAL FEATURES

General features of the ADV7181C include HS/CS, VS, and FIELD/DE output signals with programmable position, polarity, and width as well as a programmable interrupt request output pin, $\overline{\text{INT}}$, that signals SDP/CP status changes. Other features are

- Low power consumption: 1.8 V digital core, 3.3 V analog and digital I/O, low power, power-down mode, and green PC mode
- Industrial temperature range of −40°C to +85°C
- 64-lead, 10 mm × 10 mm, Pb-free LQFP
- 3.3 V ADCs giving enhanced dynamic range and performance

DETAILED DESCRIPTION

ANALOG FRONT END

The ADV7181C analog front end comprises four 10-bit ADCs that digitize the analog video signal before applying it to the SDP or CP. The analog front end uses differential channels to each ADC to ensure high performance in a mixed-signal application.

The front end also includes a 6-channel input mux that enables multiple video signals to be applied to the ADV7181C. Current and voltage clamps are positioned in front of each ADC to ensure that the video signal remains within the range of the converter. Fine clamping of the video signals is performed downstream by digital fine clamping in either the CP or SDP.

Optional antialiasing filters are positioned in front of each ADC. These filters can be used to band-limit standard definition video signals, removing spurious out-of-band noise.

The ADCs are configured to run in 4× oversampling mode when decoding composite and S-Video inputs; 2× oversampling is performed for component 525i, 625i, 525p, and 625p sources. All other video standards are 1× oversampled. Oversampling the video signals reduces the cost and complexity of external antialiasing filters with the benefit of an increased signal-to-noise ratio (SNR).

The ADV7181C can support simultaneous processing of CVBS and RGB standard definition signals to enable SCART compatibility and overlay functionality. A combination of CVBS and RGB inputs can be mixed and output under the control of the I^2C registers and the fast blank pin.

STANDARD DEFINITION PROCESSOR (SDP)

The SDP section is capable of decoding a large selection of baseband video signals in composite, S-Video, and YUV formats. The video standards supported by the SDP include PAL B/D/I/G/H, PAL60, PAL M, PAL N, NTSC M/J, NTSC 4.43, and SECAM B/D/G/K/L. The ADV7181C automatically detects the video standard and processes it accordingly.

The SDP has a 5-line super adaptive 2D comb filter that gives superior chrominance and luminance separation when decoding a composite video signal. This highly adaptive filter automatically adjusts its processing mode according to video standards and signal quality with no user intervention required. The SDP has an IF filter block that compensates for attenuation in the high frequency luma spectrum due to the tuner SAW filter.

The SDP has specific luminance and chrominance parameter control for brightness, contrast, saturation, and hue.

The ADV7181C implements a patented ADLLT algorithm to track varying video line lengths from sources such as a VCR. ADLLT enables the ADV7181C to track and decode poor quality video sources such as VCRs, noisy sources from tuner outputs, VCD players, and camcorders. The SDP also contains a chroma transient improvement (CTI) processor. This processor increases the edge rate on chroma transitions, resulting in a sharper video image.

The SDP can process a variety of VBI data services, such as teletext, closed captioning (CC), wide screen signaling (WSS), video programming system (VPS), vertical interval time codes (VITC), copy generation management system (CGMS), GemStar 1×/2×, and extended data service (XDS). The ADV7181C SDP section has a Macrovision 7.1 detection circuit that allows it to detect Type I, Type II, and Type III protection levels. The decoder is also fully robust to all Macrovision signal inputs.

COMPONENT PROCESSOR (CP)

The CP section is capable of decoding/digitizing a wide range of component video formats in any color space. Component video standards supported by the CP are 525i, 625i, 525p, 625p, 720p, 1080i, graphics up to XGA at 70 Hz, and many other standards.

The CP section of the ADV7181C contains an AGC block. When no embedded synchronization is present, the video gain can be set manually. The AGC section is followed by a digital clamp circuit that ensures the video signal is clamped to the correct blanking level. Automatic adjustments within the CP include gain (contrast) and offset (brightness); manual adjustment controls are also supported.

A fixed mode graphics RGB to component output is available.

A color space conversion matrix is placed between the analog front end and the CP section. This enables YPrPb-to-DDR RGB and RGB-to-YCrCb conversions. Many other standards of color space can be implemented using the color space converter.

The output section of the CP is highly flexible. It can be configured in SDR mode with one data packet per clock cycle or in a DDR mode where data is presented on the rising and falling edges of the clock. In SDR mode, a 20-bit 4:2:2 is possible. In these modes, HS/CS, VS, and FIELD/DE (where applicable) timing reference signals are provided. In DDR mode, the ADV7181C can be configured in an 8-bit 4:2:2 YCrCb or 12-bit 4:4:4 RGB pixel output interface with corresponding timing signals.

The CP section contains circuitry to enable the detection of Macrovision encoded YPrPb signals for 525i, 625i, 525p, and 625p. It is designed to be fully robust when decoding these types of signals.

VBI extraction of component data is performed by the CP section of the ADV7181C for interlaced, progressive, and high definition scanning rates. The data extracted can be read back over the I^2C interface.

ANALOG INPUT MUXING

The ADV7181C has an integrated analog muxing section that allows more than one source of video signal to be connected to the decoder. Figure 7 outlines the overall structure of the input muxing provided in the ADV7181C.

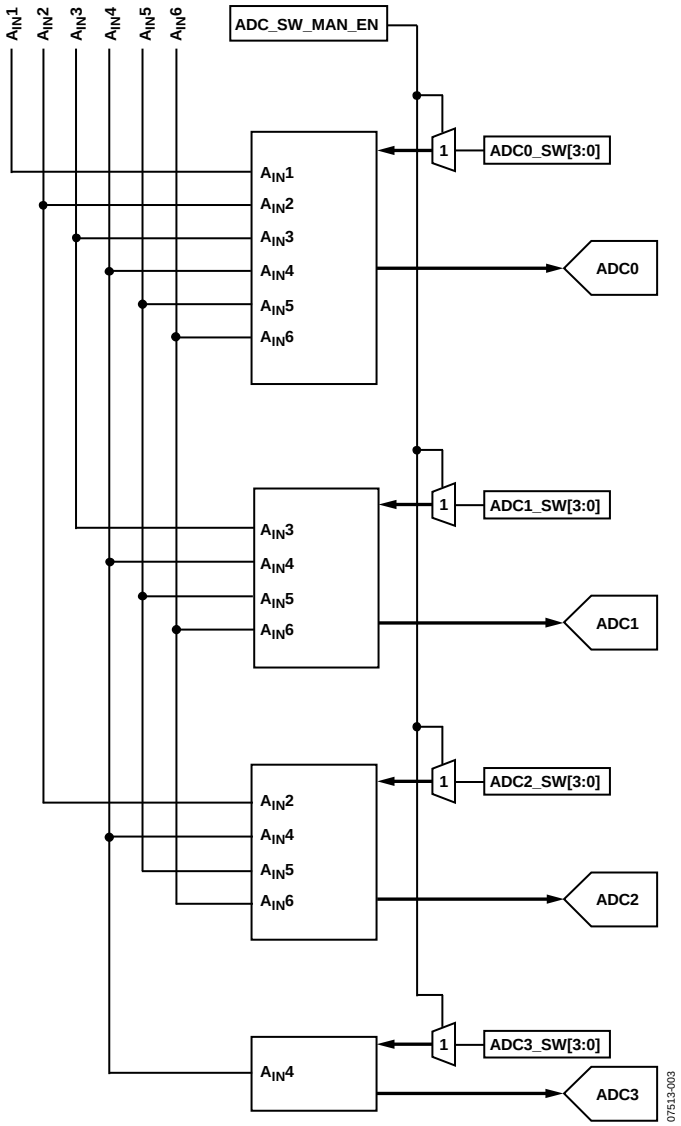


Figure 7. Internal Pin Connections

On the ADV7181C, it is recommended to use the ADC mapping shown in Table 8.

Table 8. Recommended ADC Mapping

Mode	Required ADC Mapping	AIN Channel	Core	Configuration[1]
CVBS	ADC0	CVBS = $A_{IN}1$	SD	INSEL[3:0] = 0000 SDM_SEL[1:0] = 00 PRIM_MODE[3:0] = 0000 VID_STD[3:0] = 0010
YC/YC auto	Y = ADC0 C = ADC1	Y = $A_{IN}2$ C = $A_{IN}3$	SD	INSEL[3:0] = 0000 SDM_SEL[1:0] = 11 PRIM_MODE[3:0] = 0000 VID_STD[3:0] = 0010
Component YUV	Y = ADC0 U = ADC2 V = ADC1	Y = $A_{IN}6$ U = $A_{IN}4$ V = $A_{IN}5$	SD	INSEL[3:0] = 1001 SDM_SEL[1:0] = 00 PRIM_MODE[3:0] = 0000 VID_STD[3:0] = 0010
Component YUV	Y = ADC0 U = ADC2 V = ADC1	Y = $A_{IN}6$ U = $A_{IN}4$ V = $A_{IN}5$	CP	INSEL[3:0] = 0000 SDM_SEL[1:0] = 00 PRIM_MODE[3:0] = 0000 VID_STD[3:0] = 1010
SCART RGB	CBVS = ADC0 G = ADC1 B = ADC3 R = ADC2	CVBS = $A_{IN}2$ G = $A_{IN}6$ B = $A_{IN}4$ R = $A_{IN}5$	SD	INSEL[3:0] = 0000 SDM_SEL[1:0] = 00 PRIM_MODE[3:0] = 0000 VID_STD[3:0] = 0010
Graphics RGB Mode	G = ADC0 B = ADC2 R = ADC1	G = $A_{IN}6$ B = $A_{IN}4$ R = $A_{IN}5$	CP	INSEL[3:0] = 0000 SDM_SEL[1:0] = 00 PRIM_MODE[3:0] = 0001 VID_STD[3:0] = 1100

[1] Configuration to format follow-on blocks in correct format.

Table 9. Manual MUX Settings for All ADCs

ADC_SWITCH_MAN to 1							
ADC0_SW_SEL[3:0]	ADC0 Connection	ADC1_SW_SEL[3:0]	ADC1 Connection	ADC2_SW_SEL[3:0]	ADC2 Connection	ADC3_SW_SEL[3:0]	ADC3 Connection
0001	$A_{IN}1$	0001	N/A	0001	N/A	0001	N/A
0010	$A_{IN}2$	0010	N/A	0010	$A_{IN}2$	0010	N/A
0100	$A_{IN}4$	0100	$A_{IN}4$	0100	$A_{IN}4$	0100	$A_{IN}4$
0101	$A_{IN}5$	0101	$A_{IN}5$	0101	$A_{IN}5$	0101	N/A
0110	$A_{IN}6$	0110	$A_{IN}6$	0110	$A_{IN}6$	0110	N/A
1100	$A_{IN}3$	1100	$A_{IN}3$	1100	N/A	1100	N/A

The analog input muxes of the ADV7181C must be controlled directly. This is referred to as manual input muxing. The manual muxing is activated by setting the ADC_SWITCH_MAN bit (see Table 9). It affects only the analog switches in front of the ADCs. INSEL, SDM_SEL, PRIM_MODE, and VID_STD still have to be set so that the follow-on blocks process the video data in the correct format.

Not every input pin can be routed to any ADC. There are restrictions in the channel routing imposed by the analog signal routing inside the IC. See Table 9 for an overview of the routing capabilities inside the chip. The four mux sections can be controlled by the reserved control signal buses ADC0_SW[3:0]/ADC1_SW[3:0]/ADC2_SW[3:0]/ADC3_SW[3:0].

Table 9 explains the ADC mapping configuration for the following:

- ADC_SW_MAN_EN, manual input muxing enable, IO map, Address C4[7]
- ADC0_SW[3:0], ADC0 mux configuration, IO map, Address C3[3:0]
- ADC1_SW[3:0], ADC1 mux configuration, IO map, Address C3[7:4]
- ADC2_SW[3:0], ADC2 mux configuration, IO map, Address C4[3:0]
- ADC3_SW[3:0], ADC3 mux configuration, IO map, Address F3[7:4]

PIXEL OUTPUT FORMATTING

Table 10. Pixel Output Formats

Processor, Format, and Mode		Pixel Port Pins P[19:0]																			
		19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDP	Video output 8-bit 4:2:2	YCrCb[7:0]																			
SDP	Video output 10-bit 4:2:2	YCrCb[9:0]																			
SDP	Video output 16-bit 4:2:2	Y[7:0]										CrCb[7:0]									
SDP	Video output 20-bit 4:2:2	Y[9:0]										CrCb[7:0]									
CP	Video output 12-bit 4:4:4 RGB DDR	D7[1] B[7]↑ R[3]↓	D6[1] B[6]↑ R[2]↓	D5[1] B[5]↑ R[1]↓	D4[1] B[4]↑ R[0]↓	D3[1] B[3]↑ G[7]↓	D2[1] B[2]↑ G[6]↓	D1[1] B[1]↑ G[5]↓	D0[1] B[0]↑ G[4]↓			D11[1] G[3]↑ R[7]↓	D10[1] G[2]↑ R[6]↓	D9[1] G[1]↑ R[5]↓	D8[1] G[0]↑ R[4]↓						
CP	Video output 16-bit 4:2:2	CHA[7:0] (for example, Y[7:0])										CHB/C[7:0] (for example, Cr/Cb[7:0])									
CP	Video output 20-bit 4:2:2	CHA[9:0] (for example, Y[9:0])										CHB/C[9:0] (for example, Cr/Cb[9:0])									

[1] ↑ indicates data clocked on the rising edge of LLC, ↓ indicates data clocked on the falling edge of LLC.

RECOMMENDED EXTERNAL LOOP FILTER COMPONENTS

The external loop filter components for the ELPF pin should be placed as close as possible to the respective pins. Figure 8 shows the recommended component values.

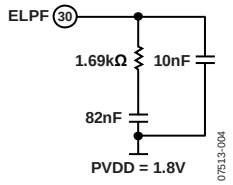


Figure 8. ELPF Components

TYPICAL CONNECTION DIAGRAM

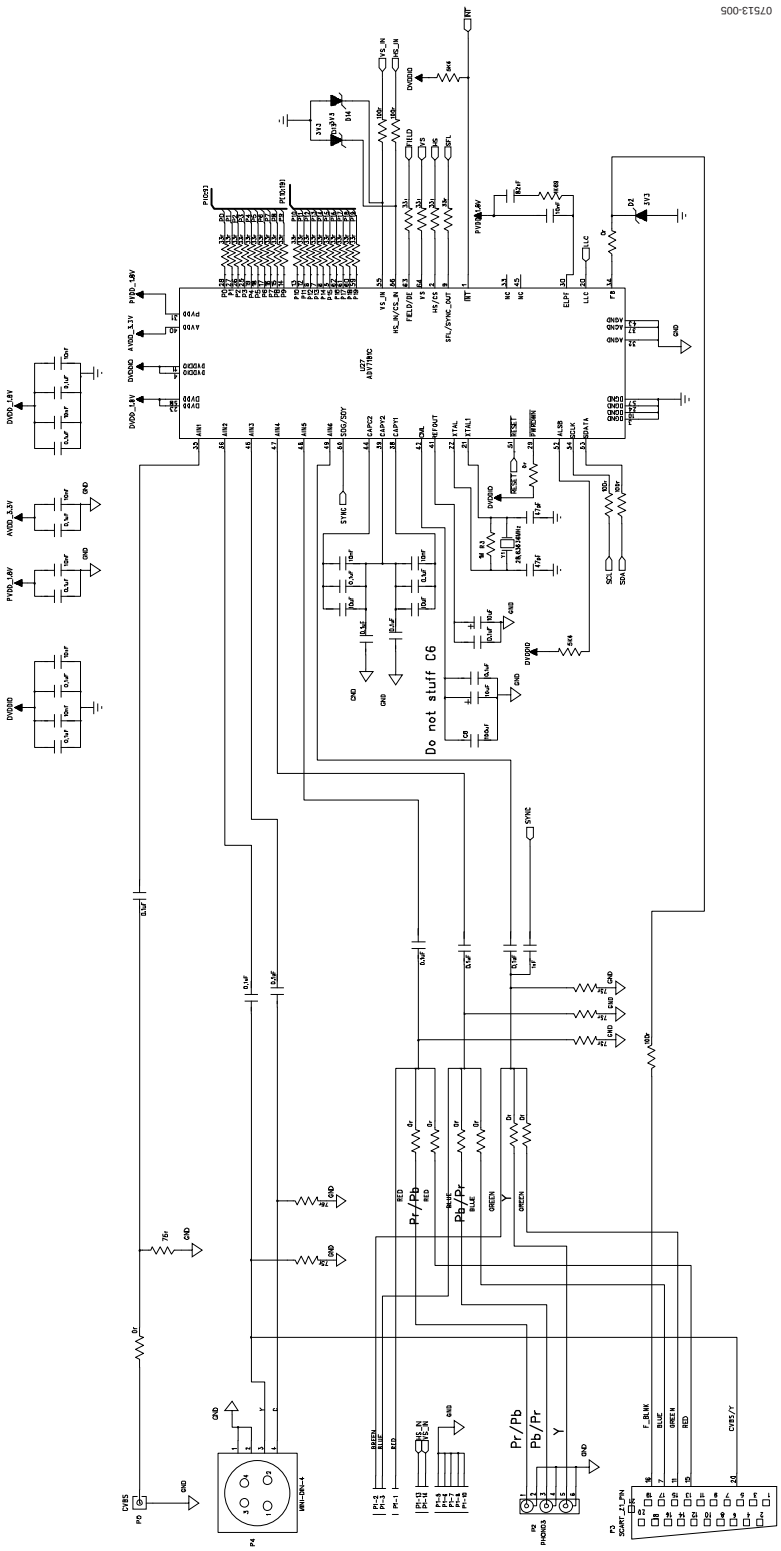
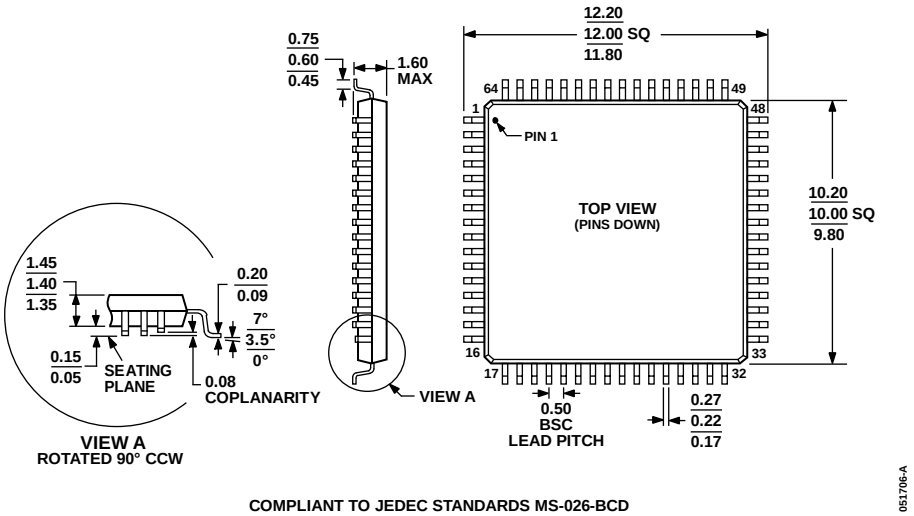


Figure 9. Typical Connection

For the latest software configuration files, visit the ADV7181C Design Support Files web page on the EngineerZone video forum.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BCD

Figure 10. 64-Lead Low Profile Quad Flat Package [LQFP]
(ST-64-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADV7181CBSTZ	−40°C to +85°C	64-Lead LQFP	ST-64-2
ADV7181CBSTZ-REEL	−40°C to +85°C	64-Lead LQFP	ST-64-2
ADV7181CWBSTZ	−40°C to +85°C	64-Lead LQFP	ST-64-2
ADV7181CWBSTZ-REEL	−40°C to +85°C	64-Lead LQFP	ST-64-2
EVAL-ADV7181CLQEBZ		Evaluation Board for the LQFP	

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADV7181CW models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

D07513-0-8/12(E)