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REVISION HISTORY

10/08—Rev. 0 to Rev. A

Changes to Theory of Operation Section and Output (OUT)	
Section.....	10
Changes to Ordering Guide	11

7/06—Revision 0: Initial Version

SPECIFICATIONS

$V_{RS+} = 2\text{ V to } 28\text{ V}$, $V_{SENSE} = (V_{RS+} - V_{RS-}) = 0\text{ V}$, $V_{CC} = 3\text{ V to } 28\text{ V}$, $T_A = -40^\circ\text{C to } +125^\circ\text{C}$, unless otherwise noted. Typical values are at $T_A = 25^\circ\text{C}$.¹

Table 1.

Parameter	Min	Typ	Max	Unit	Conditions
POWER SUPPLY					
Operating Voltage Range, V_{CC}	3		28	V	Inferred from PSRR test
Common-Mode Input Range, V_{CMR}	2		28	V	Inferred OUT voltage error test
Common-Mode Input Rejection, CMR		90		dB	$V_{SENSE} = 100\text{ mV}$, $V_{CC} = 12\text{ V}$
Supply Current, I_{CC}		0.5	1.2	mA	$V_{CC} = 28\text{ V}$
Leakage Current, I_{RS+}/I_{RS-}		0.05	2	μA	$V_{CC} = 0\text{ V}$, $V_{RS+} = 28\text{ V}$, $T_A = 85^\circ\text{C}$
Input Bias Current, I_{RS+}		20	60	μA	
Input Bias Current, I_{RS-}		40	120	μA	
Full-Scale Sense Voltage, V_{SENSE}		150		mV	$V_{SENSE} = (V_{RS+} - V_{RS-})$
Total Output Voltage Error ²		± 1		%	$V_{SENSE} = 100\text{ mV}$, $V_{CC} = 12\text{ V}$, $V_{RS+} = 2\text{ V}$
		± 1.0	± 5.0	%	$V_{SENSE} = 100\text{ mV}$, $V_{CC} = 12\text{ V}$, $V_{RS+} = 12\text{ V}$, $T_A = +25^\circ\text{C}$
			± 5.0	%	$V_{SENSE} = 100\text{ mV}$, $V_{CC} = 12\text{ V}$, $V_{RS+} = 12\text{ V}$, $T_A = -40^\circ\text{C to } +125^\circ\text{C}$
		± 1.0	± 5.0	%	$V_{SENSE} = 100\text{ mV}$, $V_{CC} = 28\text{ V}$, $V_{RS+} = 28\text{ V}$, $T_A = +25^\circ\text{C}$
			± 5.0	%	$V_{SENSE} = 100\text{ mV}$, $V_{CC} = 28\text{ V}$, $V_{RS+} = 28\text{ V}$, $T_A = -40^\circ\text{C to } +125^\circ\text{C}$
		± 7.5		%	$V_{SENSE} = 6.25\text{ mV}$, ³ $V_{CC} = 12\text{ V}$, $V_{RS+} = 12\text{ V}$
		1.0		mV	$V_{CC} = V_{RS+} = 12\text{ V}$, $V_{SENSE} > 10\text{ mV}$
Extrapolated Input Offset Voltage, V_{OS}		0.8	1.2	V	$V_{CC} = 3\text{ V}$, $V_{SENSE} = 150\text{ mV}$ (ADM4073T)
Output High Voltage ($V_{CC} - V_{OH}$)		0.8	1.2	V	$V_{CC} = 7.5\text{ V}$, $V_{SENSE} = 150\text{ mV}$ (ADM4073F)
		0.8	1.2	V	$V_{CC} = 15\text{ V}$, $V_{SENSE} = 150\text{ mV}$ (ADM4073H), $T_A = 25^\circ\text{C}$
DYNAMIC CHARACTERISTICS					
Bandwidth, BW		1.8		MHz	$V_{SENSE} = 100\text{ mV}$, $V_{CC} = 12\text{ V}$, $V_{RS+} = 12\text{ V}$, $C_{LOAD} = 5\text{ pF}$ (ADM4073T)
		1.7		MHz	$V_{SENSE} = 100\text{ mV}$, $V_{CC} = 12\text{ V}$, $V_{RS+} = 12\text{ V}$, $C_{LOAD} = 5\text{ pF}$ (ADM4073F)
		1.6		MHz	$V_{SENSE} = 100\text{ mV}$, $V_{CC} = 12\text{ V}$, $V_{RS+} = 12\text{ V}$, $C_{LOAD} = 5\text{ pF}$ (ADM4073H)
		600		kHz	$V_{SENSE} = 6.25\text{ mV}$, ³ $V_{CC} = 12\text{ V}$, $V_{RS+} = 12\text{ V}$, $C_{LOAD} = 5\text{ pF}$ (ADM4073T/F/H)
Gain, A_v		20		V/V	ADM4073T
		50		V/V	ADM4073F
		100		V/V	ADM4073H
Gain Accuracy		± 1.0	± 2.0	%	$V_{SENSE} = 10\text{ mV to } 150\text{ mV}$, $V_{CC} = 12\text{ V}$, $V_{RS+} = 12\text{ V}$, $T_A = +25^\circ\text{C}$ (ADM4073T/F)
			± 2.0	%	$V_{SENSE} = 10\text{ mV to } 150\text{ mV}$, $V_{CC} = 12\text{ V}$, $V_{RS+} = 12\text{ V}$, $T_A = -40^\circ\text{C to } +125^\circ\text{C}$ (ADM4073T/F)
		± 1.0	± 1.5	%	$V_{SENSE} = 10\text{ mV to } 100\text{ mV}$, $V_{CC} = 12\text{ V}$, $V_{RS+} = 12\text{ V}$, $T_A = +25^\circ\text{C}$ (ADM4073H)
			± 3.0	%	$V_{SENSE} = 10\text{ mV to } 100\text{ mV}$, $V_{CC} = 12\text{ V}$, $V_{RS+} = 12\text{ V}$, $T_A = -40^\circ\text{C to } +125^\circ\text{C}$ (ADM4073H)
OUT Settling Time to 1% of Final Value		400		ns	$V_{SENSE} = 6.25\text{ mV to } 100\text{ mV}$, $V_{CC} = 12\text{ V}$, $V_{RS+} = 12\text{ V}$, $C_{LOAD} = 5\text{ pF}$
		800		ns	$V_{SENSE} = 100\text{ mV to } 6.25\text{ mV}$, $V_{CC} = 12\text{ V}$, $V_{RS+} = 12\text{ V}$, $C_{LOAD} = 5\text{ pF}$
Output Resistance, R_{OUT}		12		k Ω	
Power Supply Rejection Ratio, PSRR		78		dB	$V_{SENSE} = 60\text{ mV}$, $V_{CC} = 3\text{ V to } 28\text{ V}$ (ADM4073T)
		85		dB	$V_{SENSE} = 24\text{ mV}$, $V_{CC} = 3\text{ V to } 28\text{ V}$ (ADM4073F)
		90		dB	$V_{SENSE} = 12\text{ mV}$, $V_{CC} = 3\text{ V to } 28\text{ V}$ (ADM4073H)
Power-Up Time ⁴		5		μs	$C_{LOAD} = 5\text{ pF}$, $V_{SENSE} = 100\text{ mV}$
Saturation Recovery Time ⁵		5		μs	$C_{LOAD} = 5\text{ pF}$, $V_{CC} = 12\text{ V}$, $V_{RS+} = 12\text{ V}$

¹ 100% production tested at $T_A = 25^\circ\text{C}$. Specifications over temperature limit are guaranteed by design.

² The sum of the gain and offset errors is the total OUT voltage error.

³ $6.25\text{ mV} = 1/16^{\text{th}}$ of 100 mV full-scale sense voltage.

⁴ Output settles to within 1% of final value.

⁵ When overdriven, this device does not experience phase reversal.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_{CC} to GND	–0.3 V to +30 V
RS+, RS– to GND	–0.3 V to +30 V
OUT to GND	–0.3 V to ($V_{CC} + 0.3$ V)
OUT Short-Circuit to GND	Continuous
Differential Input Voltage ($V_{RS+} - V_{RS-}$)	±5 V
Current into Any Pin	±20 mA
Storage Temperature Range	–65°C to +125°C
Operating Temperature Range	–40°C to +125°C
Lead Temperature, Soldering (10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
6-Lead SOT-23	169.5	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

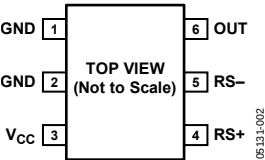
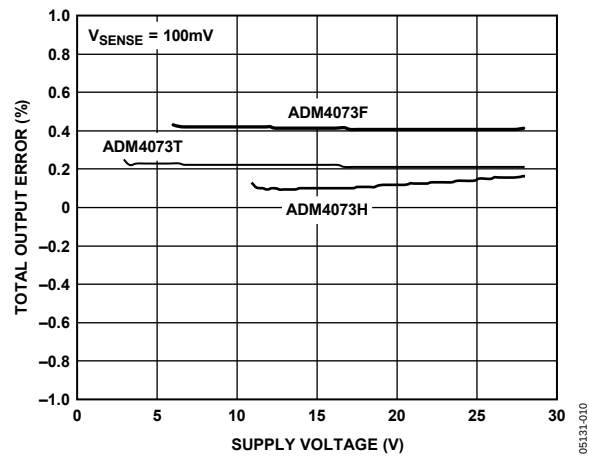
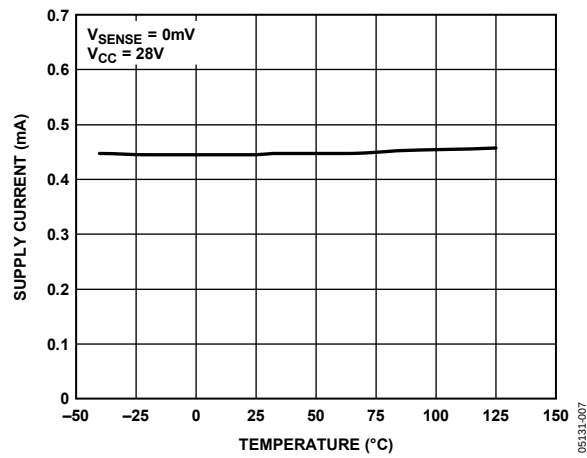
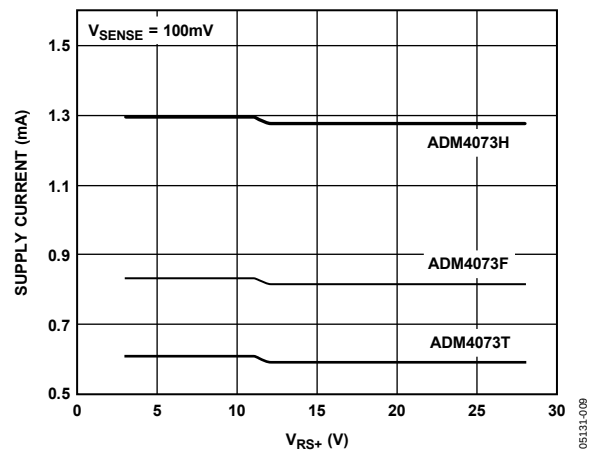
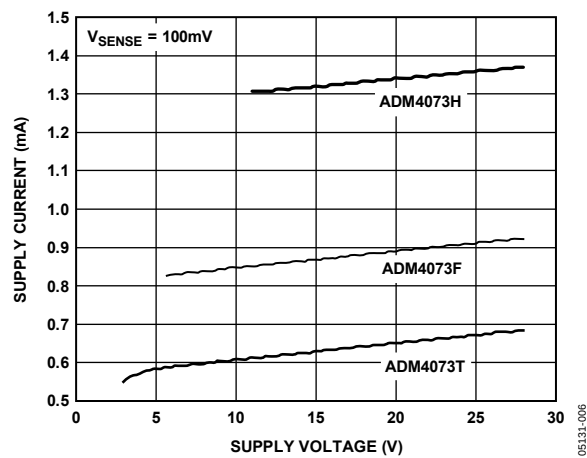
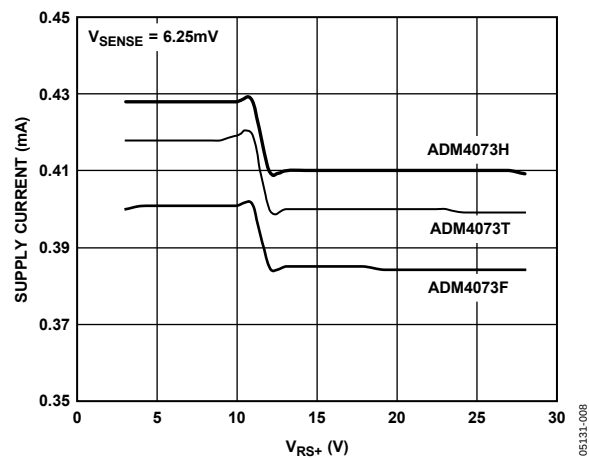
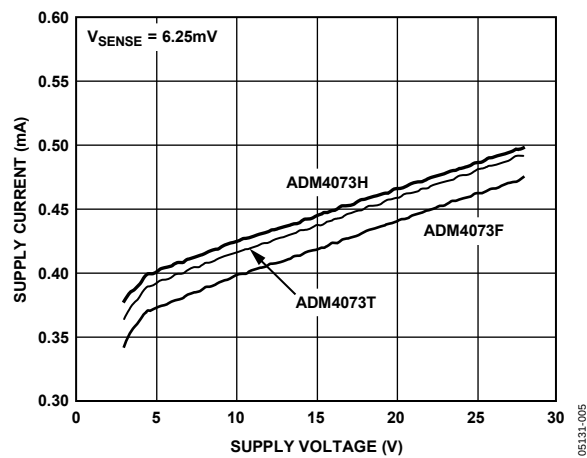


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND	Chip Ground Pin.
2	GND	Chip Ground Pin.
3	V _{CC}	Chip Power Supply. Requires a 0.1 μ F capacitor to ground.
4	RS+	Power-Side Connection to the External Sense Resistor.
5	RS-	Load-Side Connection to the External Sense Resistor.
6	OUT	Voltage Output. V _{OUT} is proportional to V _{SENSE} . Output impedance is approximately 12 k Ω .

TYPICAL PERFORMANCE CHARACTERISTICS



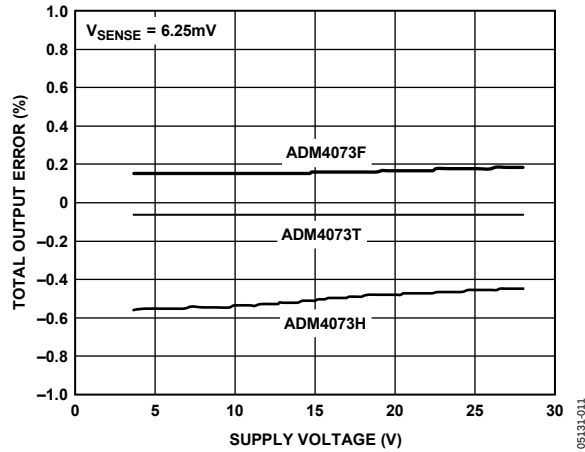


Figure 10. Total Output Error vs. Supply Voltage ($V_{SENSE} = 6.25 \text{ mV}$)

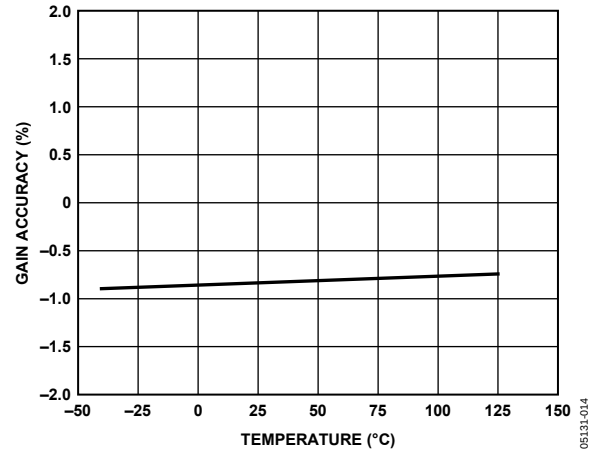


Figure 13. Gain Accuracy vs. Temperature

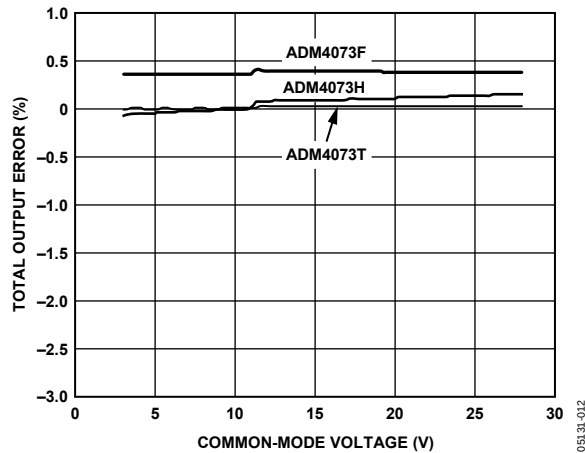


Figure 11. Total Output Error vs. Common-Mode Voltage

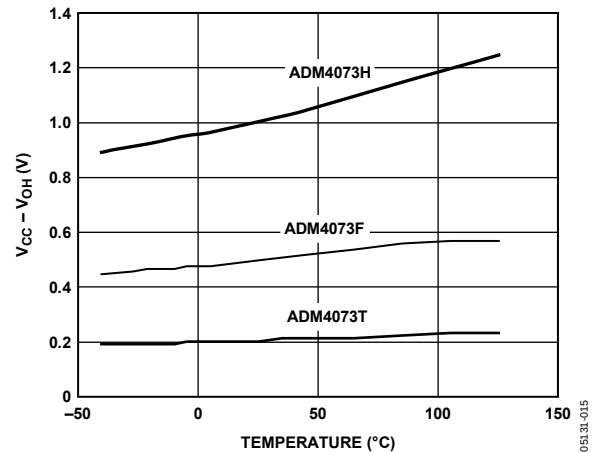


Figure 14. Output High Voltage ($V_{CC} - V_{OH}$) vs. Temperature

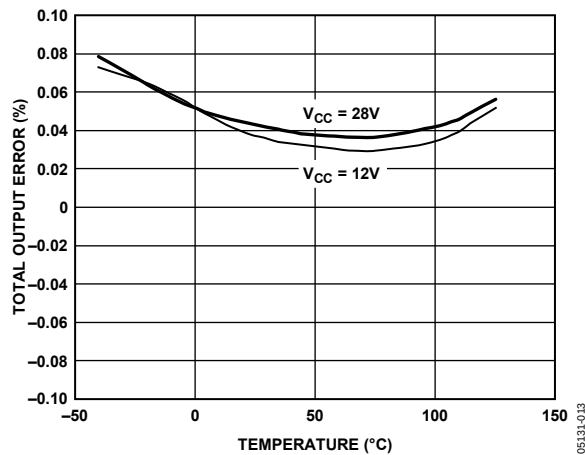


Figure 12. Total Output Error vs. Temperature

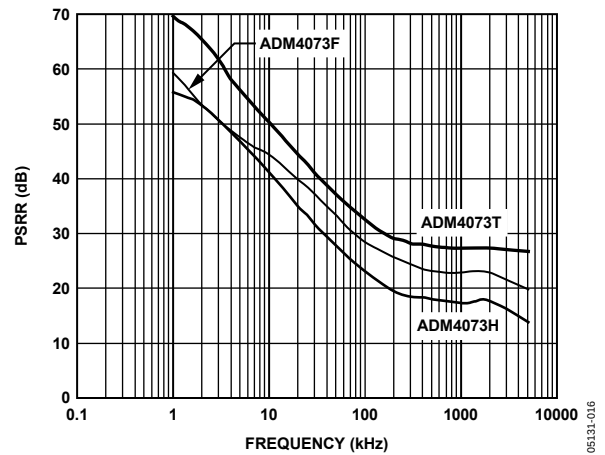


Figure 15. PSRR vs. Frequency

ADM4073

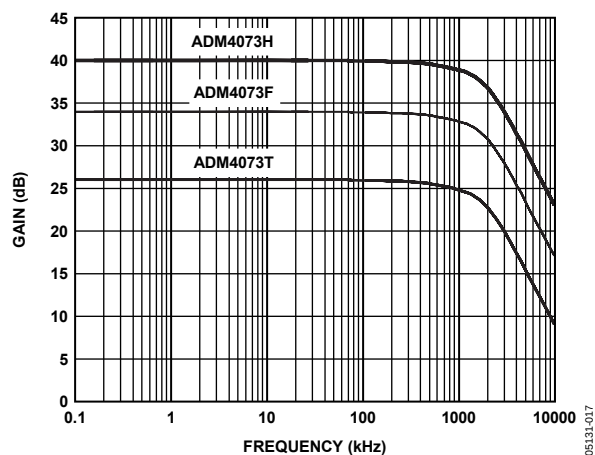


Figure 16. Small Signal Gain vs. Frequency

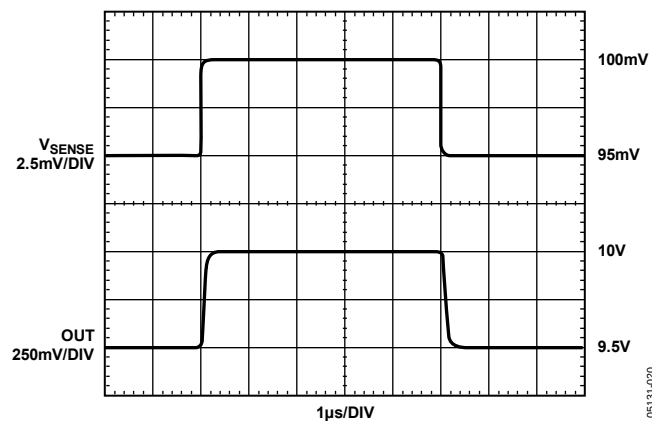


Figure 19. ADM4073H Small Signal Transient Response

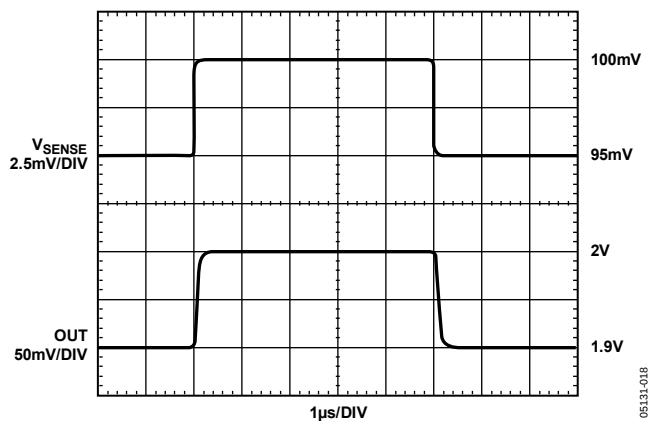


Figure 17. ADM4073T Small Signal Transient Response

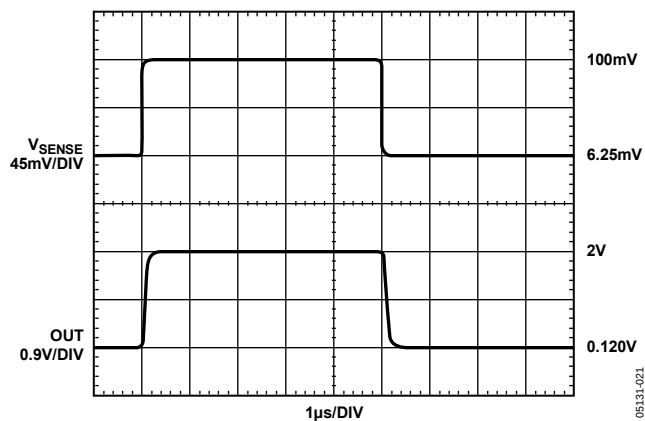


Figure 20. ADM4073T Large Signal Transient Response

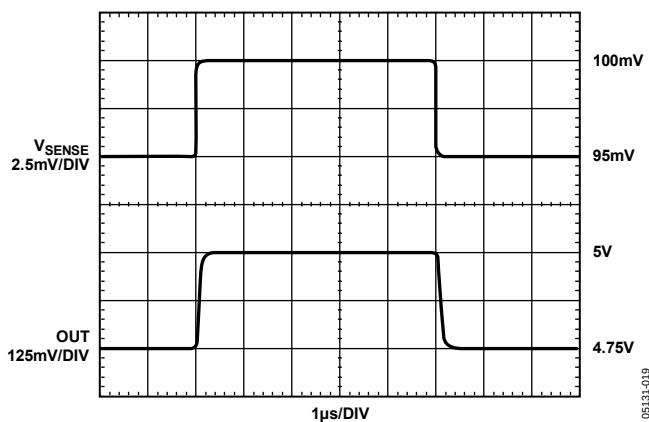


Figure 18. ADM4073F Small Signal Transient Response

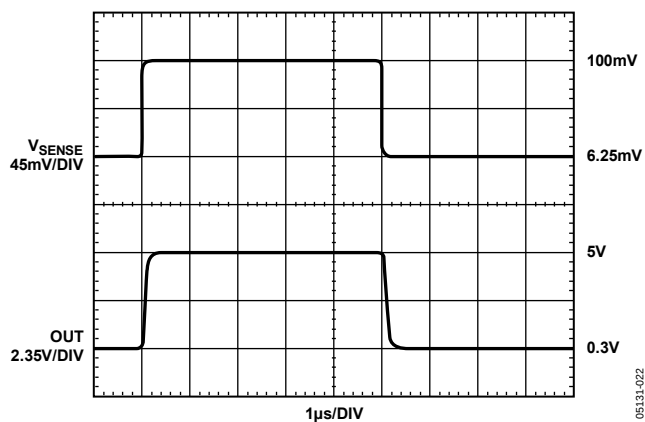


Figure 21. ADM4073F Large Signal Transient Response

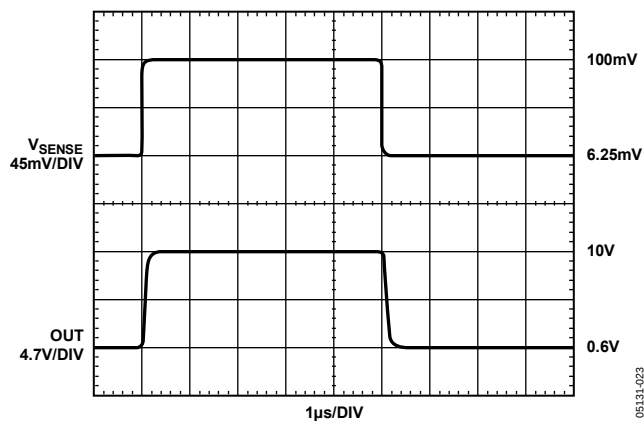


Figure 22. ADM4073H Large Signal Transient Response

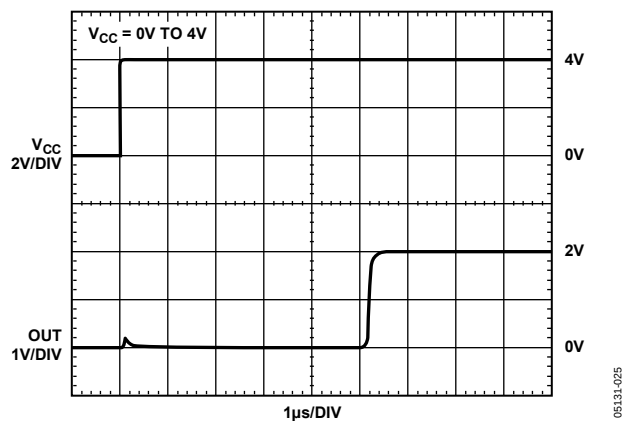


Figure 24. ADM4073T Start-Up Delay

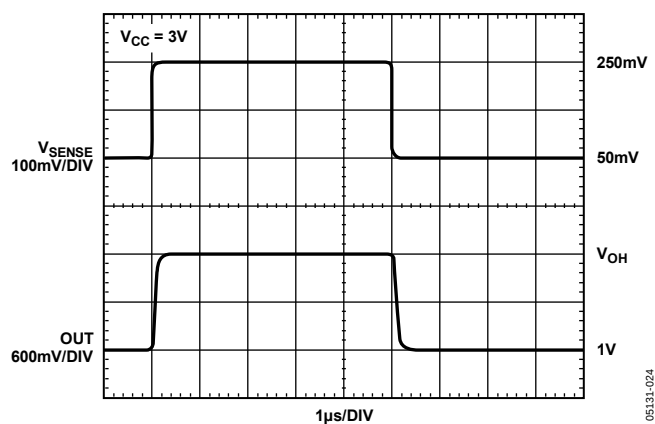


Figure 23. ADM4073T Overdrive Response

THEORY OF OPERATION

The current from the source flows through R_{SENSE} , which generates a voltage drop, V_{SENSE} , across the $RS+$ and $RS-$ terminals of the sense amplifier. The Input Stage Amplifier A1 regulates its inputs to be equal, thereby shunting a current proportional to V_{SENSE}/R_{G1} to the output current mirror. This current is then multiplied by a gain factor of b in the output stage current mirror and flows through R_{GD} to generate V_{OUT} . Therefore, V_{OUT} is related to V_{SENSE} by the ratio of R_{G1} to R_{GD} and the current gain of b .

$$V_{OUT} = A_V \times V_{SENSE}$$

where:

$$A_V = R_{GD}/R_{G1} \times b$$

A_V is equal to different voltages depending upon the model of the device.

- 20 V/V for ADM4073T.
- 50 V/V for ADM4073F.
- 100 V/V for ADM4073H.

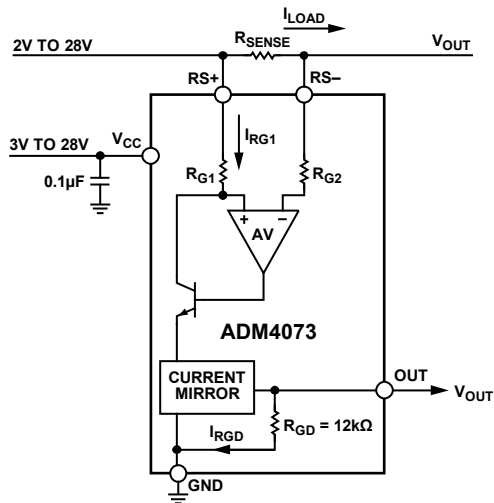


Figure 25. Functional Block Diagram

R_{SENSE}

The ADM4073 has the ability to sense a wide variety of currents by selecting a particular sense resistor. Select a suitable output voltage for full-scale current, such as 10 V for 10 A. Then, select a gain model that gives the most efficient use of the sense voltage range (150 mV max).

In the example above, using the ADM4073H (gain of 100) gives an output voltage of 10 V when the sense voltage is 100 mV. Use the following equation to determine what value of sense resistor gives 100 mV with 10 A flowing through it:

$$R_{SENSE} = 100 \text{ mV} / 10 \text{ A}$$

$$R_{SENSE} = 10 \text{ m}\Omega$$

$$V_{OUT} = (I_{LOAD} \times R_{SENSE}) \times A_V$$

To measure lower currents accurately, use as large a sense resistor as possible to utilize the higher end of the sense voltage range. This reduces the effects of the offset voltage errors in the internal amplifier.

When currents are very large, it is important to take the I^2R power losses across the sense resistor into account. If the sense resistor's rated power dissipation is not sufficient, its value can drift, giving an inaccurate output voltage or it could fail altogether. This, in turn, causes the voltage across the $RS+$ and $RS-$ pins to exceed the absolute maximum ratings.

If the monitored supply rail has a large amplitude high frequency component, choose a sense resistor with low inductance.

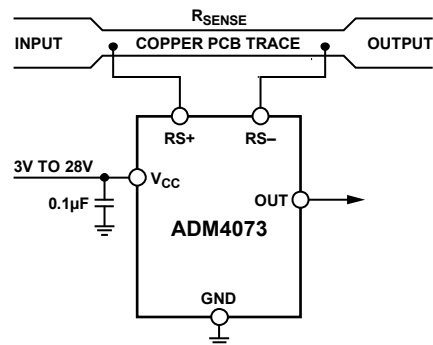


Figure 26. Using PCB Trace for Current Sensing

OUTPUT (OUT)

The output stage of the ADM4073 is a current source driving a pull-down resistance. To ensure optimum accuracy, care must be taken not to load this output externally. To minimize output errors, ensure OUT is connected to a high impedance input stage. If this is not possible, output buffering is recommended.

The percent error introduced by output loading is determined with the following formula:

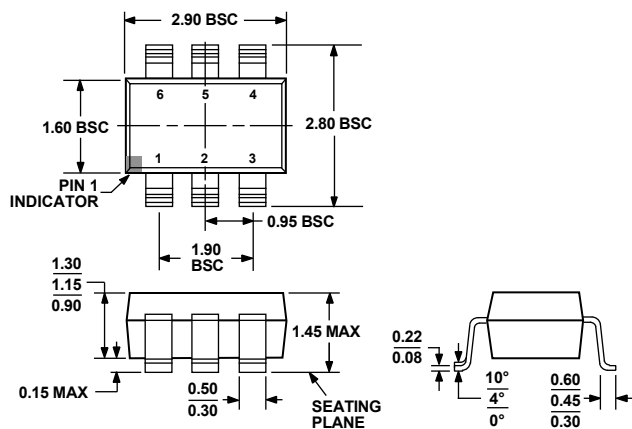
$$\% \text{ Error} = 100 \left(1 - R_{LOAD} / (R_{OUT_INT} + R_{LOAD}) \right)$$

where:

R_{LOAD} is the external load applied to OUT.

R_{OUT_INT} is the internal output resistance (12 kΩ).

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-AB
Figure 27. 6-Lead Small Outline Transistor Package [SOT-23]
(RJ-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Gain	Temperature Range	Package Description	Package Option	Branding
ADM4073TWRJZ-REEL7 ¹	20	-40°C to +125°C	6-Lead SOT-23	RJ-6	M2E
ADM4073FWRJZ-REEL7 ¹	50	-40°C to +125°C	6-Lead SOT-23	RJ-6	M2C
ADM4073HWRJZ-REEL7 ¹	100	-40°C to +125°C	6-Lead SOT-23	RJ-6	M2D
ADM4073WFWRJZ-RL7 ^{1, 2}	50	-40°C to +125°C	6-Lead SOT-23	RJ-6	M2C

¹ Z = RoHS Compliant Part.
² Automotive Grade.

NOTES