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REVISION HISTORY

4/16—Rev. 0 to Rev. A	
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5/07—Revision 0: Initial Version

SPECIFICATIONS

$V_S = 5\text{ V}$; $T_A = 25^\circ\text{C}$; LO = 2 dBm; baseband I/Q amplitude = 1 V p-p differential sine waves in quadrature with a 1.5 V dc bias; baseband I/Q frequency (f_{BB}) = 1 MHz, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Operating Frequency Range ADL5590		869 1805		960 1990	MHz MHz
ADL5590 @ $f_{\text{RF}} = 880\text{ MHz}$					
Output Power vs. Frequency vs. Temperature	$V_{\text{IQ}} = 1.0\text{ V p-p differential}$ $f_{\text{RF}} = 869\text{ MHz to }894\text{ MHz}$ $0^\circ\text{C to }85^\circ\text{C}$ $-25^\circ\text{C to }0^\circ\text{C}$	3.75	5.9 ± 0.1 0.01 0.01	8.0	dBm dB dB/ $^\circ\text{C}$ dB/ $^\circ\text{C}$
Sideband Suppression			-50		dBc
LO Leakage			-50		dBc
Output Return Loss			2.8		dB
Output P1 dB			16		dBm
Output IP3	$f_{1\text{BB}} = 3.5\text{ MHz}, f_{2\text{BB}} = 4.5\text{ MHz}, P_{\text{OUT}} = 0\text{ dBm per tone}$		29		dBm
Output IP2	$f_{1\text{BB}} = 3.5\text{ MHz}, f_{2\text{BB}} = 4.5\text{ MHz}, P_{\text{OUT}} = 0\text{ dBm per tone}$		66		dBm
Output Noise Density	$P_{\text{OUT}} = 5\text{ dBm}, 6\text{ MHz carrier offset}$		-155		dBc/Hz
Output Noise Floor	Baseband inputs biased to 1.5 V		-156.6		dBm/Hz
Modulation Spectrum	Relative to carrier in 30 kHz, $P_{\text{OUT}} = 3\text{ dBm}, 8\text{ PSK}$ 250 kHz carrier offset 400 kHz carrier offset 600 kHz carrier offset 1.2 MHz carrier offset		-42.5 -71.1 -78.5 -79.1		dBc dBc dBc dBc
RMS Error Vector Magnitude	$P_{\text{OUT}} = 3\text{ dBm}, 8\text{ PSK}$		0.5		%
Peak Error Vector Magnitude	$P_{\text{OUT}} = 3\text{ dBm}, 8\text{ PSK}$		1.5		%
ADL5590 @ $f_{\text{RF}} = 940\text{ MHz}$					
Output Power vs. Frequency vs. Temperature	$V_{\text{IQ}} = 1.0\text{ V p-p differential}$ $f_{\text{RF}} = 925\text{ MHz to }960\text{ MHz}$ $0^\circ\text{C to }85^\circ\text{C}$ $-25^\circ\text{C to }0^\circ\text{C}$	3.5	5.7 ± 0.1 0.01 0.01	7.75	dBm dB dB/ $^\circ\text{C}$ dB/ $^\circ\text{C}$
Sideband Suppression			-50		dBc
LO Leakage			-50		dBc
Output Return Loss			3.2		dB
Output P1 dB			16		dBm
Output IP3	$f_{1\text{BB}} = 3.5\text{ MHz}, f_{2\text{BB}} = 4.5\text{ MHz}, P_{\text{OUT}} = 0\text{ dBm per tone}$		29		dBm
Output IP2	$f_{1\text{BB}} = 3.5\text{ MHz}, f_{2\text{BB}} = 4.5\text{ MHz}, P_{\text{OUT}} = 0\text{ dBm per tone}$		70		dBm
Output Noise Floor	Baseband inputs biased to 1.5 V		-156.6		dBm/Hz
Modulation Spectrum	Relative to carrier in 30 kHz, $P_{\text{OUT}} = 3\text{ dBm}, 8\text{ PSK}$ 250 kHz carrier offset 400 kHz carrier offset 600 kHz carrier offset 1.2 MHz carrier offset		-42.5 -71.1 -78.5 -79.1		dBc dBc dBc dBc
RMS Error Vector Magnitude	$P_{\text{OUT}} = 3\text{ dBm}, 8\text{ PSK}$		0.4		%
Peak Error Vector Magnitude	$P_{\text{OUT}} = 3\text{ dBm}, 8\text{ PSK}$		1.4		%
ADL5591 @ $f_{\text{RF}} = 1850\text{ MHz}$					
Output Power vs. Frequency vs. Temperature	$f_{\text{RF}} = 1850\text{ MHz}$ $V_{\text{IQ}} = 1.0\text{ V p-p differential}$ $f_{\text{RF}} = 1805\text{ MHz to }1880\text{ MHz}$ $0^\circ\text{C to }85^\circ\text{C}$ $-25^\circ\text{C to }0^\circ\text{C}$	3.0	5.0 ± 0.1 0.011 0.011	7.0	dBm dB dB/ $^\circ\text{C}$ dB/ $^\circ\text{C}$
Sideband Suppression			-47		dBc

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LO Leakage			−44		dBc
Output Return Loss			5.4		dB
Output P1 dB			16		dBm
Output IP3	$f_{1BB} = 3.5 \text{ MHz}$, $f_{2BB} = 4.5 \text{ MHz}$, $P_{OUT} = -1 \text{ dBm}$ per tone		30		dBm
Output IP2	$f_{1BB} = 3.5 \text{ MHz}$, $f_{2BB} = 4.5 \text{ MHz}$, $P_{OUT} = -1 \text{ dBm}$ per tone		60		dBm
Output Noise Density	$P_{OUT} = 5 \text{ dBm}$, 6 MHz carrier offset		−156		dBc/Hz
Output Noise Floor	Baseband inputs biased to 1.5 V		−157		dBm/Hz
Modulation Spectrum	Relative to carrier in 30 kHz, $P_{OUT} = 3 \text{ dBm}$, 8 PSK				
	250 kHz carrier offset		−42.5		dBc
	400 kHz carrier offset		−71.3		dBc
	600 kHz carrier offset		−79.4		dBc
	1.2 MHz carrier offset		−80.2		dBc
RMS Error Vector Magnitude	$P_{OUT} = 3 \text{ dBm}$, 8 PSK		0.5		%
Peak Error Vector Magnitude	$P_{OUT} = 3 \text{ dBm}$, 8 PSK		1.7		%
ADL5591 @ $f_{RF} = 1960 \text{ MHz}$					
Output Power	$V_{IQ} = 1.0 \text{ V}$ p-p differential	2.5	4.7	6.5	dBm
vs. Frequency	$f_{RF} = 1930 \text{ MHz}$ to 1990 MHz		± 0.1		dB
vs. Temperature	0°C to 85°C		+0.011		dB/ $^\circ\text{C}$
	-25°C to 0°C		+0.011		dB/ $^\circ\text{C}$
Sideband Suppression			−48		dBc
LO Leakage			−44		dBc
Output Return Loss			6.0		dB
Output P1dB			16		dBm
Output IP3	$f_{1BB} = 3.5 \text{ MHz}$, $f_{2BB} = 4.5 \text{ MHz}$, $P_{OUT} = -1 \text{ dBm}$ per tone		30		dBm
Output IP2	$f_{1BB} = 3.5 \text{ MHz}$, $f_{2BB} = 4.5 \text{ MHz}$, $P_{OUT} = -1 \text{ dBm}$ per tone		60		dBm
Output Noise Density	$P_{OUT} = 5 \text{ dBm}$, 6 MHz carrier offset		−156		dBc/Hz
Output Noise Floor	Baseband inputs biased to 1.5 V		157		dBm/Hz
Modulation Spectrum	Relative to carrier in 30 kHz, $P_{OUT} = 3 \text{ dBm}$, 8 PSK				
	250 kHz carrier offset		−42.5		dBc
	400 kHz carrier offset		−71.4		dBc
	600 kHz carrier offset		−79.7		dBc
	1.2 MHz carrier offset		−80.5		dBc
RMS Error Vector Magnitude	$P_{OUT} = 3 \text{ dBm}$, 8 PSK		0.5		%
Peak Error Vector Magnitude	$P_{OUT} = 3 \text{ dBm}$, 8 PSK		1.6		%
LO INPUTS					
LO Drive Level ¹	LOIP, LOIN	−1	+2	+5	dBm
Input Return Loss	ADL5590 @ $f_{RF} = 880 \text{ MHz}$		7.5		dB
	ADL5591 @ $f_{RF} = 1850 \text{ MHz}$		10.7		dB
BASEBAND INPUTS					
I and Q Input Bias Level	Pins IBBP, IBBN, QBBP, QBBN		1.5		V
Bandwidth (3 dB)			250		MHz
Differential Input Impedance			9		k Ω
POWER SUPPLIES					
Voltage	Pin VPS1 to Pin VPS5	4.75		5.25	V
	Full specification	4.5		5.5	V
	Degraded specification				
Supply Current			170		mA
ADL5590			170		mA
ADL5591			170		mA

¹ LO drive in excess of 5 dBm can be provided to further reduce noise at 6 MHz carrier offset.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, VPS1 to VPS5	5.5 V
IBBP, IBBN, QBBP, QBBN	0 V, 3 V
LOIP	10 dBm
Internal Power Dissipation	1155 mW
θ_{JA} (Exposed Pad Soldered Down)	40°C/W
Maximum Junction Temperature	132°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Maximum Soldering Temperature	260°C

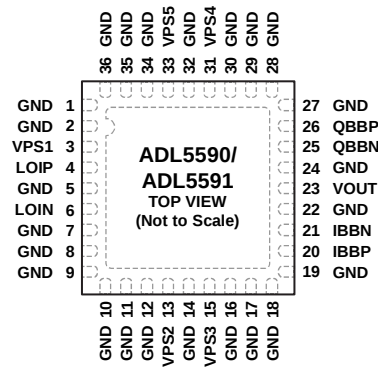
Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD. CONNECT THE EXPOSED PAD TO THE GROUND PLANE VIA A LOW IMPEDANCE PATH.

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 5, 7 to 12, 14, 16 to 19, 22, 24, 27 to 30, 32, 34 to 36	GND	Ground. Connect to ground plane via a low impedance path.
3, 13, 15, 31, 33	VPS1, VPS2, VPS3, VPS4, VPS5	Positive Supply Voltage. Connect all pins to the same supply. To ensure adequate external bypassing, connect 0.1 μ F capacitors between each pin and ground.
4, 6	LOIP, LOIN	Local Oscillator Input. 50 Ω single-ended local oscillator input. Pins must be ac-coupled. AC-couple LOIN to ground and drive LO through LOIP.
20, 21, 25, 26	IBBP, IBBN, QBBN, QBBP	Baseband Inputs. Differential in-phase and quadrature baseband inputs. These high impedance inputs must be dc-biased to approximately 1.5 V dc. These inputs are not self-biased and must be externally biased.
23	VOUT	RF Output. Single-ended, 50 Ω , internally biased RF output. Pin must be ac-coupled to the load.
	Exposed Pad	Exposed Pad. Connect the exposed pad to the ground plane via a low impedance path.

The schematic diagram illustrates the internal architecture of the ADL5590/ADL5591 PLL. The core components include a QUADRATURE PHASE SPLITTER, two multipliers (represented by 'X' symbols), and a summing junction (represented by a 'Σ' symbol). The circuit is powered by VCC and has various pins for GND, VPS1, LOIP, LOIN, and RFOUT. Capacitors C1, C2, C3, C4, C5, C6, C7, and C8 are shown with their values and connections.

Pin Connections:

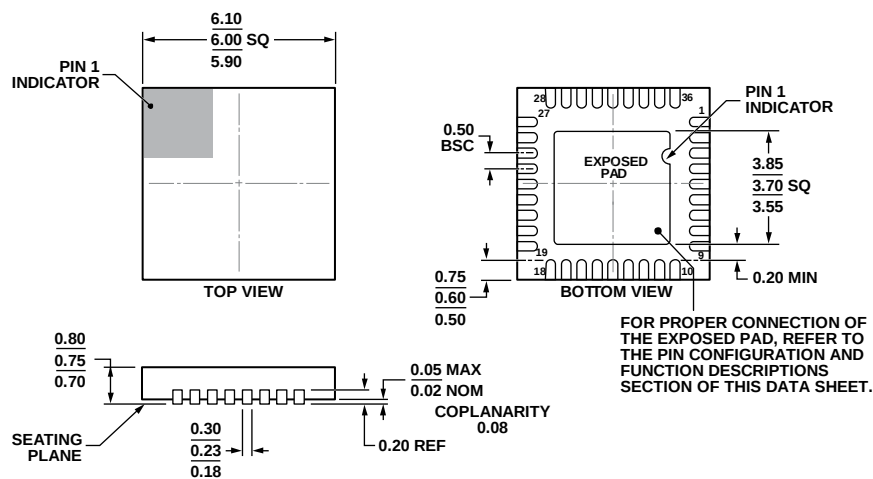
- Pin 1:** GND
- Pin 2:** GND
- Pin 3:** VPS1
- Pin 4:** LOIP
- Pin 5:** GND
- Pin 6:** LOIN
- Pin 7:** GND
- Pin 8:** GND
- Pin 9:** GND
- Pin 10:** GND
- Pin 11:** GND
- Pin 12:** GND
- Pin 13:** VPS2
- Pin 14:** GND
- Pin 15:** VPS3
- Pin 16:** GND
- Pin 17:** GND
- Pin 18:** GND
- Pin 19:** GND
- Pin 20:** IBBP
- Pin 21:** IBBN
- Pin 22:** GND
- Pin 23:** VOUT
- Pin 24:** GND
- Pin 25:** QBBN
- Pin 26:** QBBP
- Pin 27:** GND
- Pin 28:** GND
- Pin 29:** GND
- Pin 30:** GND
- Pin 31:** VPS4
- Pin 32:** GND
- Pin 33:** VPS5
- Pin 34:** GND
- Pin 35:** GND
- Pin 36:** GND

Component Values and Connections:

- C1:** 0.1μF, connected to VCC and Pin 1.
- C2:** 100pF, connected to LO and Pin 4.
- C3:** 100pF, connected to Pin 6 and GND.
- C4:** 0.1μF, connected to VCC and Pin 13.
- C5:** 0.1μF, connected to VCC and Pin 15.
- C6:** 100pF, connected to RFOUT and Pin 23.
- C7:** 0.1μF, connected to VCC and Pin 30.
- C8:** 0.1μF, connected to VCC and Pin 34.

Figure 3. Basic Connections for Operation

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WJJD-1.

Figure 4. 36-Lead Lead Frame Chip Scale Package [LFCSP]
 6 mm × 6 mm Body and 0.75 mm Package Height
 (CP-36-4)

Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADL5590ACPZ-R7	−40°C to +85°C	36-Lead LFCSP, 7" Tape and Reel	CP-36-4
ADL5591ACPZ-R7	−40°C to +85°C	36-Lead LFCSP, 7" Tape and Reel	CP-36-4

¹ Z = RoHS Compliant Part.