TABLE OF CONTENTS

Features
Applications1
General Description
Functional Block Diagrams
Revision History
Product Highlights
Specifications
15 V Dual Supply4
12 V Single Supply5
5 V Dual Supply6
REVISION HISTORY
10/06—Rev. B to Rev. C
Changes to Table 49
Changes to Ordering Guide
12/04—Rev. A to Rev. B
Updated FormatUniversal
Changes to Specifications Section
Changes to Absolute Maximum Ratings Section
Changes to Pin Configuration and Function
Descriptions Section
Updated Outline Dimensions
Changes to Ordering Guide

Absolute Maximum Ratings
ESD Caution
Pin Configuration and Function Descriptions
Typical Performance Characteristics
Terminology1
Applications
Test Circuits
Outline Dimensions
Ordering Guide1

2/98—Rev. 0 to Rev. A

10/97—Revision 0: Initial Version

PRODUCT HIGHLIGHTS

- 1. Low R_{ON} (5 Ω maximum).
- 2. Ultralow Power Dissipation.
- 3. Extended Signal Range. The ADG451/ADG452/ADG453 are fabricated on an enhanced LC^2MOS process, giving an increased signal range that fully extends to the supply rails.
- Break-Before-Make Switching.
 This prevents channel shorting when the switches are configured as a multiplexer (ADG453 only.)

- 5. Single-Supply Operation.
 - For applications in which the analog signal is unipolar, the ADG451/ADG452/ADG453 can be operated from a single rail power supply. The parts are fully specified with a single 12 V power supply and remain functional with single supplies as low as 5.0 V.
- 6. Dual-Supply Operation.

For applications where the analog signal is bipolar, the ADG451/ADG452/ADG453 can be operated from a dual power supply ranging from $\pm 4.5~V$ to $\pm 20~V$.

SPECIFICATIONS

15 V DUAL SUPPLY

 V_{DD} = 15 V, V_{SS} = -15 V, V_{L} = 5 V, GND = 0 V. All specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 1

	В	Version ¹			
Parameter	25°C	T_{MIN} to T_{MAX}	Unit	Test Conditions/Comments	
ANALOG SWITCH					
Analog Signal Range		$V_{\text{SS}} \ to \ V_{\text{DD}}$	V		
On Resistance (R _{ON})	4		Ω typ	$V_D = -10 \text{ V to } +10 \text{ V, } I_S = -10 \text{ mA}$	
	5	7	Ω max		
On Resistance Match Between Channels (ΔR_{ON})	0.1		Ω typ	$V_D = \pm 10 \text{ V}, I_S = -10 \text{ mA}$	
	0.5	0.5	Ω max		
On Resistance Flatness (R _{FLAT(ON)})	0.2		Ωtyp	$V_D = -5 \text{ V}, 0 \text{ V}, +5 \text{ V}, I_S = -10 \text{ mA}$	
	0.5	0.5	Ω max		
LEAKAGE CURRENTS ²					
Source Off Leakage, Is (OFF)	±0.02		nA typ	$V_D = \pm 10 \text{ V}, V_S = \pm 10 \text{ V}; \text{ see Figure 17}$	
	±0.5	±2.5	nA max		
Drain Off Leakage, I _D (OFF)	±0.02		nA typ	$V_D = \pm 10 \text{ V}, V_S = \pm 10 \text{ V}; \text{ see Figure 17}$	
	±0.5	±2.5	nA max	_	
Channel On Leakage, ID, IS (ON)	±0.04		nA typ	$V_D = V_S = \pm 10 \text{ V}$; see Figure 18	
	±1	±5	nA max	_	
DIGITAL INPUTS					
Input High Voltage, V _{INH}		2.4	V min		
Input Low Voltage, V _{INL}		0.8	V max		
Input Current, I _{INL} or I _{INH}	0.005		μA typ	$V_{IN} = V_{INL}$ or V_{INH} ; all others = 2.4 V or 0.8 V, respectively	
·		±0.5	μA max		
DYNAMIC CHARACTERISTICS ³					
ton	70		ns typ	$R_L = 300 \Omega$, $C_L = 35 pF$, $V_S = \pm 10 V$; see Figure 19	
	180	220	ns max		
toff	60		ns typ	$R_L = 300 \Omega$, $C_L = 35 pF$, $V_S = \pm 10 V$; see Figure 19	
	140	180	ns max		
Break-Before-Make Time Delay, t _D (ADG453 Only)	15		ns typ	$R_L = 300 \Omega$, $C_L = 35 pF$, $V_{S1} = V_{S2} = +10 V$; see Figure 20	
	5	5	ns min		
Charge Injection	20		pC typ	$V_S = 0 \text{ V}, R_S = 0 \Omega, C_L = 1.0 \text{ nF}; \text{ see Figure 21}$	
	30		pC max		
Off Isolation	65		dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$; see Figure 22	
Channel-to-Channel Crosstalk	-90		dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$; see Figure 23	
C _s (OFF)	37		pF typ	f = 1 MHz	
C _D (OFF)	37		pF typ	f = 1 MHz	
C_D , C_S (ON)	140		pF typ	f = 1 MHz	
POWER REQUIREMENTS				$V_{DD} = 16.5 \text{ V}, V_{SS} = -16.5 \text{ V}; \text{ digital inputs} = 0 \text{ V or } 5 \text{ V}$	
I _{DD}	0.0001		μA typ		
	0.5	5	μA max		
Iss	0.0001		μA typ		
	0.5	5	μA max		
I _L	0.0001		μA typ		
	0.5	5	μA max		
$I_{GND}{}^{3}$	0.0001		μA typ		
	0.5	5	μA max		

 $^{^{1}}$ Temperature range for B version is -40° C to $+85^{\circ}$ C.

 $^{^{2}}T_{MAX} = 70^{\circ}C.$

 $^{^{\}rm 3}$ Guaranteed by design, not subject to production test.

12 V SINGLE SUPPLY

 $V_{DD} = 12 \; V, \, V_{SS} = 0 \; V, \, V_L = 5 \; V, \, GND = 0 \; V. \; All \; specifications \; T_{MIN} \; to \; T_{MAX}, \, unless \; otherwise \; noted.$

Table 2.

Parameter Par		B Version ¹			
Analog Signal Range On Resistance (Row) 6 8 10 Ω typ On Resistance Match Between Channels (ΔRow) On Resistance Flatness (R _{FLNTIONI}) 0.5 0.5 0.5 0.5 0.6 Ω max On Resistance Flatness (R _{FLNTIONI}) 0.1 0.0 0.5 0.5 0.5 0.7 0 max On Resistance Flatness (R _{FLNTIONI}) 0.1 0.0 0.0	Parameter	25°C	T_{MIN} to T_{MAX}	Unit	Test Conditions/Comments
On Resistance (Row) 6 Ω typ Q nax (Ω raw) V ₀ = 0 V to +10 V, I ₅ = −10 mA On Resistance Match Between Channels (ΔRow) 0.1 Ω typ Q nax V ₀ = 10 V, I ₅ = −10 mA On Resistance Flatness (Retarjow) 1.0 1.0 Ω typ Q nax V ₀ = 10 V, I ₅ = −10 mA LEAKAGE CURRENTS ^{2.3} Source Off Leakage, I ₅ (OFF) ±0.02 nA typ ±0.5 nA typ nA max V ₀ = 0 V, 10 V, V ₅ = 0 V, 10 V; see Figure 17 Drain Off Leakage, I ₀ (OFF) ±0.02 nA typ ±0.5 nA max V ₀ = 0 V, 10 V, V ₅ = 0 V, 10 V; see Figure 17 Channel On Leakage, I ₀ , I ₅ (ON) ±0.02 nA max nA typ nA max V ₀ = 0 V, 10 V, V ₅ = 0 V, 10 V; see Figure 17 DIGITAL INPUTS Input High Voltage, V _{NM} 1 (put Current, I ₁ n ₁ or I ₁ n ₂ or I ₁ n ₂ or I ₁ n ₂ or I ₁ n ₃ 2.4 V min nA max V max part name Input Current, I ₁ n ₁ or I ₁ n ₂ or I ₁ n ₂ or I ₁ n ₃ 0.8 V max part name V ₁ = 300 Ω, C ₁ = 35 pF, V ₅ = 8 V; see Figure 19 DYNAMIC CHARACTERISTICS ⁴ to 1 100 styp name ns typ name R ₁ = 300 Ω, C ₁ = 35 pF, V ₅ = 8 V; see Figure 19 Break-Before-Make Time Delay, t ₀ (ADG453 Only) 15 styp name ns max name ns typ name R ₁ = 300 Ω, C ₁ = 35 pF, V ₅ = 8 V; see Figure 21 C ₁ (OFF) (c ₁ C ₁ C ₂ (C ₁)	ANALOG SWITCH				
No Resistance Match Between Channels (ΔRow) On Resistance Flatness (RrLARICOW) On A Day Vo = 10 V, Is = −10 mA No typ Vo = 0 V, 10 V, Vs = 0 V, 10 V; see Figure 17 No max No typ Vo = 0 V, 10 V, Vs = 0 V, 10 V; see Figure 17 No max Vo = 0 V, 10 V, Vs = 0 V, 10 V; see Figure 17 No max Vo = 0 V, 10 V, Vs = 0 V, 10 V; see Figure 17 No max Vo = 0 V, 10 V, Vs = 0 V, 10 V; see Figure 17 No max Vo = 0 V, 10 V, Vs = 0 V, 10 V; see Figure 17 No max Vo = 0 V, 10 V, Vs = 0 V, 10 V; see Figure 17 No max Vo = 0 V, 10 V, Vs = 0 V, 10 V; see Figure 18 Vo = 0 V, 10 V, Vs = 0 V, 10 V; see Figure 17 No max Vo = 0 V, 10 V, Vs = 0 V, 10 V; see Figure 18 Vo = 0 V, 10 V, Vs = 0 V, 10 V; see Figure 17 No max Vo = 0 V, 10 V, Vs = 0 V, 10 V; see Figure 17 No max Vo = 0 V, 10 V, Vs = 0 V, 10 V; see Figure 17 No max Vo = 0 V, 10 V, Vs = 0 V, 10 V; see Figure 17 No max Vo = 0 V, 10 V, Vs = 0 V, 10 V; see Figure 18 Vo = 0 V, 10 V, Vs = 0 V, 10 V; see Figure 17 No max Vo = 0 V, 10 V, Vs = 0 V, 10 V; see Figure 17 No max Vo = 0 V, 10 V, Vs = 0 V, 10 V; see Figure 17 No max Vo = 0 V, 10 V, Vs = 0 V, 10 V; see Figure 19 No max No	Analog Signal Range		$0VtoV_{DD}$	V	
On Resistance Match Between Channels (ΔRow) 0.1 Ω typ (0.5) V _D = 10 V, I _S = −10 mA On Resistance Flatness (R _{FLATIONO}) 1.0 1.0 Ω typ V _D = 0 V, 5 V, I _S = −10 mA LEAKAGE CURRENTS ^{2,3} Source Off Leakage, I _S (OFF) ±0.02 ±0.5 ±2.5 nA max NA typ V _D = 0 V, 10 V, V _S = 0 V, 10 V; see Figure 17 Drain Off Leakage, I _D (OFF) ±0.02 ±0.5 ±2.5 nA max nA typ V _D = 0 V, 10 V, V _S = 0 V, 10 V; see Figure 17 Channel On Leakage, I _D (NFC) ±0.5 ±2.5 nA max nA typ V _D = 0 V, 10 V, V _S = 0 V, 10 V; see Figure 17 DIGITAL INPUTS nA max nA max V _D = V _S = 0 V, 10 V; see Figure 18 Input High Voltage, V _{NoL} 0.8 V max V _D = V _S = 0 V, 10 V; see Figure 18 Input Current, I _{NoL} or I _{Not} 0.005 ±0.5 µA max V _D = V _S = 0 V, 10 V; see Figure 18 DYNAMIC CHARACTERISTICS ⁴ ns typ Ns typ Ns typ Ns typ R _L = 300 Ω, C _L = 35 pF, V _S = 8 V; see Figure 19 Break-Before-Make Time Delay, t _O (ADG453 Only) 15 ns typ R _L = 300 Ω, C _L = 35 pF, V _S = 8 V; see Figure 21 Charge Injection 10 10 ns typ V _S = 6 V, R _S = 0 Ω, C _L =	On Resistance (RoN)	6		Ω typ	$V_D = 0 \text{ V to } +10 \text{ V}, I_S = -10 \text{ mA}$
Do No Resistance Flatness (Relations) 1.0 1.0 1.0 Ω typ V ₀ = 0 V, 5 V, Is = −10 mA		8	10	Ω max	
On Resistance Flatness (Relations) 1.0 1.0 1.0 Ω typ V _D = 0 V, 5 V, Is = −10 mA LEAKAGE CURRENTS ²⁻³ 50urce Off Leakage, Is (OFF) ±0.02 ±0.5 ±2.5 nA max nA typ ±0.02 t±0.5 ±2.5 nA max nA typ ±0.04 nA typ ±0.04 nA typ ±1 ±5 nA max V _D = 0 V, 10 V, V _S = 0 V, 10 V; see Figure 17 Channel On Leakage, Io (OFF) ±0.02 ±0.04 nA max nA typ ±0.04 nA max nA typ nA max V _D = V _S = 0 V, 10 V; see Figure 18 DIGITAL INPUTS 2.4 V min Input Low Voltage, V _{INL} NPML Input Low Voltage, V _{INL} NPML Input Low Voltage, V _{INL} NPML Input Current, I _{INL} or I _{INH} 0.005 μA max 0.8 V max μA typ μA max V _{IN} = V _{INL} or V _{INL} NPML Input Current, I _{INL} or I _I o	On Resistance Match Between Channels (ΔR _{ON})	0.1		Ω typ	$V_D = 10 \text{ V, } I_S = -10 \text{ mA}$
LEAKAGE CURRENTS ^{2, 3} Source Off Leakage, Is (OFF) ±0.02		0.5	0.5	Ω max	
Source Off Leakage, Is (OFF)		1.0	1.0	Ω typ	$V_D = 0 \text{ V}, 5 \text{ V}, I_S = -10 \text{ mA}$
Drain Off Leakage, Io (OFF)	LEAKAGE CURRENTS ^{2, 3}				
Drain Off Leakage, Io (OFF) ±0.02 ±0.5 ±2.5 ±2.5 ±2.5 nA max typ ±0.04 ±0.04 ±0.04 ±0.04 to .nA typ nA typ nA typ nA max nA max nA typ nA max	Source Off Leakage, Is (OFF)	±0.02		nA typ	$V_D = 0 \text{ V}$, 10 V, $V_S = 0 \text{ V}$, 10 V; see Figure 17
±0.5 ±2.5 nA max nA typ thin typ thing Nottage, V _{INL} lnput Low Voltage, V _{INL} lnput Current, I _{INL} or I _{INH} ±0.04 thin typ thing Nottage, V _{INL} lnput Current, I _{INL} or I _{INH} 2.4 v min thing Nottage, V _{INL} lnput Current, I _{INL} or I _{INH} V max thing Nottage, V _{INL} lnput Current, I _{INL} or I _{INH} V max thing Nottage, V _{INL} lnput Current, I _{INL} or I _{INH} V max thing Nottage, V _{INL} lnput Current, I _{INL} or I _{INH} V max thing Nottage, V _{INL} lnput Current, I _{INL} or I _{INH} V max thing Nottage, V _{INL} lnput Current, I _{INL} or I _{INH} V max thing Nottage, V _{INL} lnput Current, I _{INL} or I _{INH} V max thing Nottage, V _{INL} lnput Current, I _{INL} or I _{INL} lnput Current, I		±0.5	±2.5	nA max	
Channel On Leakage, Io, Is (ON) ±0.04 ±1 ±5 nA typ nA max Vo = Vs = 0 V, 10 V; see Figure 18 DIGITAL INPUTS ±1 ±5 nA max V min Input High Voltage, V _{INH} Input Low Voltage, V _{INL} Input Current, I _{INL} or I _{INH} 0.8 V max µA max V max µA max DYNAMIC CHARACTERISTICS ⁴ 100 ns typ µA max RL = 300 Ω, CL = 35 pF, V ₅ = 8 V; see Figure 19 toFF 80 ns typ ns max RL = 300 Ω, CL = 35 pF, V ₅ = 8 V; see Figure 19 Break-Before-Make Time Delay, to (ADG453 Only) 15 ns typ ns max RL = 300 Ω, CL = 35 pF, V ₅ = 8 V; see Figure 19 Charge Injection 10 10 ns min ns min ns min ns min ns min ns min ns typ C typ Q V s = 6 V, Rs = 0 Ω, CL = 1.0 nF; see Figure 21 Channel-to-Channel Crosstalk -90 dB typ RL = 50 Ω, CL = 5 pF, f = 1 MHz; see Figure 23 C _S (OFF) 60 pF typ f = 1 MHz C _D , C _S (ON) 100 pF typ f = 1 MHz POWER REQUIREMENTS Vop = 13.2 V; digital inputs = 0 V or 5 V I _{DD} 0.0001 µA typ	Drain Off Leakage, I _D (OFF)	±0.02		nA typ	$V_D = 0 \text{ V}$, 10 V, $V_S = 0 \text{ V}$, 10 V; see Figure 17
±1 ±5 nA max		±0.5	±2.5	nA max	
DIGITAL INPUTS	Channel On Leakage, ID, IS (ON)	±0.04		nA typ	$V_D = V_S = 0 V$, 10 V; see Figure 18
Input High Voltage, V _{INL} 0.8 V min V max μA typ μA max		±1	±5	nA max	
Input Low Voltage, V _{INL} D.005	DIGITAL INPUTS				
Input Current, Inp	Input High Voltage, V _{INH}		2.4	V min	
DYNAMIC CHARACTERISTICS4 μA max toN 100 ns typ R _L = 300 Ω, C _L = 35 pF, V _S = 8 V; see Figure 19 toFF 80 ns typ R _L = 300 Ω, C _L = 35 pF, V _S = 8 V; see Figure 19 Break-Before-Make Time Delay, to (ADG453 Only) 15 ns typ R _L = 300 Ω, C _L = 35 pF, V _S = 8 V; see Figure 19 Charge Injection 10 10 ns min Channel-to-Channel Crosstalk -90 dB typ V _S = 6 V, R _S = 0 Ω, C _L = 1.0 nF; see Figure 21 C _S (OFF) 60 pF typ f = 1 MHz C _O (OFF) 60 pF typ f = 1 MHz C _O , C _S (ON) 100 pF typ f = 1 MHz POWER REQUIREMENTS 0.0001 μA typ V _{DD} = 13.2 V; digital inputs = 0 V or 5 V I _L 0.0001 μA typ μA typ	Input Low Voltage, V _{INL}		0.8	V max	
DYNAMIC CHARACTERISTICS ⁴ 100 ns typ R _L = 300 Ω, C _L = 35 pF, V _S = 8 V; see Figure 19 toFF 80 ns typ R _L = 300 Ω, C _L = 35 pF, V _S = 8 V; see Figure 19 Break-Before-Make Time Delay, t _D (ADG453 Only) 15 ns typ R _L = 300 Ω, C _L = 35 pF, V _S = 8 V; see Figure 19 Charge Injection 10 10 ns min Charge Injection 10 pC typ V _S = 6 V, R _S = 0 Ω, C _L = 1.0 nF; see Figure 21 Channel-to-Channel Crosstalk -90 dB typ R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 23 C _S (OFF) 60 pF typ f = 1 MHz C _D , C _S (ON) 100 pF typ f = 1 MHz POWER REQUIREMENTS μA typ V _{DD} = 13.2 V; digital inputs = 0 V or 5 V I _{DD} 0.0001 μA typ I _L 0.0001 μA typ	Input Current, I _{INL} or I _{INH}	0.005		μA typ	$V_{IN} = V_{INL} \text{ or } V_{INH}$
toN 100 ns typ R _L = 300 Ω, C _L = 35 pF, V _S = 8 V; see Figure 19 toFF 80 ns typ R _L = 300 Ω, C _L = 35 pF, V _S = 8 V; see Figure 19 Break-Before-Make Time Delay, t _D (ADG453 Only) 15 ns typ R _L = 300 Ω, C _L = 35 pF, V _S = 8 V; see Figure 19 Charge Injection 10 10 ns min Channel-to-Channel Crosstalk -90 dB typ V _S = 6 V, R _S = 0 Ω, C _L = 1.0 nF; see Figure 21 C _S (OFF) 60 pF typ f = 1 MHz C _D (OFF) 60 pF typ f = 1 MHz C _D , C _S (ON) 100 pF typ f = 1 MHz POWER REQUIREMENTS 0.0001 µA typ V _{DD} = 13.2 V; digital inputs = 0 V or 5 V I _D 0.0001 µA typ µA typ I _L 0.0001 µA typ µA typ			±0.5	μA max	
$t_{OFF} \\ t_{OFF} \\ t_{OFF} \\ t_{OFF} \\ t_{OD} \\ t_{OD}$	DYNAMIC CHARACTERISTICS ⁴				
toff 80 ns typ R _L = 300 Ω, C _L = 35 pF, V _S = 8 V; see Figure 19 Break-Before-Make Time Delay, t _D (ADG453 Only) 15 ns typ R _L = 300 Ω, C _L = 35 pF, V _{S1} = V _{S2} = 8 V; see Figure 20 10 10 ns min R _L = 300 Ω, C _L = 35 pF, V _{S1} = V _{S2} = 8 V; see Figure 20 Charge Injection 10 ns min PC typ V _S = 6 V, R _S = 0 Ω, C _L = 1.0 nF; see Figure 21 Channel-to-Channel Crosstalk -90 dB typ R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 23 C _S (OFF) 60 pF typ f = 1 MHz C _D (OFF) 60 pF typ f = 1 MHz C _D , C _S (ON) 100 pF typ f = 1 MHz POWER REQUIREMENTS V _{DD} = 13.2 V; digital inputs = 0 V or 5 V I _{DD} 0.5 5 μA typ I _L 0.0001 μA typ	ton	100		ns typ	$R_L = 300 \Omega$, $C_L = 35 pF$, $V_S = 8 V$; see Figure 19
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$		220	260	ns max	
Break-Before-Make Time Delay, t_D (ADG453 Only) 15 ns typ R _L = 300 Ω , C_L = 35 pF, V_{S1} = V_{S2} = 8 V; see Figure 20 10 10 ns min Charge Injection Channel-to-Channel Crosstalk C _S (OFF) C _D (OFF) C _D , C_S (ON) 100 POWER REQUIREMENTS I _{DD} R _L = 300 Ω , C_L = 35 pF, V_{S1} = V_{S2} = 8 V; see Figure 20 R _L = 50 Ω , C_L = 1.0 nF; see Figure 21 dB typ R _L = 50 Ω , C_L = 5 pF, f = 1 MHz; see Figure 23 pF typ f = 1 MHz f = 1 MHz V _{DD} = 13.2 V; digital inputs = 0 V or 5 V V _{DD} = 13.2 V; digital inputs = 0 V or 5 V µA typ I _D N	toff	80		ns typ	$R_L = 300 \Omega$, $C_L = 35 pF$, $V_S = 8 V$; see Figure 19
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		160	200	ns max	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Break-Before-Make Time Delay, t _D (ADG453 Only)	15		ns typ	
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$		10	10	ns min	j
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	Charge Injection			pC typ	$V_S = 6 \text{ V}, R_S = 0 \Omega, C_L = 1.0 \text{ nF}; \text{ see Figure 21}$
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$		-90			=
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Cs (OFF)	60			
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		60			f = 1 MHz
POWER REQUIREMENTS $I_{DD} \qquad 0.0001 \qquad \mu A \ typ \\ 0.5 \qquad 5 \qquad \mu A \ max \\ I_{L} \qquad 0.0001 \qquad \mu A \ typ$					
$\begin{array}{cccccccccccccccccccccccccccccccccccc$. //	$V_{DD} = 13.2 \text{ V}$; digital inputs = 0 V or 5 V
0.5 5 μA max I _L 0.0001 μA typ		0.0001		μΑ typ	, , , , , , , , , ,
I _L 0.0001 μA typ			5		
	l _L				
ν C.C = JV XbIII ΑΨ		0.5	5	μA max	$V_L = 5.5 \text{ V}$
I_{GND}^4 0.0001 μA typ	I_{GND}^4			-	
0.5 5 $\mu A \text{ max}$ $V_L = 5.5 \text{ V}$			5		$V_L = 5.5 V$

 $^{^1}$ Temperature range for B version is –40°C to +85°C. 2 T_{MAX} = 70°C.

³ Tested with dual supplies.

⁴ Guaranteed by design, not subject to production test.

5 V DUAL SUPPLY

 V_{DD} = +5 V, V_{SS} = -5 V, V_L = +5 V, GND = 0 V. All specifications T_{MIN} to T_{MAX} , unless otherwise noted.

	B Version ¹				
Parameter	25°C T _{MIN} to T _{MAX}		Unit	Test Conditions/Comments	
ANALOG SWITCH					
Analog Signal Range		$V_{\text{SS}}toV_{\text{DD}}$	V		
On Resistance (RoN)	7		Ωtyp	$V_D = -3.5 \text{ V to } +3.5 \text{ V, } I_S = -10 \text{ mA}$	
	12	15	Ω max		
On Resistance Match Between Channels (ΔR_{ON})	0.3		Ω typ	$V_D = 3.5 \text{ V, } I_S = -10 \text{ mA}$	
	0.5	0.5	Ω max		
LEAKAGE CURRENTS ^{2, 3}					
Source Off Leakage, Is (OFF)	±0.02		nA typ	$V_D = \pm 4.5$, $V_S = \pm 4.5$; see Figure 17	
	±0.5	±2.5	nA max		
Drain Off Leakage, I _D (OFF)	±0.02		nA typ	$V_D = 0 \text{ V}, 5 \text{ V}, V_S = 0 \text{ V}, 5 \text{ V}; \text{ see Figure 17}$	
	±0.5	±2.5	nA max		
Channel On Leakage, ID, IS (ON)	±0.04		nA typ	$V_D = V_S = 0 \text{ V}, 5 \text{ V}; \text{ see Figure 18}$	
	±1	±5	nA max		
DIGITAL INPUTS					
Input High Voltage, V _{INH}		2.4	V min		
Input Low Voltage, V _{INL}		8.0	V max		
Input Current, I _{INL} or I _{INH}	0.005		μA typ	$V_{IN} = V_{INL}$ or V_{INH}	
		±0.5	μA max		
DYNAMIC CHARACTERISTICS ⁴					
ton	160		ns typ	$R_L = 300 \Omega$, $C_L = 35 pF$, $V_S = 3 V$; see Figure 19	
	220	300	ns max		
toff	60		ns typ	$R_L = 300 \Omega$, $C_L = 35 pF$, $V_S = 3 V$; see Figure 19	
	140	180	ns max		
Break-Before-Make Time Delay, t _D (ADG453 Only)	50		ns typ	$R_L = 300 \Omega$, $C_L = 35 pF$, $V_{S1} = V_{S2} = 3 V$; see Figure 20	
	5	5	ns min		
Charge Injection	10		pC typ	$V_S = 0 \text{ V}, R_S = 0 \Omega, C_L = 1.0 \text{ nF}; \text{ see Figure 21}$	
Off Isolation	65		dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$; see Figure 22	
Channel-to-Channel Crosstalk	-76		dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$; see Figure 23	
C _s (OFF)	48		pF typ	f = 1 MHz	
C _D (OFF)	48		pF typ	f = 1 MHz	
C_D , C_S (ON)	148		pF typ	f = 1 MHz	
POWER REQUIREMENTS				$V_{DD} = 5.5 \text{ V}$; digital inputs = 0 V or 5 V	
I _{DD}	0.0001		μA typ		
	0.5	5	μA max		
Iss	0.0001		μA typ		
	0.5	5	μA max		
l _L	0.0001		μA typ		
	0.5	5	μA max	$V_L = 5.5 \text{ V}$	
I _{GND} ⁴	0.0001		μA typ		
	0.5	5	μA max	$V_L = 5.5 \text{ V}$	

 $^{^1}$ Temperature range for B version is -40°C to +85°C. 2 T_{MAX} = 70°C. 3 Tested with dual supplies. 4 Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

 $T_A = 25$ °C, unless otherwise noted.

Table 4.

Table 4.	
Parameters	Ratings
V _{DD} to V _{SS}	44 V
V_{DD} to GND	−0.3 V to +32 V
V _{SS} to GND	+0.3 V to -32 V
V _L to GND	$-0.3 \text{ V to V}_{DD} + 0.3 \text{ V}$
Analog, Digital Inputs ¹	$V_{SS} - 2V$ to $V_{DD} + 2V$ or 30 mA, whichever occurs first
Continuous Current, S or D	100 mA
Peak Current, S or D (pulsed at 1 ms, 10% duty cycle maximum)	300 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Plastic DIP Package, Power Dissipation	470 mW
θ_{JA} Thermal Impedance	117°C/W
Lead Temperature, Soldering (10 sec)	260°C
SOIC Package, Power Dissipation	600 mW
θ_{JA} Thermal Impedance	77°C/W
TSSOP Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	115°C/W
θ_{JC} Thermal Impedance	35°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD	2 kV

¹ Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

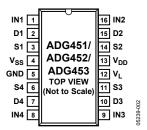


Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	IN1	Logic Control Input.
2	D1	Drain Terminal. Can be an input or an output.
3	S1	Source Terminal. Can be an input or an output.
4	V _{SS}	Most Negative Power Supply Potential in Dual Supplies. In single-supply applications, it can be connected to GND.
5	GND	Ground (0 V) Reference.
6	S4	Source Terminal. Can be an input or an output.
7	D4	Drain Terminal. Can be an input or an output.
8	IN4	Logic Control Input.
9	IN3	Logic Control Input.
10	D3	Drain Terminal. Can be an input or an output.
11	S3	Source Terminal. Can be an input or an output.
12	VL	Logic Power Supply (5 V).
13	V_{DD}	Most Positive Power Supply Potential.
14	S2	Source Terminal. Can be an input or an output.
15	D2	Drain Terminal. Can be an input or an output.
16	IN2	Logic Control Input.

Table 6. Truth Table (ADG451/ADG452)

ADG451 In	ADG452 In	Switch Condition
0	1	On
1	0	Off

Table 7. Truth Table (ADG453)

Logic	Switch 1, Switch 4	Switch 2, Switch 3
0	Off	On
1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

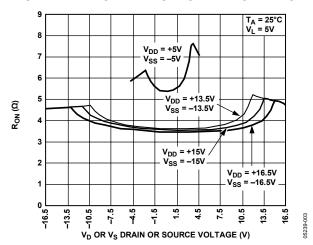


Figure 5. On Resistance as a Function of V_D (V_S) for Various Dual Supplies

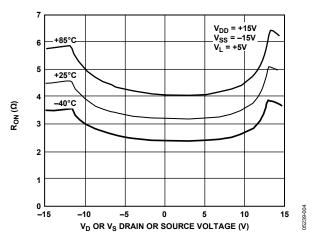


Figure 6. On Resistance as a Function of V_D (V_S) for Different Temperatures with Dual Supplies

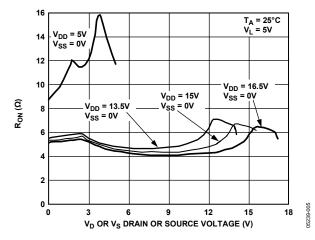


Figure 7. On Resistance as a Function of V_D (V_S) for Various Single Supplies

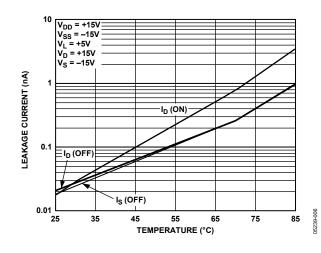


Figure 8. Leakage Currents as a Function of Temperature

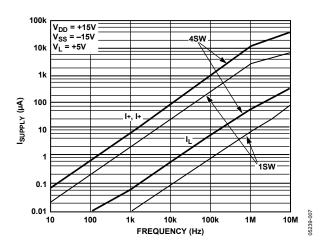


Figure 9. Supply Current vs. Input Switching Frequency

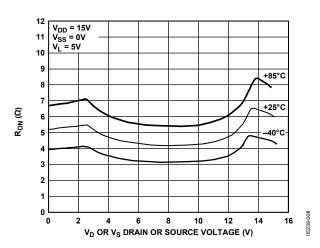


Figure 10. On Resistance as a Function of V_D (V_S) for Different Temperatures with Single Supplies

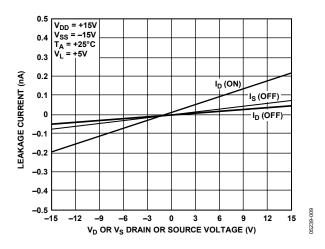


Figure 11. Leakage Currents as a Function of V_D (V_S)

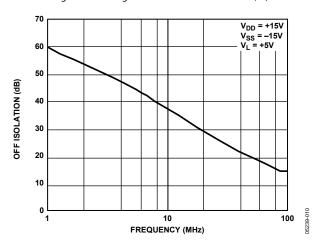


Figure 12. Off Isolation vs. Frequency

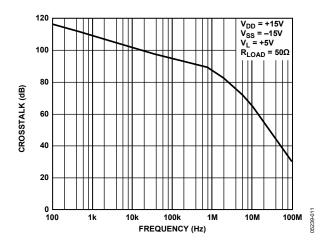


Figure 13. Crosstalk vs. Frequency

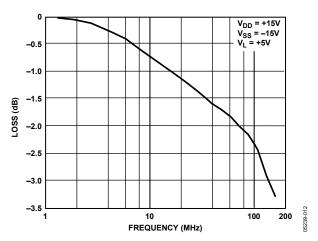


Figure 14. Frequency Response with Switch On

TERMINOLOGY

Ron

Ohmic resistance between D and S.

ΔR_{ON}

On resistance match between any two channels, that is, $R_{\rm ON}$ maximum minus $R_{\rm ON}$ minimum.

R_{FLAT(ON)}

Flatness is defined as the difference between the maximum and minimum value of on resistance, as measured over the specified analog signal range.

Is (OFF)

Source leakage current with the switch off.

I_D (OFF)

Drain leakage current with the switch off.

ID, Is (ON)

Channel leakage current with the switch on.

$V_D(V_S)$

Analog voltage on Terminal D and Terminal S.

Cs (OFF)

Off switch source capacitance.

C_D (OFF)

Off switch drain capacitance.

C_D (ON), C_S (ON)

On switch capacitance.

ton

Delay between applying the digital control input and the output switching on. See Figure 19.

toff

Delay between applying the digital control input and the output switching off.

\mathbf{t}_{D}

Off time or on time measured between the 90% points of both switches, when switching from one address state to another. See Figure 20.

Crosstalk

A measure of unwanted signal coupled through from one channel to another as a result of parasitic capacitance.

Off Isolation

A measure of unwanted signal coupling through an off switch.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

APPLICATIONS

Figure 15 illustrates a precise, fast, sample-and-hold circuit. An AD845 is used as the input buffer, and the output operational amplifier is an AD711. During track mode, SW1 is closed, and the output, V_{OUT} , follows the input signal, V_{IN} . In hold mode, SW1 is opened, and the signal is held by the hold capacitor, C_{H} .

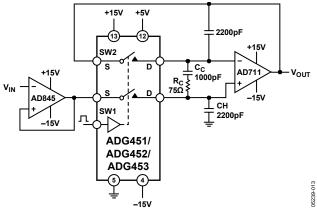


Figure 15. Fast, Accurate Sample-and-Hold Circuit

Due to switch and capacitor leakage, the voltage on the hold capacitor decreases with time. The ADG451/ADG452/ADG453 minimize this droop due to their low leakage specifications. The droop rate is further minimized by the use of a polystyrene hold capacitor. The droop rate for the circuit shown is typically 30 $\mu V/\mu s.$

A second switch, SW2, which operates in parallel with SW1, is included in this circuit to reduce pedestal error. Because both switches are at the same potential, they have a differential effect on the op amp, AD711, which minimizes charge injection effects. Pedestal error is also reduced by the compensation network, $R_{\rm C}$ and $C_{\rm C}$. This compensation network reduces the hold time glitch while optimizing the acquisition time. Using the illustrated op amps and component values, the pedestal error has a maximum value of 5 mV over the ± 10 V input range. Both the acquisition and settling times are 850 ns.

TEST CIRCUITS

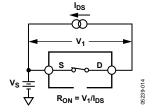


Figure 16. On Resistance

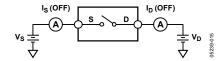


Figure 17. Off Leakage

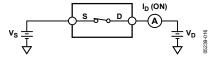


Figure 18. On Leakage

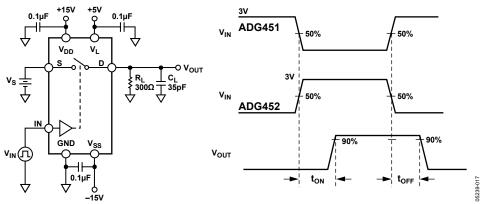
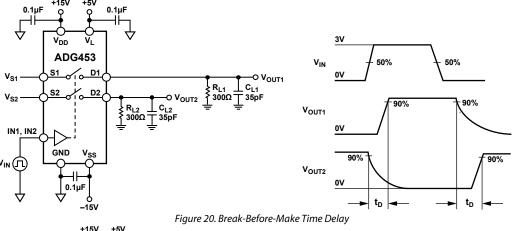


Figure 19. Switching Times



 $V_{S} = V_{OUT}$ $V_{IN} = C_{L} \times \Delta V_{OUT}$

Figure 21. Charge Injection

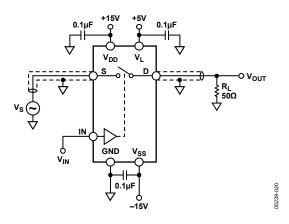


Figure 22. Off Isolation

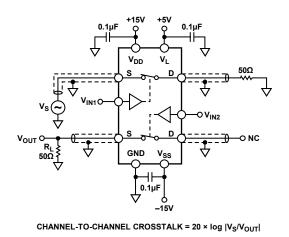
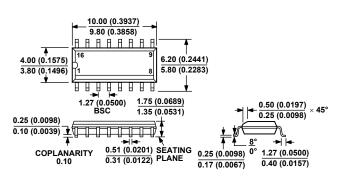


Figure 23. Channel-to-Channel Crosstalk

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AC

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 24. 16-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-16)

Dimensions shown in millimeters and (inches)

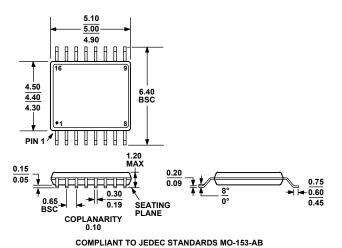
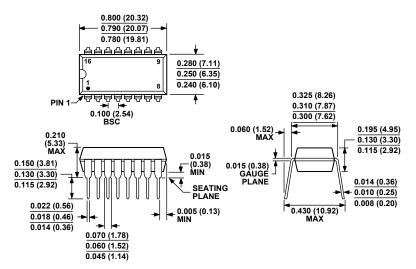


Figure 25. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-001-AB

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 26. 16-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-16)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG451BN	-40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
ADG451BNZ ¹	-40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
ADG451BR	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG451BR-REEL	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG451BR-REEL7	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG451BRZ ¹	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG451BRZ-REEL ¹	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG451BRZ-REEL7 ¹	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG451BRUZ ¹	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG451BRUZ- REEL ¹	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG451BRUZ- REEL71	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG451BCHIPS		DIE	
ADG452BN	-40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
ADG452BNZ ¹	−40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
ADG452BR	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG452BR-REEL	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG452BR-REEL7	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG452BRZ ¹	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG452BRZ-REEL ¹	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG452BRZ-REEL7 ¹	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG452BRUZ ¹	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG452BRUZ-REEL ¹	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG452BRUZ-REEL7 ¹	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG453BN	-40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
ADG453BNZ ¹	-40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
ADG453BR	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG453BR-REEL	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG453BR-REEL7	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG453BRZ ¹	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG453BRZ-REEL ¹	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG453BRZ-REEL7 ¹	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG453BRUZ ¹	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG453BRUZ-REEL ¹	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG453BRUZ-REEL7 ¹	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16

¹ Z = Pb-free part.



Rev. C | Page 16 of 16