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REVISION HISTORY

11/2019—Rev. B to Rev. C

Changes to Figure 12	9
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11/2016—Rev. A to Rev. B

Change to Serial Port Timing Section and Time From BCLK Falling Parameter; Table 7	10
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7/2013—Rev. 0 to Rev. A

Changes to Supply Current Test Conditions/Comments	3
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Added Figure 6; Renumbered Sequentially	6
Changes to Figure 14 and Figure 15	10
Changes to Figure 16, Figure 17, and Figure 18	11
Changes to Figure 19, Figure 20, and Figure 21	12

1/2013—Revision 0: Initial Version

SPECIFICATIONS

IOVDD = 1.8 V, T_A = 25°C, BCLK = 3.072 MHz, output = 48 kHz, I²S format, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL INPUT/OUTPUT					
High Level Input Voltage (V _{IH})			0.7 × IOVDD		V
Low Level Input Voltage (V _{IL})			0.3 × IOVDD		V
Input Leakage, High (I _{IH})	BCLK and LRCLK pins			1	μA
Input Leakage, Low (I _{IL})	BCLK and LRCLK pins			1	μA
Input Capacitance				5	pF
SDATA			4.5		mA
PDM_CLK			9		mA
PERFORMANCE					
Dynamic Range	20 Hz to 20 kHz, –60 dB input				
With A-Weighted Filter (RMS)			110		dB
Signal-to-Noise-Ratio	A-weighted, fourth-order input		110		dB
Decimation Ratio			64×		
Frequency Response	DC to 0.45 output f _s	–0.1		+0.01	dB
Stop Band			0.566		f _s
Stop-Band Attenuation		60			dB
Group Delay	0.02 f _s input signal		3.31		LRCLK cycles
Gain	PDM to PCM		0		dB
Start-Up Time			48		LRCLK cycles
Bit Width	Internal and output		20		Bits
Interchannel Phase			0		Degrees
CLOCKING					
Output Sampling Rate	f _s LRCLK pulse rate	4	48	96	kHz
BCLK Frequency	f _{BCLK}	0.256	3.072	24.576	MHz
POWER SUPPLIES					
Supply Voltage Range	IOVDD	1.62		3.6	V
Supply Current	IOVDD = 1.8 V		0.67		mA
	IOVDD = 3.3 V		1.33		mA
	IOVDD = 1.8 V, 16 kHz output		0.21		mA
	IOVDD = 3.3 V, 16 kHz output		0.41		mA
Shutdown Current	IOVDD _{SD} , no input clocks		1		μA

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
IOVDD Supply Voltage	3.6 V
Input Voltage	3.6 V
ESD Susceptibility	4 kV
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	–40°C to +85°C
Junction Temperature Range	–65°C to +165°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} (junction to air) is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. θ_{JA} is determined according to JESD51-9 on a 4-layer printed circuit board (PCB) with natural convection cooling.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
8-ball, 1.56 mm × 0.76 mm WLCSP	90	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

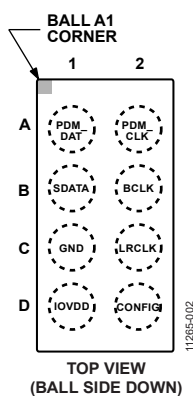


Figure 2. Pin Configuration (Top Side View)

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
A1	PDM_DAT	Input	PDM Data Input
A2	PDM_CLK	Output	PDM Clock Output
B1	SDATA	Output	Serial Data Output for I ² S/TDM
B2	BCLK	Input	Bit Clock for I ² S/TDM
C1	GND	Ground	Ground
C2	LRCLK	Input	Left/Right Clock for I ² S/Frame Sync for TDM
D1	IOVDD	Supply	Input/Output and Digital Supply
D2	CONFIG	Input	Configuration Pin

TYPICAL PERFORMANCE CHARACTERISTICS

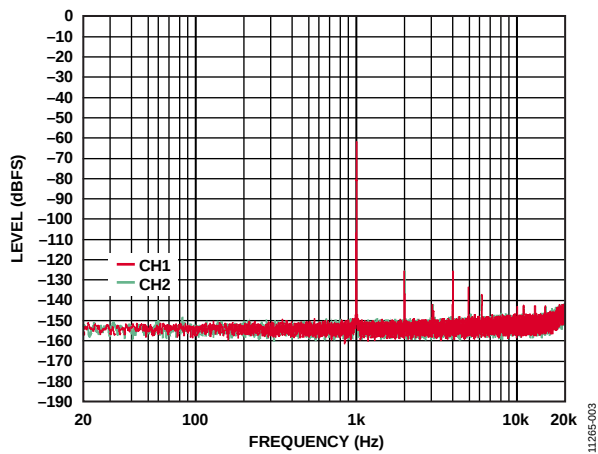


Figure 3. FFT, $f_s = 48$ kHz, -60 dBFS Input

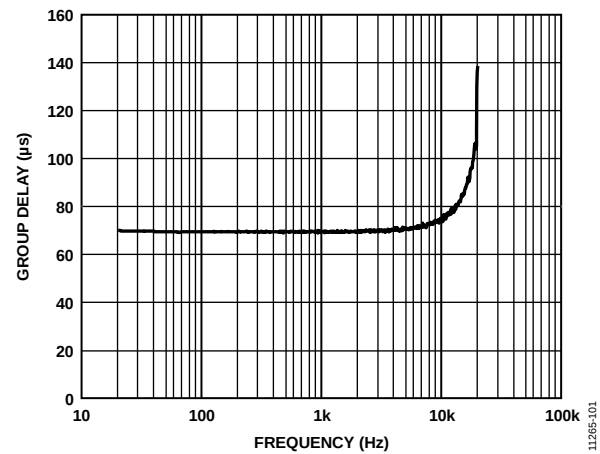


Figure 6. Group Delay vs. Frequency, $f_s = 48$ kHz

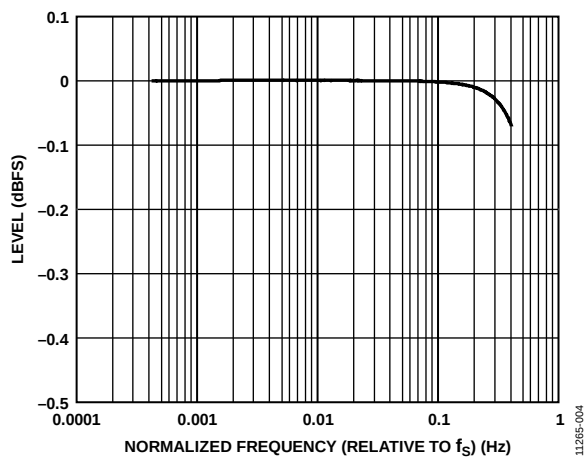


Figure 4. Frequency Response

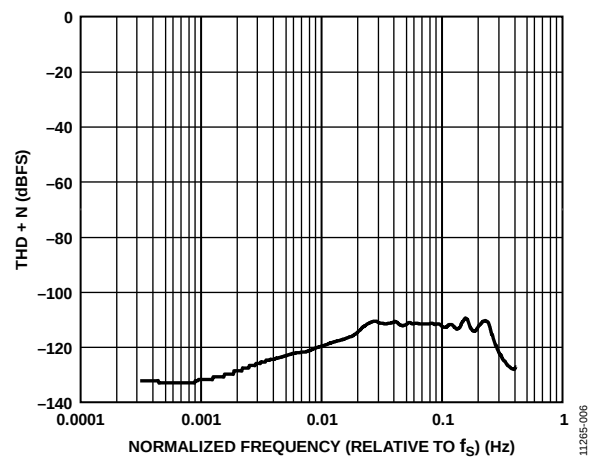


Figure 7. Total Harmonic Distortion + Noise (THD + N) vs. Normalized Frequency (Relative to f_s)

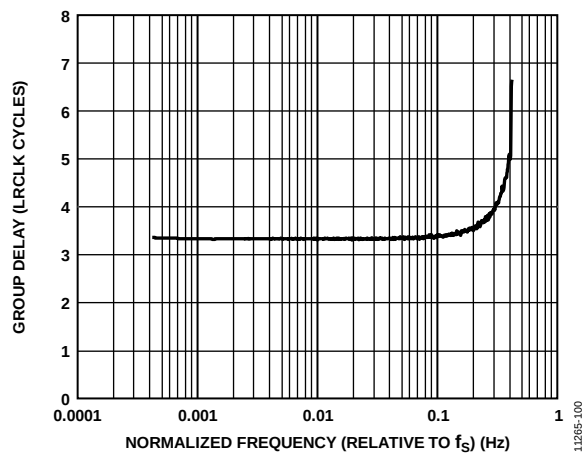


Figure 5. Group Delay vs. Normalized Frequency (Relative to f_s)

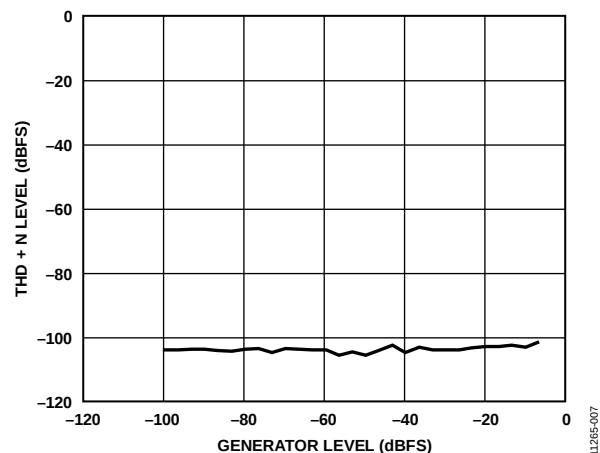


Figure 8. THD + N Level vs. Generator Level

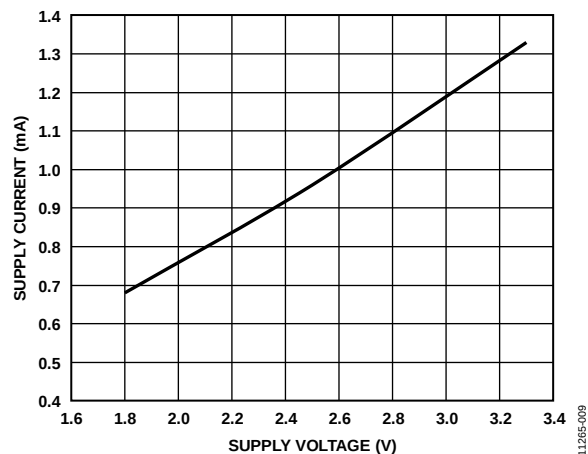


Figure 9. Supply Current vs. Supply Voltage

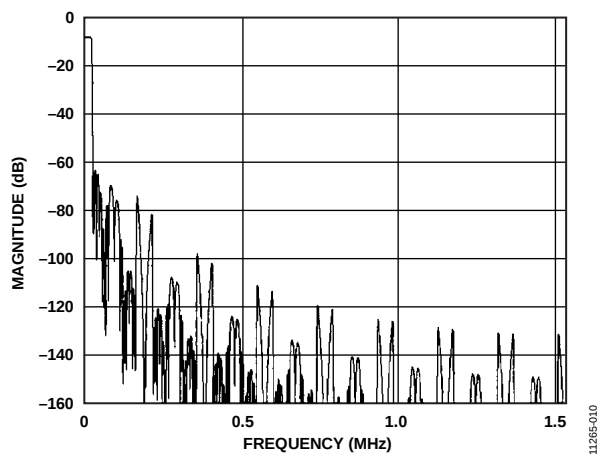


Figure 10. Out-of-Band Frequency Response (48 kHz Output)

TYPICAL APPLICATION CIRCUIT

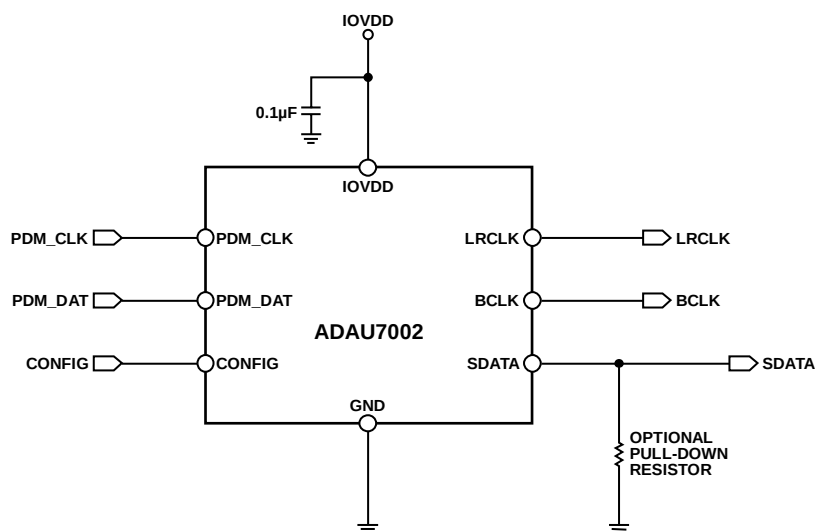


Figure 11. Typical Application Circuit

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APPLICATIONS INFORMATION

OVERVIEW

The [ADAU7002](#) provides stereo decimation from a 1-bit PDM source to a 20-bit PCM audio. The downsampling ratio is fixed at 64×. The 20-bit downsampled PCM audio is output via standard I²S or TDM formats.

The input source for the [ADAU7002](#) can be any device that has a PDM output, such as a digital microphone. The output pins of these microphones can connect directly to the input pins of the [ADAU7002](#).

CLOCKING

The [ADAU7002](#) requires a BCLK rate that is a minimum of 64× the LRCLK sample rate. BCLK rates of 128×, 192×, 256×, 384×, and 512× the LRCLK rate are also supported. The [ADAU7002](#) automatically detects the ratio between BCLK and LRCLK and generates a PDM clock output at 64× the LRCLK rate. The minimum sample rate is 4 kHz, and the maximum is 96 kHz, which correspond to a PDM clock range of 256 kHz to 6.144 MHz. Internally, all processing is done at the PDM_CLK rate.

When BCLK is removed, the [ADAU7002](#) powers down automatically. When BCLK is not present, the PDM_CLK output stops.

Table 5. PDM Timing Parameters

Parameter	t _{MIN}	t _{MAX}	Unit
Data Setup Time, t _{SETUP}	10		ns
Data Hold Time, t _{HOLD}	7		ns

PDM data is latched on both edges of the clock.

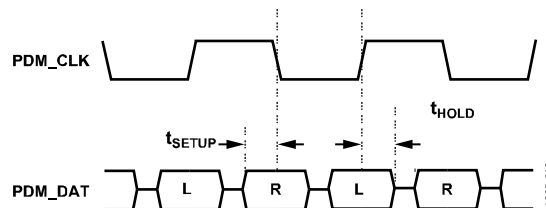


Figure 12. PDM Timing Diagram

SERIAL AUDIO OUTPUT INTERFACE

The [ADAU7002](#) supports I²S and TDM serial output formats. Format selection and TDM slot placement is set with the CONFIG pin. The SDATA pin is in tristate mode, except when the port is driving serial data based on the CONFIG pin configuration.

Table 6. TDM Slot Selection

Device Setting	CONFIG Pin Configuration
I ² S Format	Tie to IOVDD
TDM Slot 1 to Slot 2 Used/Driven, 32-Bit Slots	Tie to GND
TDM Slot 3 to Slot 4 Used/Driven, 32-Bit Slots	Open
TDM Slot 5 to Slot 6 Used/Driven, 32-Bit Slots	Tie to IOVDD through a 47 kΩ resistor
TDM Slot 7 to Slot 8 Used/Driven, 32-Bit Slots	Tie to GND through a 47 kΩ resistor

Serial Port Timing

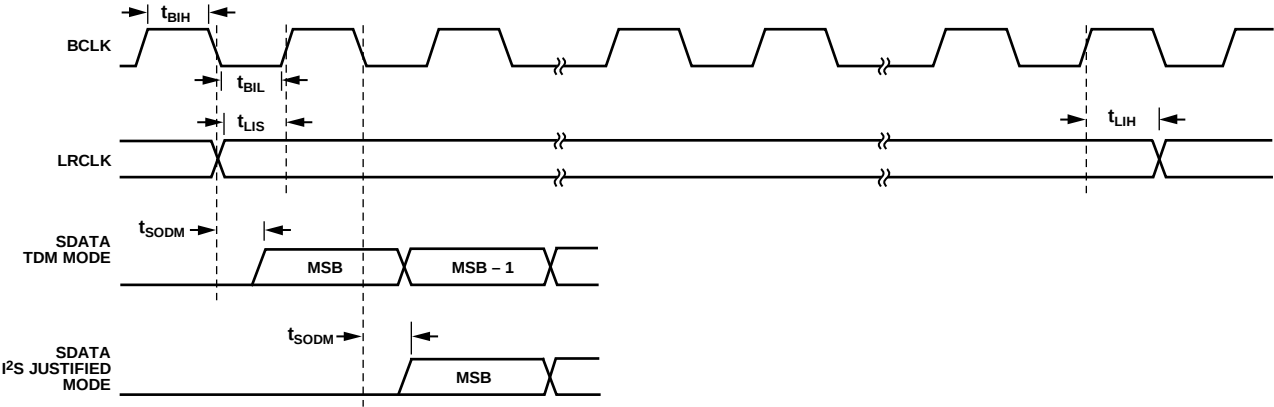


Figure 13. Serial Port Timing Diagram

IOVDD = 1.62 V to 3.63 V, load capacitance = 25 pF, unless otherwise noted.

Table 7. I²S/TDM Timing Parameters

Parameter	Symbol	t _{MIN}	t _{MAX}	Unit
BCLK Pulse Width High	t _{BIH}	10		ns
BCLK Pulse Width Low	t _{BIL}	10		ns
LRCLK Setup Time	t _{LIS}	10		ns
LRCLK Hold Time	t _{LIH}	10		ns
Time from BCLK Falling	t _{SODM}		18	ns

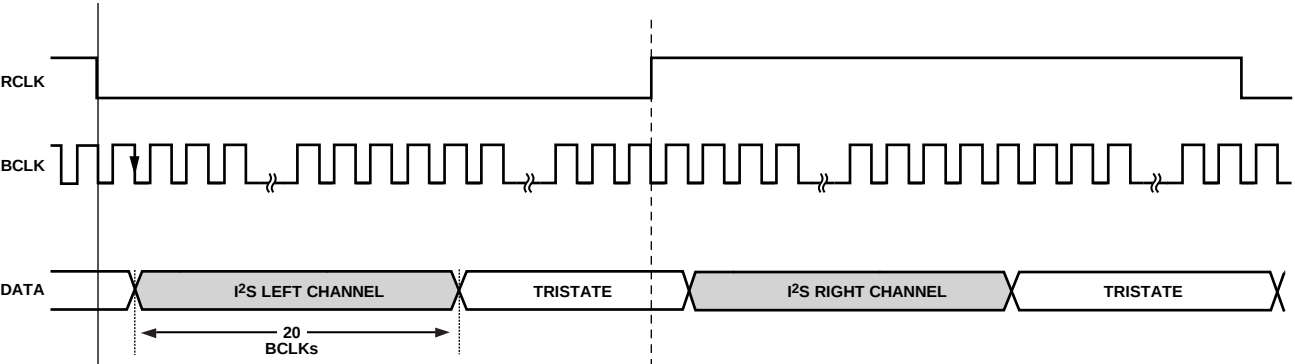


Figure 14. I²S, CONFIG Pin Tied to IOVDD

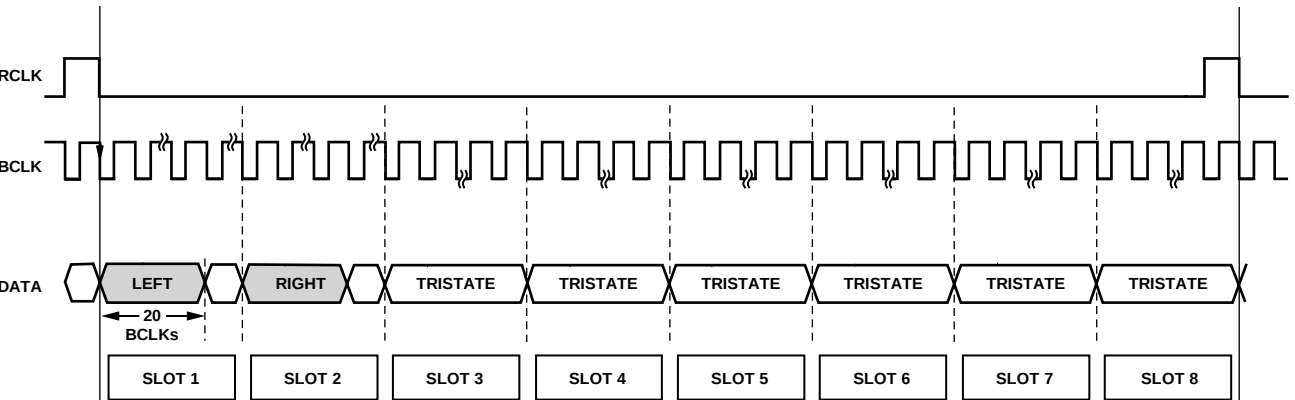


Figure 15. TDM8 Channel 1 and Channel 2, CONFIG Pin Tied to GND

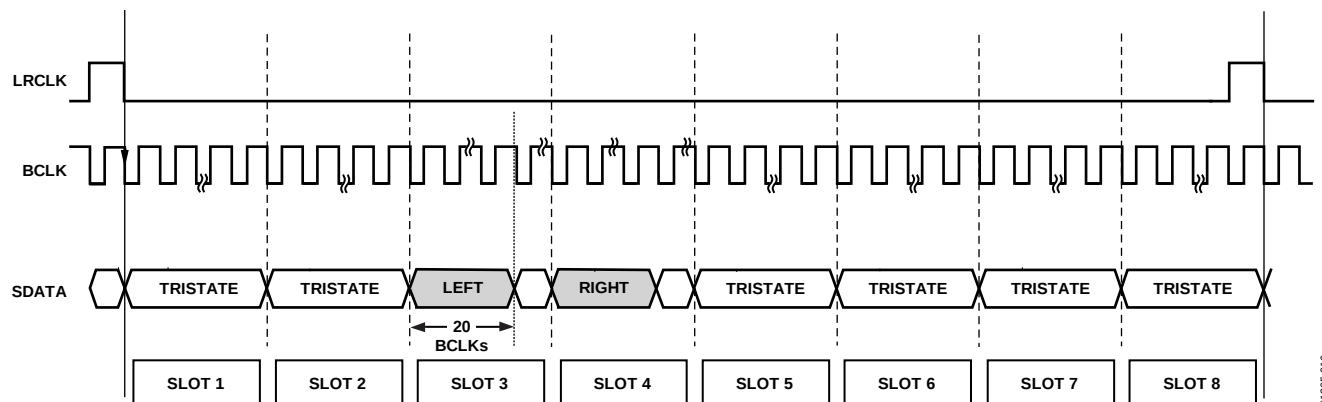


Figure 16. TDM8 Channel 3 and Channel 4, CONFIG Pin Open

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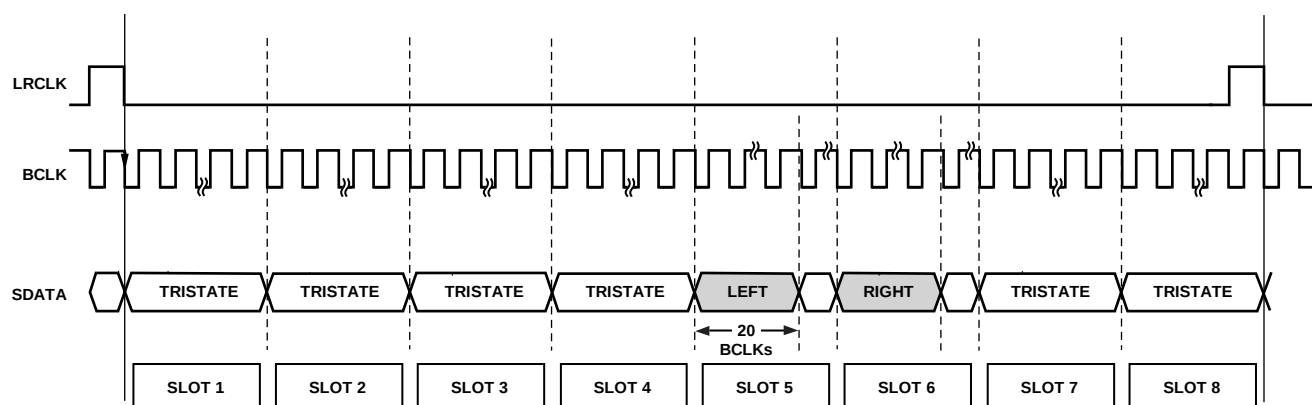


Figure 17. TDM8 Channel 5 to Channel 6, CONFIG Pin Tied to IOVDD Through a 47 kΩ Resistor

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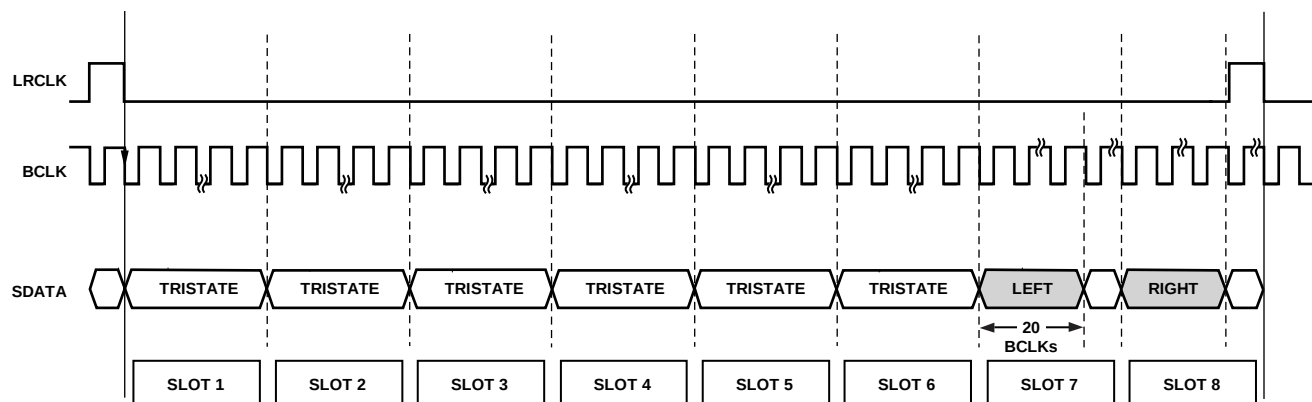


Figure 18. TDM8 Channel 7 and Channel 8, CONFIG Pin Tied to GND Through a 47 kΩ Resistor

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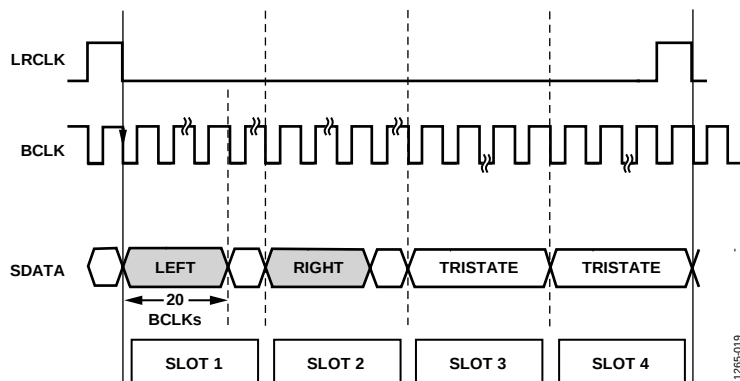


Figure 19. TDM4 Channel 1 and Channel 2, CONFIG Pin Tied to GND

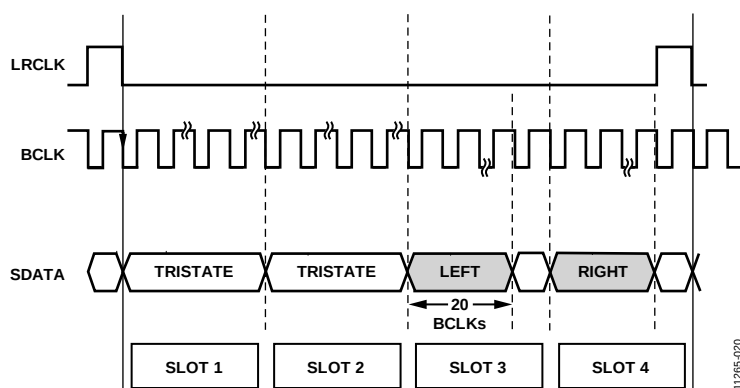


Figure 20. TDM4 Channel 3 and Channel 4, CONFIG Pin Open

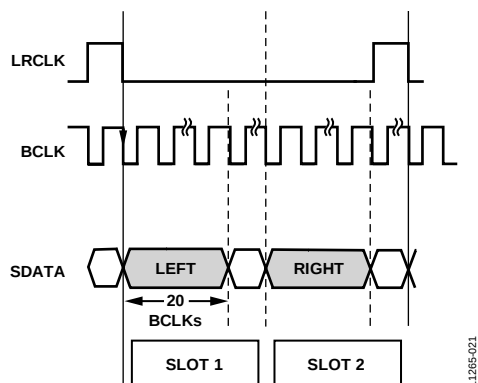


Figure 21. TDM2 Channel 1 and Channel 2, CONFIG Pin Tied to GND

OUTLINE DIMENSIONS

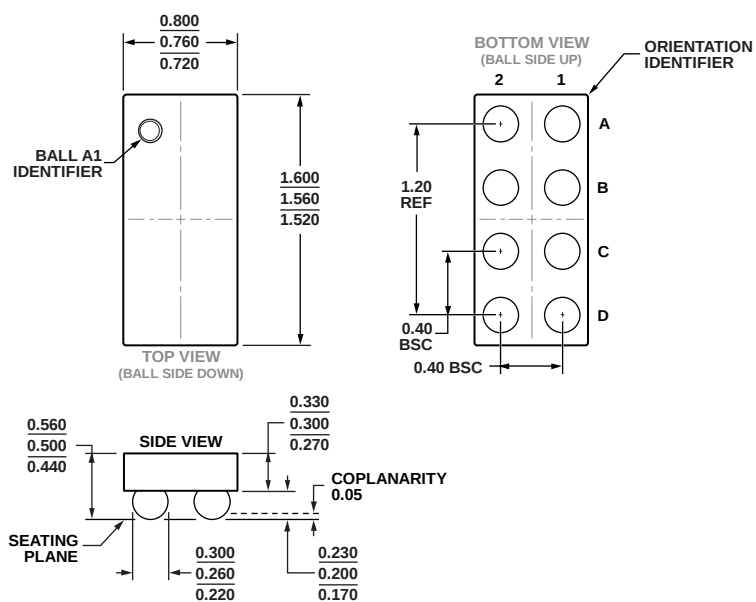


Figure 22. 8-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-8-6)

Dimensions shown in millimeters

10-18-2016-A

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Marking Code
ADAU7002ACBZ-R7	−40°C to +85°C	8-Ball Wafer Level Chip Scale Package [WLCSP], 7" Tape and Reel	CB-8-6	BE
ADAU7002ACBZ-RL	−40°C to +85°C	8-Ball Wafer Level Chip Scale Package [WLCSP], 13" Tape and Reel	CB-8-6	BE
EVAL-ADAU7002Z		Evaluation Board		

¹ Z = RoHS Compliant Part.

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