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REVISION HISTORY

8/07—Revision 0: Initial Version

SPECIFICATIONS

V_S = 12 V, R_F = 499 Ω (@ T_A = 25°C, G = +5, R_L = 100 Ω to V_S/2), unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} = 0.1 V p-p, PD1 = 0, PD0 = 0, R_{LOAD} = 50 Ω		310		MHz
	V_{OUT} = 0.1 V p-p, PD1 = 0, PD0 = 1, R_{LOAD} = 50 Ω		220		MHz
	V_{OUT} = 0.1 V p-p, PD1 = 1, PD0 = 0, R_{LOAD} = 50 Ω		140		MHz
Full Power Bandwidth	V_{OUT} = 10.2 V p-p, PD1 = 0, PD0 = 0, R_{LOAD} = 50 Ω		12.9		MHz
Slew Rate	V_{OUT} = 2 V p-p, PD1 = 0, PD0 = 0		1050		V/µs
	V_{OUT} = 2 V p-p, PD1 = 0, PD0 = 1		1050		V/µs
	V_{OUT} = 2 V p-p, PD1 = 1, PD0 = 0		1000		V/µs
NOISE/DISTORTION PERFORMANCE					
Differential Distortion (Worst Harmonic)	f_C = 1 MHz, V_{OUT} = 2 V p-p				
	PD1 = 0, PD0 = 0		−98		dBc
	PD1 = 0, PD0 = 1		−95		dBc
	PD1 = 1, PD0 = 0		−86		dBc
	f_C = 10 MHz, V_{OUT} = 2 V p-p				
	PD1 = 0, PD0 = 0		−72		dBc
	PD1 = 0, PD0 = 1		−63		dBc
	PD1 = 1, PD0 = 0		−52		dBc
	f_C = 20 MHz, V_{OUT} = 2 V p-p				
	PD1 = 0, PD0 = 0		−56		dBc
	PD1 = 0, PD0 = 1		−49		dBc
	PD1 = 1, PD0 = 0		−43		dBc
Input Voltage Noise	f = 100 kHz		2.4		nV/√Hz
Input Current Noise	f = 100 kHz		17		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage		−3	+1	+3	mV
Input Bias Current					
Noninverting Input		−9	−2	+3	µA
Inverting Input		−4	+4.5	+16	µA
Open-Loop Transimpedance	R_{LOAD} = 50 Ω	4	14		MΩ
	R_{LOAD} = 100 Ω	15	35		MΩ
Common-Mode Rejection		57	62		dB
INPUT CHARACTERISTICS					
Input Resistance	+IN, f < 100 kHz		500		kΩ
OUTPUT CHARACTERISTICS					
Single-Ended, +Swing	R_{LOAD} = 50 Ω	11	11.1		V_P
Single-Ended, −Swing	R_{LOAD} = 50 Ω		0.9	1	V_P
Single-Ended, +Swing	R_{LOAD} = 100 Ω	11	11.1		V_P
Single-Ended, −Swing	R_{LOAD} = 100 Ω		0.8	0.9	V_P
Differential Swing	R_{LOAD} = 100 Ω	20.2	20.6		V p-p
POWER SUPPLY					
Single Supply			12		V
Supply Current	PD1 = 0, PD0 = 0	10.5	11.8	13	mA/amp
	PD1 = 0, PD0 = 1	7	7.9	9	mA/amp
	PD1 = 1, PD0 = 0	4.3	5.2	6.3	mA/amp
	PD1 = 1, PD0 = 1		0.9	1.3	mA/amp

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER-DOWN PINS					
PD1, PD0 Threshold	Referenced to GND		1.5		V
High Level Input Voltage, V_{IH}		2		5	V
Low Level Input Voltage, V_{IL}		0		0.8	V
PD1, PD0 = 0 Pin Bias Current	PD1 or PD0 = 0 V	−1.5	−0.2	+1.5	µA
PD1, PD0 = 1 Pin Bias Current	PD1 or PD0 = 3 V	40	63	80	µA
Enable/Disable Time			130/116		ns
Power Supply Rejection Ratio		−63	−70		dB

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	13.6 V
Power Dissipation	$(T_{JMAX} - T_A)/\theta_{JA}$
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Thermal resistance (θ_{JA}) is specified for the worst-case conditions, that is, θ_{JA} is specified for device soldered in circuit board for surface-mount packages.

Table 3.

Package Type	θ_{JA}	Unit
10-Lead MINI_SO_EP	44	°C/W

Maximum Power Dissipation

The maximum safe power dissipation for the ADA4311-1 is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the amplifiers. Exceeding a junction temperature of 150°C for an extended period can result in changes in silicon devices, potentially causing degradation or loss of functionality.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 10-lead MINI_SO_EP (44°C/W) on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

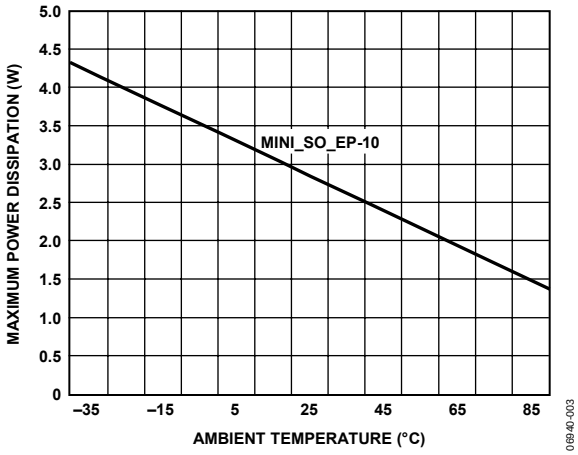

Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

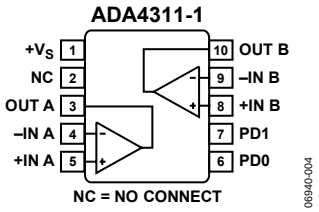

Figure 4. Pin Configuration

Table 4. Pin Function Description

Pin No.	Mnemonic	Description
1	$+V_S$	Positive Power Supply Input.
2	NC	No Connection.
3	OUT A	Amplifier A Output.
4	–IN A	Amplifier A Inverting Input.
5	+IN A	Amplifier A Noninverting Input.
6	PD0	Power Dissipation Control.
7	PD1	Power Dissipation Control.
8	+IN B	Amplifier B Noninverting Input.
9	–IN B	Amplifier B Inverting Input.
10	OUT B	Amplifier B Output.
11 (Exposed Paddle)	GND	Ground (Electrical Connection Required).

TYPICAL PERFORMANCE CHARACTERISTICS

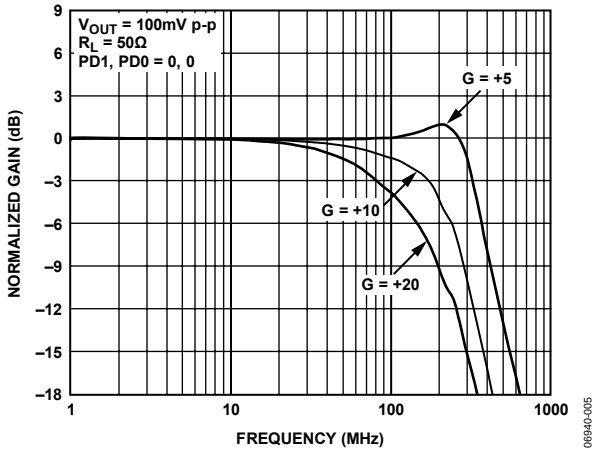

Figure 5. Small Signal Frequency Response for Various Closed-Loop Gains

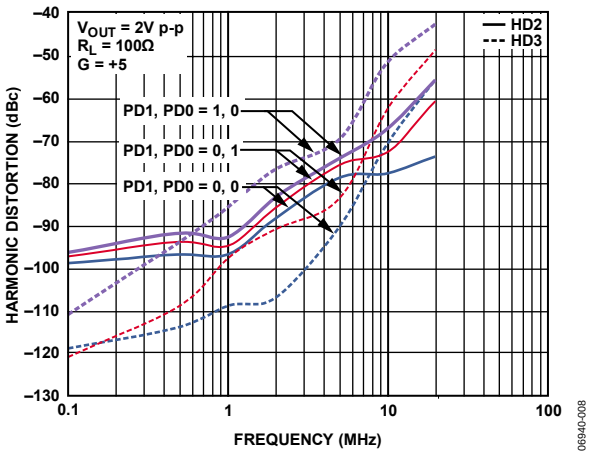

Figure 8. Differential Harmonic Distortion vs. Frequency

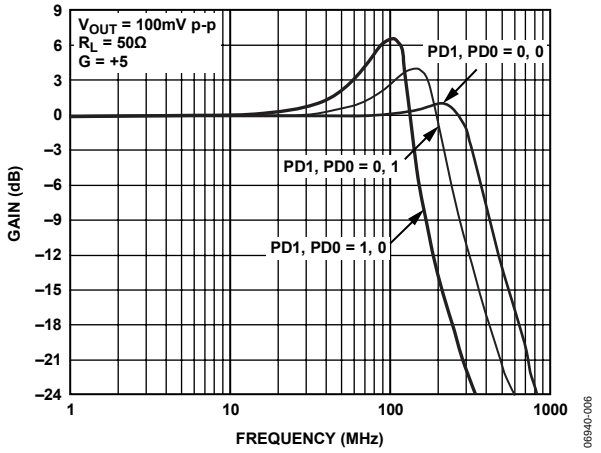

Figure 6. Small Signal Frequency Response for Various Modes

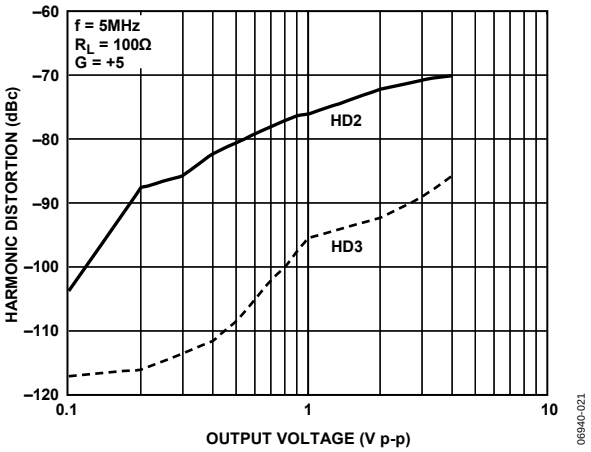

Figure 9. Differential Harmonic Distortion vs. Output Voltage

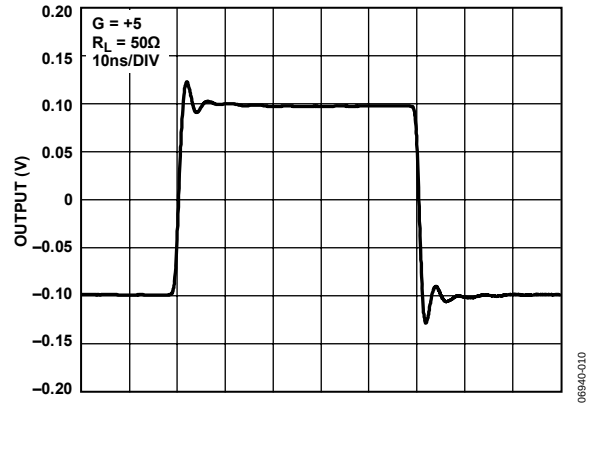

Figure 7. Small Signal Transient Response

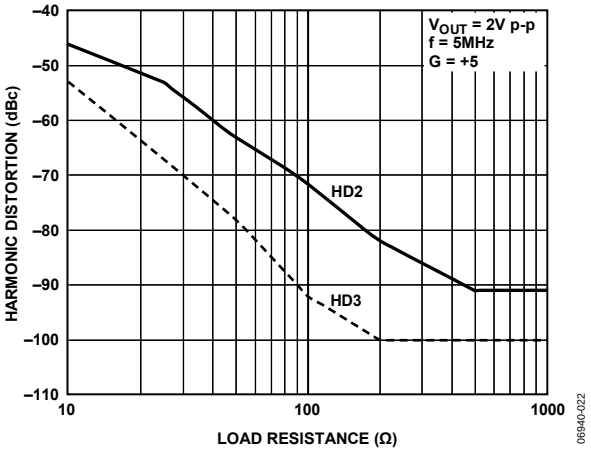

Figure 10. Differential Harmonic Distortion vs. Load Resistance

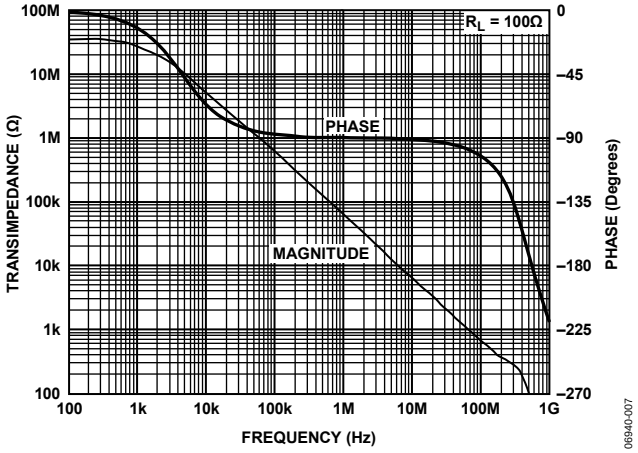

Figure 11. Open-Loop Transimpedance and Phase vs. Frequency

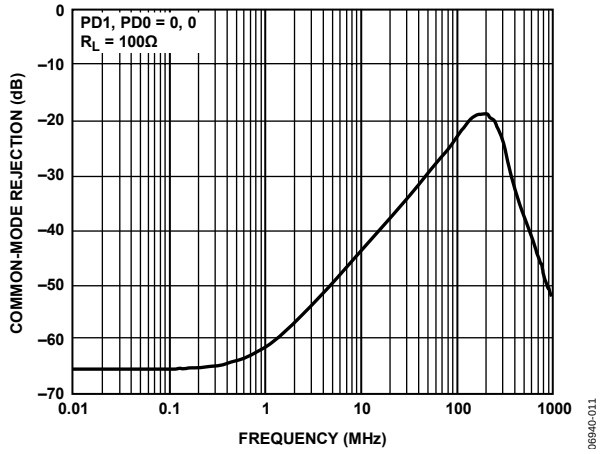

Figure 12. Common-Mode Rejection vs. Frequency

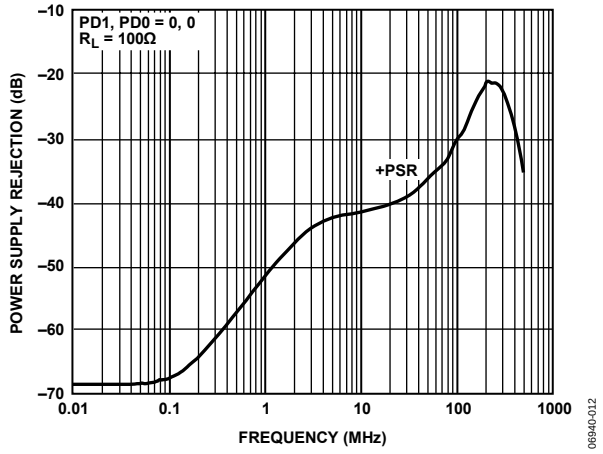

Figure 13. Power Supply Rejection vs. Frequency

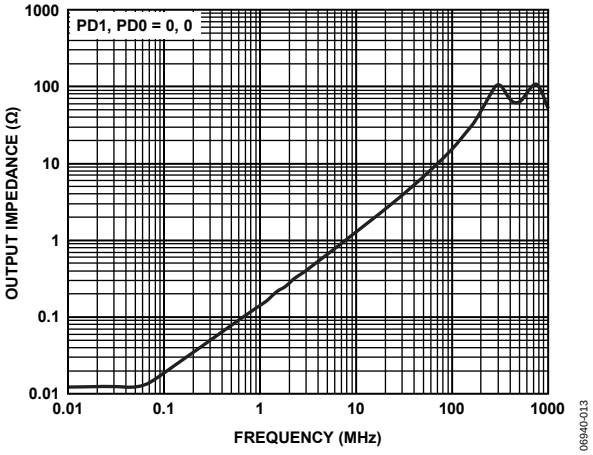

Figure 14. Closed-Loop Output Impedance vs. Frequency

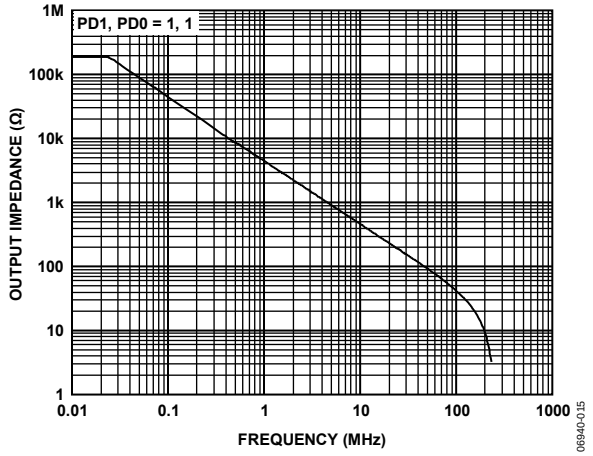

Figure 15. Output Impedance vs. Frequency (Disabled)

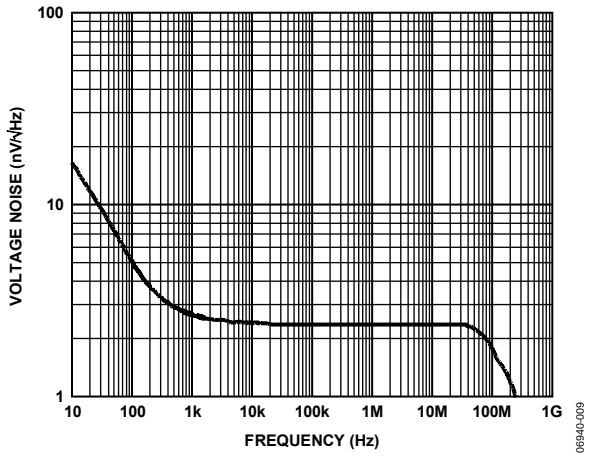

Figure 16. Voltage Noise vs. Frequency

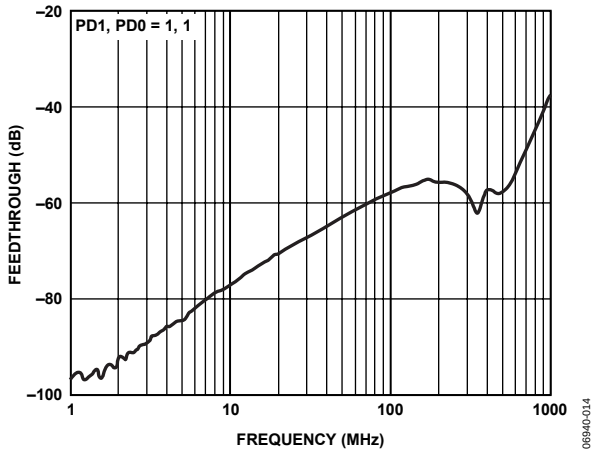

Figure 17. Feedthrough vs. Frequency

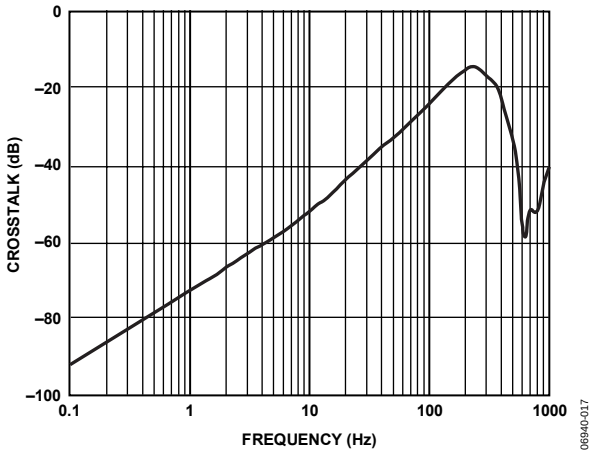

Figure 19. Crosstalk vs. Frequency

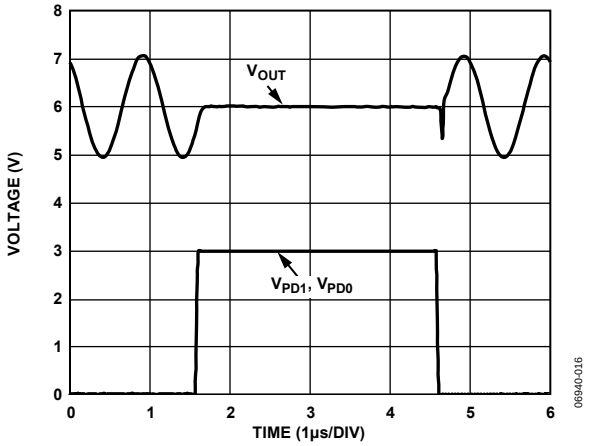

Figure 18. Power-Down Turn On/Turn Off

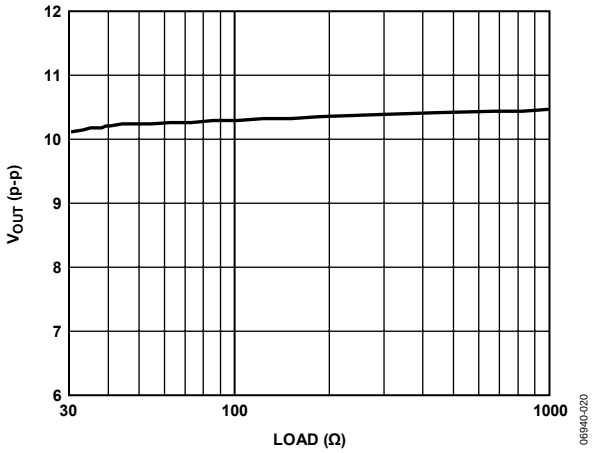

Figure 20. Single-Ended Output Swing vs. Load

THEORY OF OPERATION

The ADA4311-1 is a dual-current feedback amplifier with high output current capability. With a current feedback amplifier, the current into the inverting input is the feedback signal, and the open-loop behavior is that of a transimpedance, dV_O/dI_{IN} or T_Z.

The open-loop transimpedance is analogous to the open-loop voltage gain of a voltage feedback amplifier. Figure 21 shows a simplified model of a current feedback amplifier. Because R_{IN} is proportional to $1/g_m$, the equivalent voltage gain is $T_Z \times g_m$, where g_m is the transconductance of the input stage. Basic analysis of the follower with gain circuit yields

$$\frac{V_{OUT}}{V_{IN}} = G \times \frac{T_Z(s)}{T_Z(s) + G \times R_{IN} + R_F}$$

where:

$$G = 1 + \frac{R_F}{R_G}$$

$$R_{IN} = \frac{1}{g_m} \approx 50\ \Omega$$

Because $G \times R_{IN} << R_F$ for low gains, a current feedback amplifier has relatively constant bandwidth vs. gain, the 3 dB point being set when $|T_Z| = R_F$.

For a real amplifier, there are additional poles that contribute excess phase, and there is a value for R_F below which the amplifier is unstable. Tolerance for peaking and desired flatness determines the optimum R_F in each application.

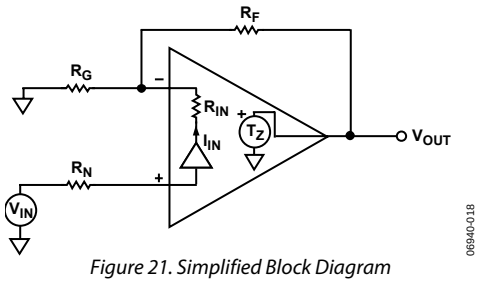

Figure 21. Simplified Block Diagram

APPLICATION INFORMATION

FEEDBACK RESISTOR SELECTION

The feedback resistor has a direct impact on the closed-loop bandwidth and stability of the current feedback op amp. Reducing the resistance below the recommended value can make the amplifier response peak and even become unstable. Increasing the size of the feedback resistor beyond the recommended value reduces the closed-loop bandwidth. Table 5 provides a convenient reference for quickly determining the feedback and gain resistor values, and the corresponding bandwidth, for common gain configurations. The recommended feedback resistor value for the ADA4311-1 is 499 Ω.

Table 5. Recommended Values and Frequency Performance[1]

Gain	R_F (Ω)	R_G (Ω)	−3 dB SS BW (MHz)
+5	499	124	310
+5	1 k	250	220
+10	499	55.4	175
+20	499	26.1	84

[1] Conditions: V_S = ±12 V, T_A = 25°C, R_L = 50 Ω, PD1, PD0 = 0, 0.

POWER CONTROL MODES OF OPERATION

The ADA4311-1 features four power modes: full power, ¾ power, ½ power, and shutdown. The power modes are controlled by two logic pins, PD0 and PD1. The power-down control pins are compatible with standard 3 V and 5 V CMOS logic. Table 6 shows the various power modes and associated logic states. In the power-down mode, the output of the amplifier goes into a high impedance state.

Table 6. Power Modes

PD1	PD0	Power Mode	Total Supply Current (mA)	Output Impedance
Low	Low	Full Power	23.6	Low
Low	High	¾ Power	15.8	Low
High	Low	½ Power	10.4	Low
High	High	Power-Down	1.8	High

EXPOSED THERMAL PAD CONNECTIONS

The exposed thermal pad on the 10-lead MSOP is both the reference for the PD pins and the only electrical connection for the negative supply voltage. Therefore, in the 10-lead MSOP, the ADA4311-1 can only be used on a single supply. The exposed thermal pad must be connected to ground. Failure to do so renders the part inoperable.

A requirement for this package is that the thermal pad be connected to a solid plane with low thermal resistance, ensuring adequate heat transfer away from the die and into the board.

POWERLINE APPLICATION

Applications (that is, powerline AV modems) requiring greater than 10 dBm peak power should consider using an external line driver, such as the ADA4311-1. Figure 22 shows an example interface between the TxDAC® output and the ADA4311-1 biased for single-supply operation. The peak-to-peak differential output voltage swing of the TxDAC should be limited to 2 V p-p, with the gain of the ADA4311-1 configured to realize the additional voltage gain required by the application. A low-pass filter should be considered to filter the DAC images inherent in the signal reconstruction process. In addition, dc blocking capacitors are required to level-shift the output signal of the TxDAC to the common-mode level of the ADA4311-1 (that is, $V_{MID} = V_{CC} - GND/2$).

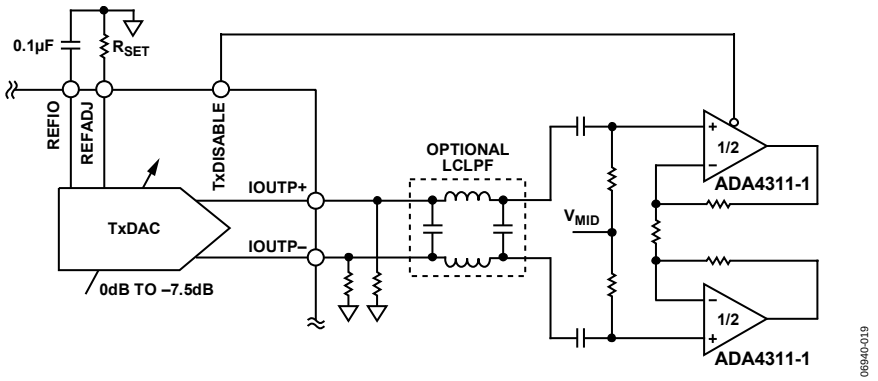

Figure 22. TxDAC Output Directly via Center-Tap Transformer

BOARD LAYOUT

As is the case with all high speed applications, careful attention to printed circuit board (PCB) layout details prevents associated board parasitics from becoming problematic. Proper RF design technique is mandatory. The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance return path. Removing the ground plane on all layers from the area near the input and output pins reduces stray capacitance, particularly in the area of the inverting inputs. Signal lines connecting the feedback and gain resistors should be as short as possible to minimize the inductance and stray capacitance associated with these traces. Termination resistors and loads should be located as close as possible to their respective inputs and outputs. Input and output traces should be kept as far apart as possible to minimize coupling (crosstalk) though the board. Wherever there are complementary signals, a symmetrical layout should be provided to the extent possible to maximize balanced performance. When running differential signals over a long distance, the traces on the PCB should be close. Doing this reduces the radiated energy and makes the circuit less susceptible to RF interference. Adherence to stripline design techniques for long signal traces (greater than about 1 inch) is recommended.

For more information on high speed board layout, see *A Practical Guide to High-Speed Printed-Circuit-Board Layout*.

POWER SUPPLY BYPASSING

The ADA4311-1 operates on supplies from 6 V to 12 V. The ADA4311-1 circuit should be powered with a well-regulated power supply. Careful attention must be paid to decoupling the power supply. High quality capacitors with low equivalent series resistance (ESR), such as multilayer ceramic capacitors (MLCCs), should be used to minimize supply voltage ripple and power dissipation. In addition, 0.1 µF MLCC decoupling capacitors should be located no more than ⅛-inch away from each of the power supply pins. A large, usually tantalum, 10 µF capacitor is required to provide good decoupling for lower frequency signals and to supply current for fast, large signal changes at the ADA4311-1 outputs. Bypassing capacitors should be laid out in such a manner as to keep return currents away from the inputs of the amplifiers, which minimizes any voltage drops that can develop due to ground currents flowing through the ground plane. A large ground plane also provides a low impedance path for the return currents.

OUTLINE DIMENSIONS

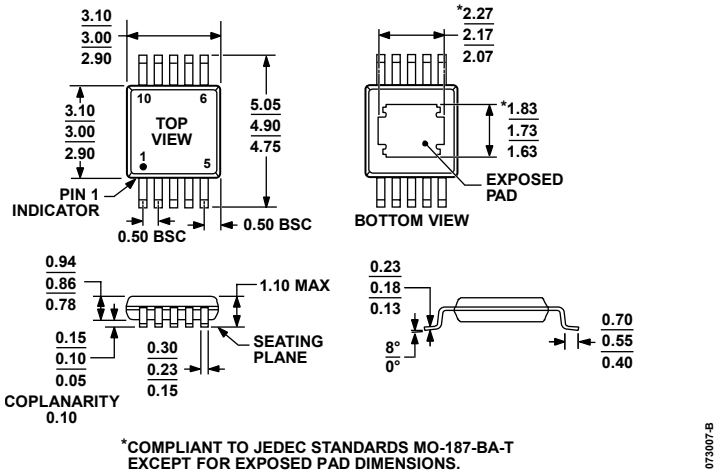

Figure 23. 10-Lead Mini Small Outline Package with Exposed Pad [MINI_SO_EP]
(RH-10-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADA4311-1ARHZ[1]	−40°C to +85°C	10-Lead Mini Small Outline Package with Exposed Pad [MINI_SO_EP]	RH-10-1	1A
ADA4311-1ARHZ-RL[1]	−40°C to +85°C	10-Lead Mini Small Outline Package with Exposed Pad [MINI_SO_EP]	RH-10-1	1A
ADA4311-1ARHZ-R7[1]	−40°C to +85°C	10-Lead Mini Small Outline Package with Exposed Pad [MINI_SO_EP]	RH-10-1	1A

[1] Z = RoHS Compliant Part.

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