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REVISION HISTORY

8/04—Data sheet changed from Rev. A to Rev. B
Changes to Table 5 ... 16

4/01—Data sheet changed from Rev. 0 to Rev. A
Updated Format ... Universal
Changes to TPC 2 ... 8
Added Figures 41 to 46 ... 23

7/99—Revision 0: Initial Version

SPECIFICATIONS

AVDD = 3 V, DRVDD = 3 V, F_S = 40 MSPS, input span from 0.5 V to 2.5 V, internal 1 V reference, PWRCON = AVDD, 50% clock duty cycle, T_{MIN} to T_{MAX} unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
RESOLUTION			10		Bits	
MAX CONVERSION RATE	F_S	40			MSPS	
PIPELINE DELAY				5.5	Clock Cycles	
DC ACCURACY						
Differential Nonlinearity	DNL		± 0.25 ± 0.7	LSB		
Integral Nonlinearity	INL		± 0.65 ± 1.4	LSB		
Offset Error	E_{ZS}		± 0.6 ± 2.8	% FSR		
Gain Error	E_{FS}		± 0.7 ± 4.0	% FSR		
ANALOG INPUT						
Input Voltage Range	AIN	1		2	V p-p	
Input Capacitance	C_{IN}		1.4		pF	
Aperture Delay	T_{AP}		2.0		ns	
Aperture Uncertainty (Jitter)	T_{AJ}		1.2		ps rms	
Input Bandwidth (–3 dB)	BW		390		MHz	
Input Referred Noise			0.3		mV	Switched, Single-Ended
INTERNAL REFERENCE						
Output Voltage (0.5 V Mode)	VREF		0.5		V	REFSENSE = VREF
Output Voltage (1 V Mode)	VREF		1		V	REFSENSE = GND
Output Voltage Tolerance (1 V Mode)			± 5	± 30	mV	
Load Regulation			0.65	1.2	mV	1.0 mA Load
POWER SUPPLY						
Operating Voltage	AVDD	2.7	3.0	3.6	V	
	DRVDD	2.7	3.0	3.6	V	
Analog Supply Current	IAVDD		20.1	22.0	mA	
Digital Supply Current	IDRVDD		4.4	6.0	mA	f_{IN}= 4.8 MHz, Output Bus Load = 10pF
			9.5	14.0	mA	f_{IN}= 20 MHz, Output Bus Load = 20 pF
Power Consumption			74	84.0	mW	f_{IN}= 4.8 MHz, Output Bus Load = 10pF
			88.8	108.0	mW	f_{IN}= 20 MHz, Output Bus Load = 20 pF
Power-Down	P_D		0.65	1.2	mW	
Power Supply Rejection Ratio	PSRR		0.04	± 0.25	% F_S	
DYNAMIC PERFORMANCE (AIN = 0.5 dBFS)						
Signal-to-Noise and Distortion	SINAD					
f = 4.8 MHz			59.7		dB	
f = 20 MHz		57.2	59.3		dB	
Effective Bits	ENOB					
f = 4.8 MHz			9.6		Bits	
f = 20 MHz		9.2	9.55		Bits	
Signal-to-Noise Ratio	SNR					
f = 4.8 MHz			60.0		dB	
f = 20 MHz		57.5	59.5		dB	
Total Harmonic Distortion	THD					
f = 4.8MHz			–76.0		dB	
f = 20 MHz			–74.0	–65.0	dB	
Spurious-Free Dynamic Range	SFDR					
f = 4.8 MHz[1]			80		dB	
f = 20 MHz		67.8	78		dB	

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Two-Tone Intermodulation Distortion	IMD		68		dB	f = 44.49 MHz and 45.52 MHz
Differential Phase	DP		0.2		Degree	NTSC 40 IRE Ramp
Differential Gain	DG		0.3		%	
DIGITAL INPUTS						
High Input Voltage	V_{IH}	2.0			V	
Low Input Voltage	V_{IL}			0.4	V	
Clock Pulse Width High		11.25			ns	
Clock Pulse Width Low		11.25			ns	
Clock Period[2]			25		ns	
DIGITAL OUTPUTS						
High-Z Leakage	I_{OZ}			± 5.0	µA	Output = 0 to DRVDD
Data Valid Delay	t_{OD}		5		ns	C_L= 20 pF
Data Enable Delay	t_{DEN}		6		ns	C_L= 20 pF
Data High-Z Delay	t_{DHZ}		6		ns	C_L= 20 pF
LOGIC OUTPUT (with DRVDD = 3 V)						
High Level Output Voltage (I_{OH} = 50 µA)	V_{OH}	2.95			V	
High Level Output Voltage (I_{OH} = 0.5 mA)	V_{OH}	2.80			V	
Low Level Output Voltage (I_{OL}= 1.6 mA)	V_{OL}			0.3	V	
Low Level Output Voltage (I_{OL}= 50 µA)	V_{OL}			0.05	V	

[1] Differential Input (2 V p-p).
[2] The AD9203 will convert at clock rates as low as 20 kHz.

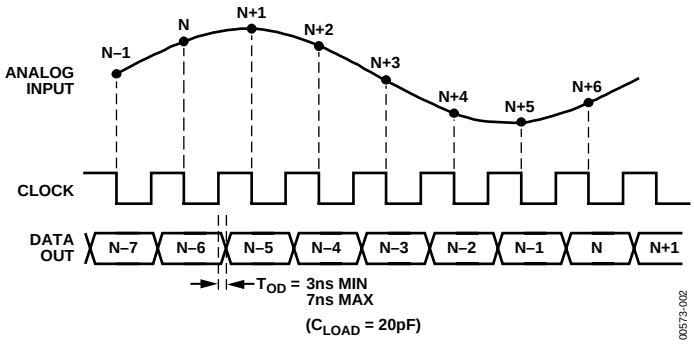

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	With Respect to	Min	Max	Unit
AVDD	AVSS	–0.3	+3.9	V
DRVDD	DRVSS	–0.3	+3.9	V
AVSS	DRVSS	–0.3	+0.3	V
AVDD	DRVDD	–3.9	+3.9	V
REFCOM	AVSS	–0.3	+0.3	V
CLK	AVSS	–0.3	AVDD + 0.3	V
Digital Outputs	DRVSS	–0.3	DRVDD + 0.3	V
AINP	AINN	AVSS –0.3	AVDD + 0.3	V
VREF	AVSS	–0.3	AVDD + 0.3	V
REFSENSE	AVSS	–0.3	AVDD + 0.3	V
REFTF, REFBF	AVSS	–0.3	AVDD + 0.3	V
STBY	AVSS	–0.3	AVDD + 0.3	V
CLAMP	AVSS	–0.3	AVDD + 0.3	V
CLAMPIN	AVSS	–0.3	AVDD + 0.3	V
PWRCON	AVSS	–0.3	AVDD + 0.3	V
DFS	AVSS	–0.3	AVDD + 0.3	V
3-STATE	AVSS	–0.3	AVDD + 0.3	V
Junction Temperature			150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 s)			300	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

28-Lead TSSOP

θ_{JA} = 97.9°C/W

θ_{JC} = 14.0°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

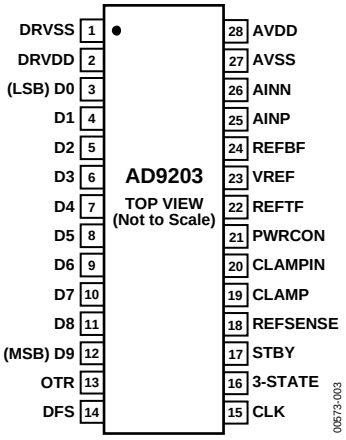

Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin	Name	Description
1	DRVSS	Digital Ground.
2	DRVDD	Digital Supply.
3	D0	Bit 0, Least Significant Bit.
4	D1	Bit 1.
5	D2	Bit 2.
6	D3	Bit 3.
7	D4	Bit 4.
8	D5	Bit 5.
9	D6	Bit 6.
10	D7	Bit 7.
11	D8	Bit 8.
12	D9	Bit 9, Most Significant Bit.
13	OTR	Out-of-Range Indicator.
14	DFS	Data Format Select HI: Twos Complement; LO: Straight Binary.
15	CLK	Clock Input.
16	3-STATE	HI: High Impedance State Output; LO: Active Digital Output Drives.
17	STBY	HI: Power-Down Mode; LO: Normal Operation.
18	REFSENSE	Reference Select.
19	CLAMP	HI: Enable Clamp; LO: Open Clamp.
20	CLAMPIN	Clamp Signal Input.
21	PWRCON	Power Control Input.
22	REFTF	Top Reference Decoupling.
23	VREF	Reference In/Out.
24	REFBF	Bottom Reference Decoupling.
25	AINP	Noninverting Analog Input.
26	AINN	Inverting Analog Input.
27	AVSS	Analog Ground.
28	AVDD	Analog Supply.

TERMINOLOGY

Integral Nonlinearity Error (INL)
Linearity error refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs 1/2 LSB before the first code transition. Positive full scale is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

Differential Nonlinearity Error (DNL, No Missing Codes)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 10-bit resolution indicates that all 1024 codes respectively, must be present over all operating ranges.

Signal-To-Noise and Distortion (S/N+D, SINAD) Ratio
S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

Effective Number of Bits (ENOB)
For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

$$N = (SINAD - 1.76)/6.02$$

it is possible to get a measure of performance expressed as N, the effective number of bits.

Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

Signal-To-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)
The difference in dB between the rms amplitude of the input signal and the peak spurious signal.

Offset Error
First transition should occur for an analog value 1/2 LSB above negative full scale. Offset error is defined as the deviation of the actual transition from that point.

Gain Error
The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur for an analog value 1 1/2 LSB below the positive full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

Power Supply Rejection
The specification shows the maximum change in full scale from the value with the supply at the minimum limit to the value with the supply at its maximum limit.

Aperture Jitter
Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the A/D.

Aperture Delay
Aperture delay is a measure of the sample-and-hold amplifier (SHA) performance and is measured from the rising edge of the clock input to when the input signal is held for conversion.

Pipeline Delay (Latency)
The number of clock cycles between conversion initiation and the associated output data being made available. New output data is provided on every rising edge.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 3 V, DRVDD = 3 V, F_S = 40 MSPS, 1 V Internal Reference, PWRCON = AVDD, 50% Duty Cycle, unless otherwise noted.

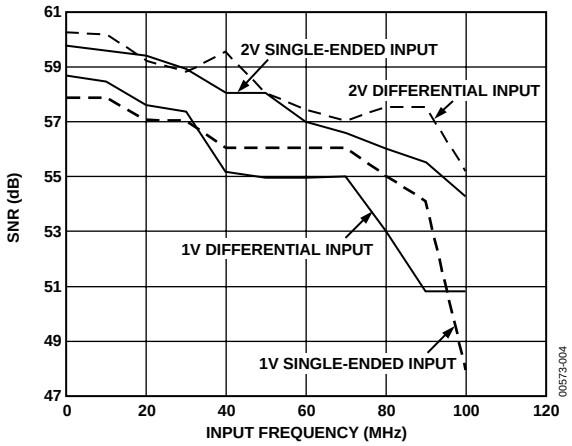

Figure 4. SNR vs. Input Frequency and Configuration

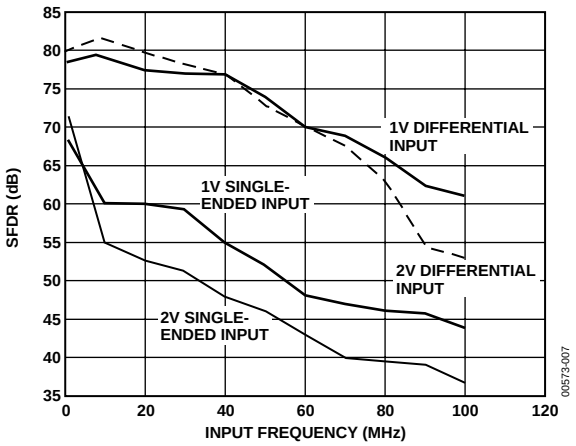

Figure 7. SFDR vs. Input Frequency and Configuration

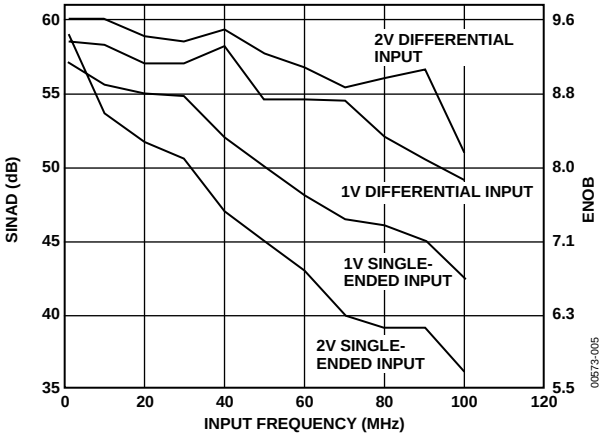

Figure 5. SINAD vs. Input Frequency and Configuration

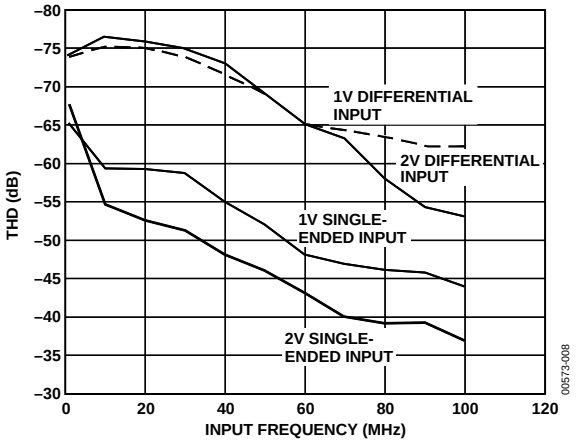

Figure 8. THD vs. Input Frequency and Configuration

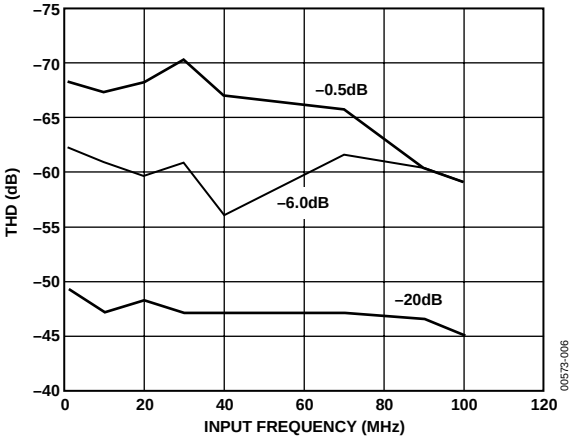

Figure 6. THD vs. Input Frequency and Amplitude (Differential Input VREF = 0.5 V)

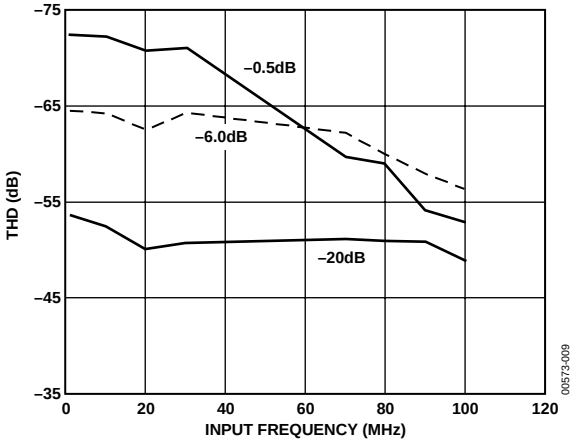

Figure 9. THD vs. Input Frequency and Amplitude (Differential Input VREF = 1 V)

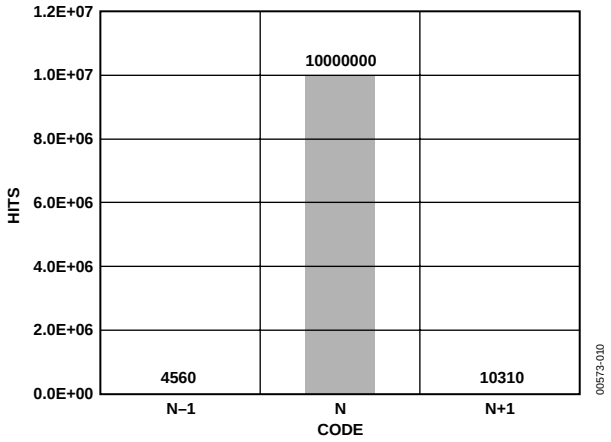

Figure 10. Grounded Input Histogram

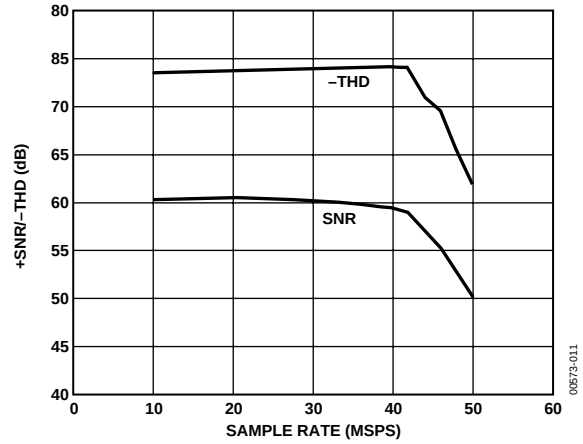

Figure 11. SNR and THD vs. Sample Rate (f_{IN} = 20 MHz)

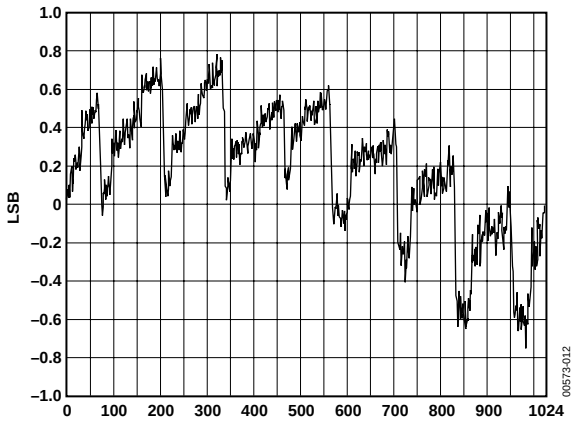

Figure 12. Typical INL Performance

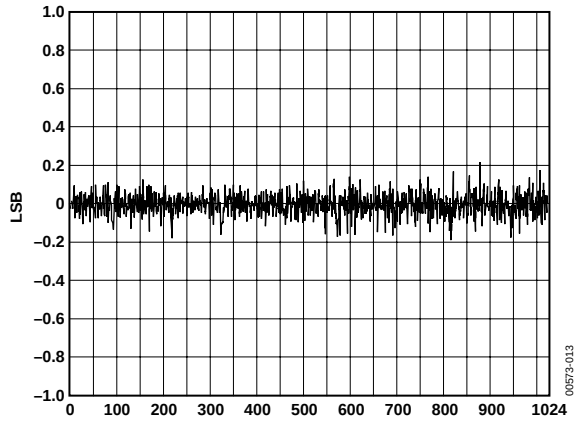

Figure 13. Typical DNL Performance

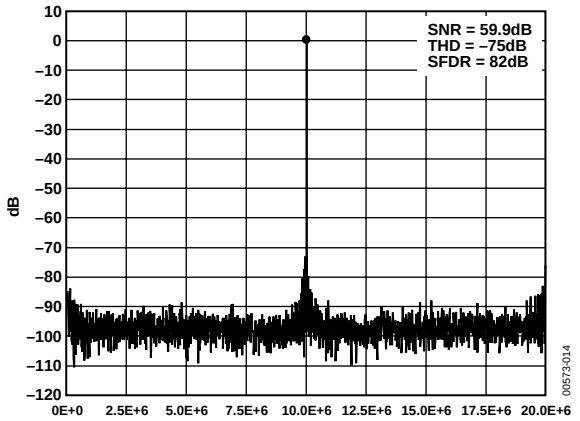

Figure 14. Single Tone Frequency Domain Performance (Input Frequency = 10 MHz, Sample Rate = 40 MSPS 2 V Differential Input, 8192 Point FFT)

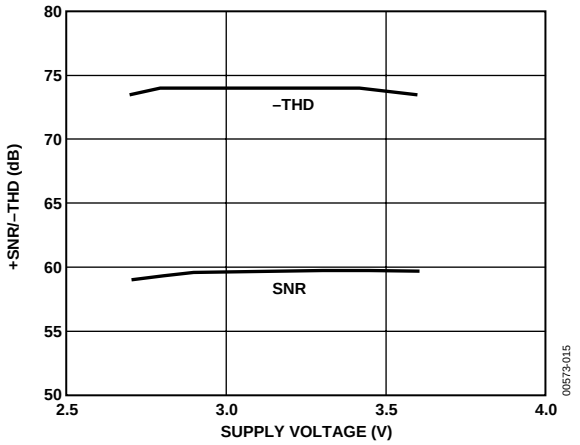

Figure 15. SNR and THD vs. Power Supply (f_{IN} = 20 MHz, Sample Rate = 40 MSPS)

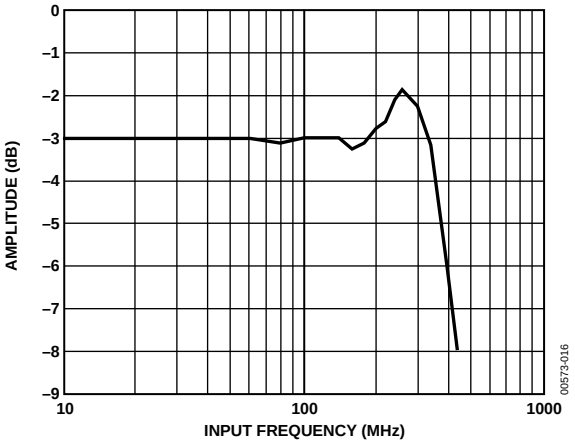

Figure 16. Full Power Bandwidth

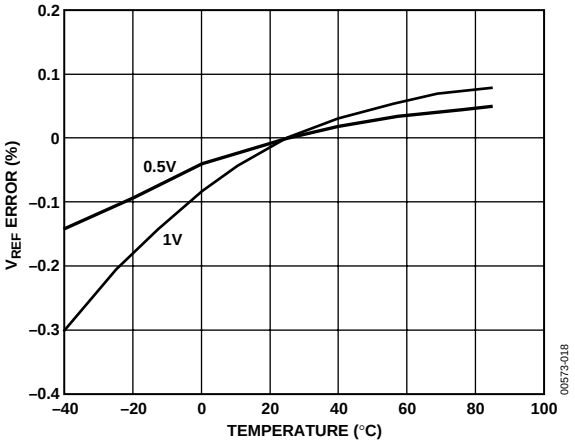

Figure 18. Reference Voltage vs. Temperature

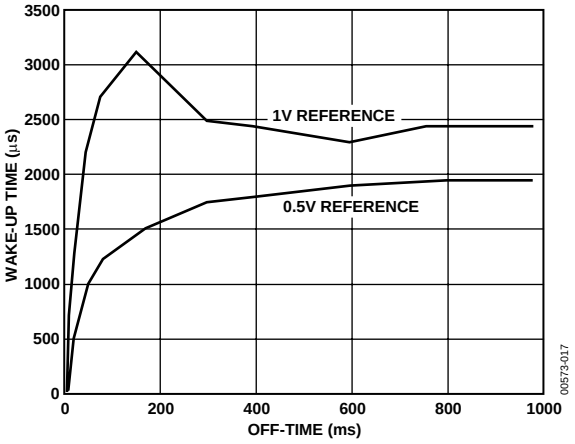

Figure 17. Wake-Up Time vs. Off Time (VREF Decoupling = 10 µF)

OPERATIONS

THEORY OF OPERATION

The AD9203 implements a pipelined multistage architecture to achieve high sample rates while consuming low power. It distributes the conversion over several smaller A/D subblocks, refining the conversion with progressively higher accuracy as it passes the results from stage to stage. As a consequence of the distributed conversion, the AD9203 requires a small fraction of the 1023 comparators used in a traditional 10-bit flash-type A/D. A sample-and-hold function within each of the stages permits the first stage to operate on a new input sample while the remaining stages operate on preceding samples.

Each stage of the pipeline, excluding the last, consists of a low resolution flash A/D connected to a switched capacitor DAC and interstage residue amplifier (MDAC). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each one of the stages to facilitate digital correction of flash errors. The last stage simply consists of a flash A/D.

The input of the AD9203 incorporates a novel structure that merges the input sample-and-hold amplifier (SHA) and the first pipeline residue amplifier into a single, compact switched capacitor circuit. This structure achieves considerable noise and power savings over a conventional implementation that uses separate amplifiers by eliminating one amplifier in the pipeline. By matching the sampling network of the input SHA with the first stage flash A/D, the AD9203 can sample inputs well beyond the Nyquist frequency with no degradation in performance. Sampling occurs on the falling edge of the clock.

OPERATIONAL MODES

The AD9203 may be connected in several input configurations, as shown in Table 4.

The AD9203 may be driven differentially from a source that keeps the signal peaks within the power supply rails.

Alternatively, the input may be driven into AINP or AINN from a single-ended source. The input span will be 2 the programmed reference voltage. One input will accept the signal, while the opposite input will be set to midscale by connecting it to the internal or an external reference. For example, a 2 V p-p signal may be applied to AINP while a 1 V reference is applied to AINN. The AD9203 will then accept a signal varying between 2 V and 0 V. See Figure 19, Figure 20, and Figure 21 for more details.

The single-ended (ac-coupled) input of the AD9203 may also be clamped to ground by the internal clamp switch. This is accomplished by connecting the CLAMP pin to AINN or AINP. Digital output formats may be configured in binary and twos complement. This is determined by the potential on the DFS pin. If the pin is set to Logic 0, the data will be in straight binary format. If the pin is asserted to Logic 1, the data will be in twos complement format.

Power consumption may be reduced by placing a resistor between PWRCON and AVSS. This may be done to conserve power when not encoding high-speed analog input frequencies or sampling at the maximum conversion rate. See the

Power Control section for more information.

Table 4. Modes

Name	Figure Number	Advantages
1 V Differential	Figure 28 with VREF Connected to REFSENSE	Differential Modes Yield the Best Dynamic Performance
2 V Differential	Figure 28 with REFSENSE Connected to AGND	Differential Modes Yield the Best Dynamic Performance
1 V Single-Ended	Figure 20	Video and Applications Requiring Clamping Require Single-Ended Inputs
2 V Single-Ended	Figure 19	Video and Applications Requiring Clamping Require Single-Ended Inputs

INPUT AND REFERENCE OVERVIEW

Like the voltage applied to the top of the resistor ladder in a flash A/D converter, the value VREF defines the maximum input voltage to the *A/D core*. The minimum input voltage to the A/D core is automatically defined to be −VREF.

The addition of a differential input structure gives the user an additional level of flexibility that is not possible with traditional flash converters. The input stage allows the user to easily configure the inputs for either single-ended operation or differential operation. The A/D's input structure allows the dc offset of the input signal to be varied independently of the input span of the converter. Specifically, the input to the A/D core is the difference of the voltages applied at the AINP and AINN input pins. Therefore, the equation,

$$V_{CORE} = AINP - AINN \quad (1)$$

defines the output of the differential input stage and provides the input to the A/D core.

The voltage, V_{CORE}, must satisfy the condition,

$$-VREF \leq V_{CORE} \leq VREF \quad (2)$$

where *VREF* is the voltage at the *VREF* pin.

The actual span (AINP − AINN) of the ADC is ±VREF.

While an infinite combination of AINP and AINN inputs exist that satisfy Equation 2, an additional limitation is placed on the inputs by the power supply voltages of the AD9203. The power supplies bound the valid operating range for AINP and AINN. The condition,

$$AVSS - 0.3\ V < AINP < AVDD + 0.3\ V$$
$$AVSS - 0.3\ V < AINN < AVDD + 0.3\ V \quad (3)$$

where AVSS is nominally 0 V and AVDD is nominally 3 V, defines this requirement. The range of valid inputs for AINP and AINN is any combination that satisfies both Equations 2 and 3.

INTERNAL REFERENCE CONNECTION

A comparator within the AD9203 will detect the potential of the VREF pin. If REFSENSE is grounded, the reference amplifier switch will connect to the resistor divider (see Figure 19). That will make VREF equal to 1 V. If resistors are placed between VREF, REFSENSE and ground, the switch will be connected to the REFSENSE position and the reference amplitude will depend on the external programming resistors (Figure 21). If REFSENSE is tied to VREF, the switch will also connect to REFSENSE and the reference voltage will be 0.5 V (Figure 20). REFTF and REFBF will drive the ADC conversion core and establish its maximum and minimum span. The range of the ADC will equal twice the voltage at the reference pin for either an internal or external reference.

Figure 19 illustrates the input configured with a 1 V reference. This will set the single-ended input of the AD9203 in the 2 V span (2 × VREF). This example shows the AINN input is tied to the 1 V VREF. This will configure the AD9203 to accept a 2 V input centered around 1 V.

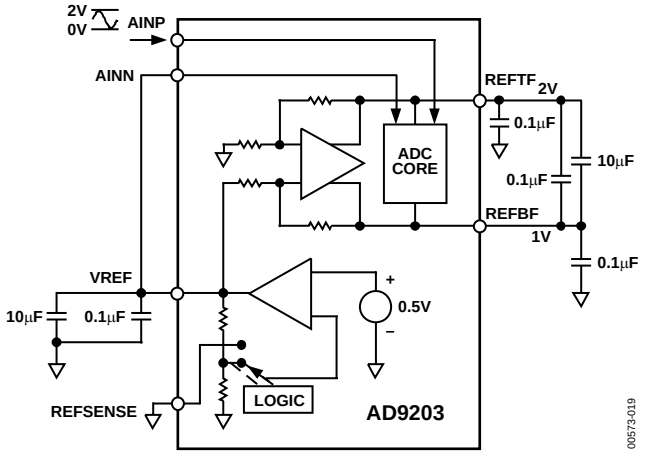

Figure 19. Internal Reference Set for a 2 V Span

Figure 20 illustrates the input configured with a 0.5 V reference. This will set the single-ended input of the ADC in a 1 V span (2 × VREF). The AINN input is tied to the 0.5 VREF. This will configure the AD9203 to accept a 1 V input centered around 0.5 V.

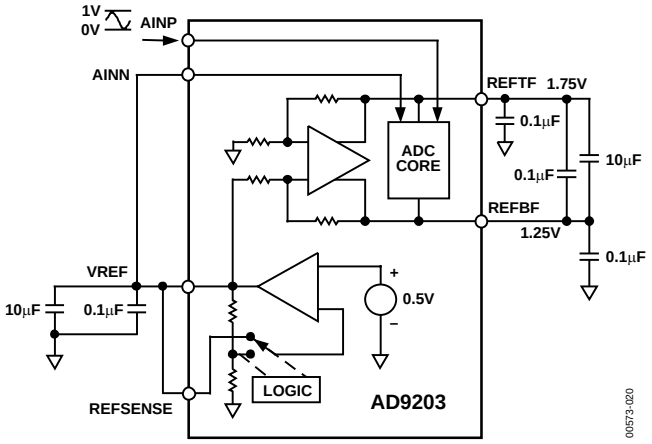

Figure 20. Internal Reference Set for a 1 V Span

Figure 21 shows the reference programmed by external resistors for 0.75 V. This will set the ADC to receive a 1.5 V span centered about 0.75 V. The reference is programmed according to the algorithm:

$$VREF = 0.5\ V \times [1 + (RA/RB)]$$

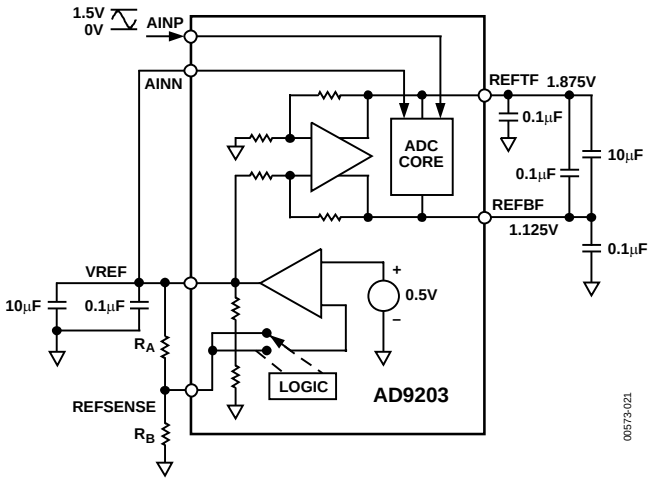

Figure 21. Programmable Reference Configuration

EXTERNAL REFERENCE OPERATION

Figure 22 illustrates the use of an external reference. An external reference may be necessary for several reasons. Tighter reference tolerance will enhance the accuracy of the ADC and will allow lower temperature drift performance. When several ADCs track one another, a single reference (internal or external) will be necessary. The AD9203 will draw less power when an external reference is used.

When the REFSENSE pin is tied to AVDD, the internal reference will be disabled, allowing the use of an external reference.

The AD9203 contains an internal reference buffer. It will load the external reference with an equivalent 10 kΩ load. The internal buffer will generate positive and negative full-scale references for the ADC core.

In Figure 22, an external reference is used to set the midscale set point for single-ended use. At the same time, it sets the input voltage span through a resistor divider. If the ADC is being driven differentially through a transformer, the external reference can set the center tap (common-mode voltage).

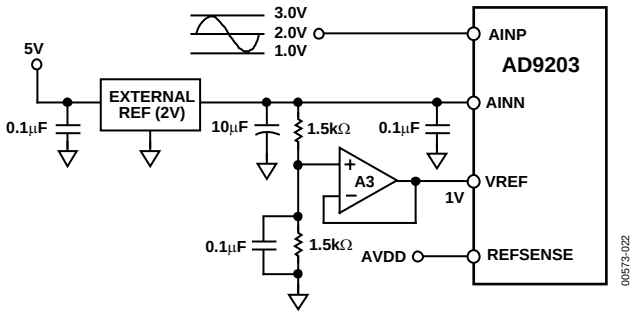

Figure 22. External Reference Configuration

CLAMP OPERATION

The AD9203 contains an internal clamp. It may be used when operating the input in a single-ended mode. This clamp is very useful for clamping NTSC and PAL video signals to ground. The clamp cannot be used in the differential input mode.

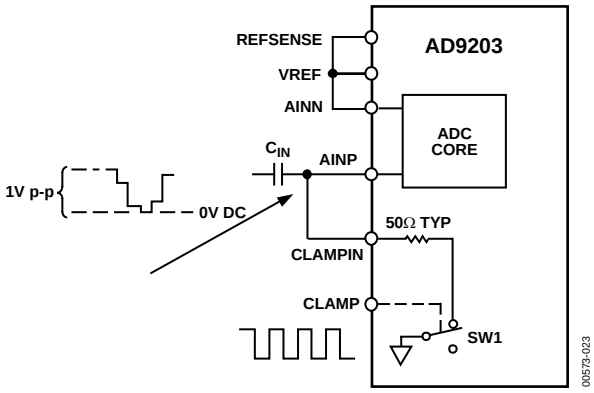

Figure 23. Clamp Configuration (VREF = 0.5 V)

Figure 23 shows the internal clamp circuitry and the external control signals needed for clamp operation. To enable the clamp, apply a logic high 1 to the CLAMP pin. This will close SW1, the internal switch. SW1 is opened by asserting the CLAMP pin low 0. The capacitor holds the voltage across C_{IN} constant until the next interval. The charge on the capacitor will leak off as a function of input bias current (see Figure 24).

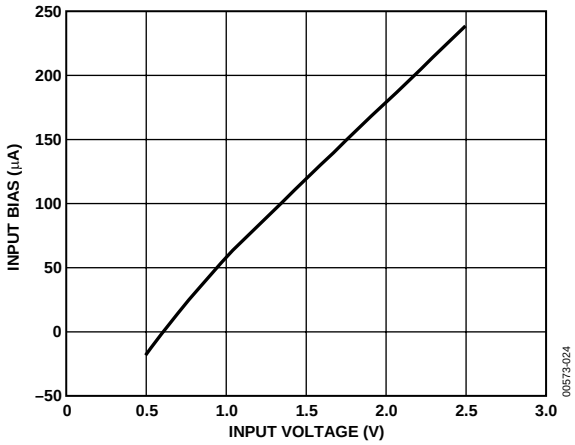

Figure 24. Input Bias Current vs. Input Voltage (F_S = 40 MSPS)

DRIVING THE ANALOG INPUT

Figure 25 illustrates the equivalent analog input of the AD9203, (a switched capacitor input). Bringing CLK to a logic high, opens S3 and closes S1 and S2. The input source connected to AIN and must charge Capacitor C_H during this time. Bringing CLK to a logic low opens S2, and then S1 opens followed by closing S3. This puts the input in the hold mode.

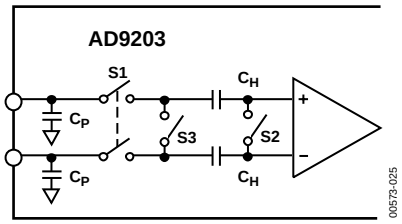

Figure 25. Input Architecture

The structure of the input SHA places certain requirements on the input drive source. The combination of the pin capacitance, C_P, and the hold capacitance, C_H, is typically less than 5 pF. The input source must be able to charge or discharge this capacitance to 10-bit accuracy in one half of a clock cycle. When the SHA goes into track mode, the input source must charge or discharge capacitor C_H from the voltage already stored on C_H to the new voltage. In the worst case, a full-scale voltage step on the input source must provide the charging current through the R_{ON} (100 Ω) of Switch 1 and quickly (within 1/2 CLK period) settle. This situation corresponds to driving a low input impedance. Adding series resistance between the output of the signal source and the AIN pin reduces the drive requirements placed on the signal source. Figure 26 shows this configuration. The bandwidth of the particular application limits the size of this resistor. To maintain the performance outlined in the data sheet specifications, the resistor should be limited to 50 Ω or less. The series input resistor can be used to isolate the driver from the AD9203's switched capacitor input. The external capacitor may be selected to limit the bandwidth into the AD9203. Two input RC networks should be used to balance differential input drive schemes (Figure 26).

The input span of the AD9203 is a function of the reference voltage. For more information regarding the input range, see the Internal Reference Connection and External Reference Operation sections of the data sheet.

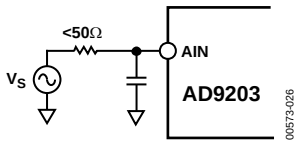

Figure 26. Simple AD9203 Drive Configuration

In many cases, particularly in single-supply operation, ac coupling offers a convenient way of biasing the analog input signal to the proper signal range. Figure 27 shows a typical configuration for ac-coupling the analog input signal to the AD9203. Maintaining the specifications outlined in the data sheet requires careful selection of the component values. The most important is the $f_{-3\,dB}$ high-pass corner frequency. It is a function of R2 and the parallel combination of C1 and C2.

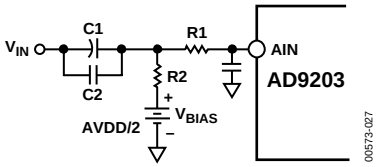

Figure 27. AC-Coupled Input

The $f_{-3\,dB}$ point can be approximated by the equation:

$$f_{-3dB} = 1/(2\pi \times [R2]\ C_{EQ})$$

where C_{EQ} is the parallel combination of C1 and C2. Note that C1 is typically a large electrolytic or tantalum capacitor that becomes inductive at high frequencies. Add a small ceramic or polystyrene capacitor (on the order of 0.01 µF) that is negligibly inductive at higher frequencies while maintaining a low impedance over a wide frequency range.

There are additional considerations when choosing the resistor values for an ac-coupled input. The ac-coupling capacitors integrate the switching transients present at the input of the AD9203 and cause a net dc bias current, IB, to flow into the input. The magnitude of the bias current increases as the signal changes and as the clock frequency increases. This bias current will result in an offset error of (R1 + R2) IB. If it is necessary to compensate for this error, consider modifying VBIAS to account for the resultant offset. In systems that must use dc coupling, use an op amp to level shift ground-referenced signals to comply with the input requirements of the AD9203.

OP AMP SELECTION GUIDE

Op amp selection for the AD9203 is highly application dependent. In general, the performance requirements of any given application can be characterized by either time domain or frequency domain constraints. In either case, one should carefully select an op amp that preserves the performance of the A/D. This task becomes challenging when one considers the AD9203's high performance capabilities coupled with other system level requirements such as power consumption and cost.

The ability to select the optimal op amp may be further complicated by either limited power supply availability and/or limited acceptable supplies for a desired op amp. Newer, high performance op amps typically have input and output range limitations in accordance with their lower supply voltages. As a result, some op amps will be more appropriate in systems where ac coupling is allowed. When dc coupling is required, the headroom constraints of op amps (such as rail-to-rail op amps) or ones where larger supplies can be used, should be considered.

The following section describes some op amps currently available from Analog Devices. Please contact the factory or local sales office for updates on Analog Devices latest amplifier product offerings.

AD8051: $f_{-3\ dB}$ = 110 MHz. Low cost. Best used for driving single-ended ac-coupled configuration. Operates on a 3 V power rail.

AD8052: Dual Version of above amp.

AD8138 is a higher performance version of AD8131. Its gain is programmable and provides 14-bit performance.

DIFFERENTIAL MODE OF OPERATION

Since not all applications have a signal preconditioned for differential operation, there is often a need to perform a single-ended-to-differential conversion. In systems that do not need a dc input, an RF transformer with a center tap is one method to generate differential inputs beyond 20 MHz for the AD9203. This provides all the benefits of operating the A/D in the differential mode without contributing additional noise or distortion. An RF transformer also has the benefit of providing electrical isolation between the signal source and the A/D.

An improvement in THD and SFDR performance can be realized by operating the AD9203 in differential mode. The performance enhancement between the differential and single-ended mode is greatest as the input frequency approaches and goes beyond the Nyquist frequency (i.e., $f_{IN} > F_S/2$).

The AD8138 provides a convenient method of converting a single-ended signal to a differential signal. This is an ideal method for generating a direct coupled signal to the AD9203. The AD8138 will accept a signal and shift it to an externally provided common-mode level. The AD8138 configuration is shown in Figure 28.

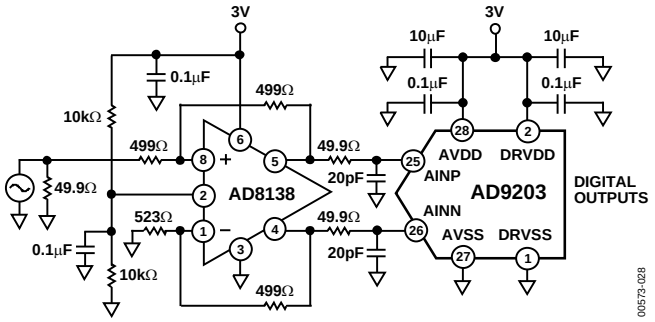

Figure 28. AD8138 Driving an AD9203, a 10-Bit, 40 MSPS A/D Converter

Figure 29 shows the schematic of a suggested transformer circuit. The circuit uses a Minicircuits RF transformer, model number T4–1T, which has an impedance ratio of four (turns ratio of 2).

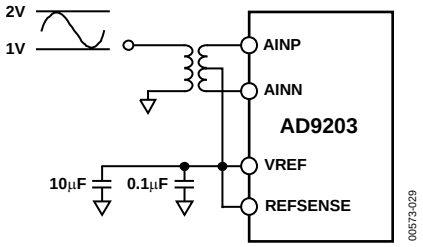

Figure 29. Transformer Coupled Input

The center tap of the transformer provides a convenient means of level-shifting the input signal to a desired common-mode voltage. Figure 30 illustrates the performance of the AD9203 over a wide range of common-mode levels.

Transformers with other turns ratios may also be selected to optimize the performance of a given application. For example, selecting a transformer with a higher impedance ratio, such as minicircuits T16–6T with an impedance ratio of 16, effectively steps up the signal amplitude, thus further reducing the driving requirements of the signal source.

The AD9203 can be easily configured for either a 1 V p-p or 2 V p-p input span by setting the internal reference. Other input spans can be realized with two external gain setting resistors as shown in Figure 21 of this data sheet. Figure 34 and Figure 35 demonstrate the SNR and SFDR performance over a wide range of amplitudes required by most communication applications.

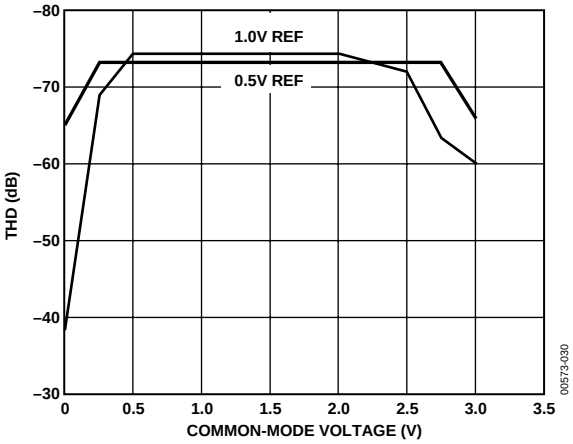

Figure 30. THD vs. Common-Mode Voltage vs. THD (AIN = 2 V Differential) (f_{IN} = 5 MHz, f_S = 40 MSPS)

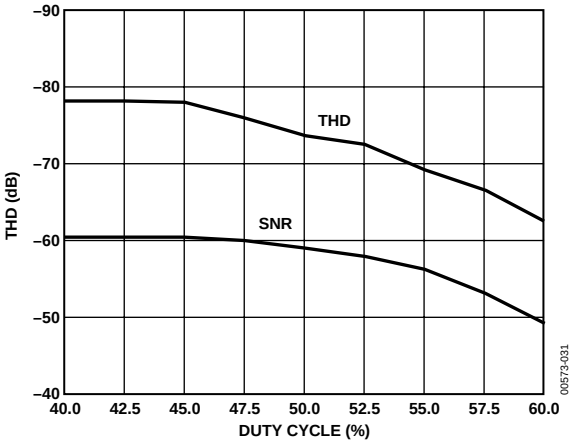

Figure 31. THD and SNR vs. Clock Duty Cycle (f_{IN} = 5 MHz Differential, Clock = 40 MSPS)

Table 5. Power Programming Resistance

Clock MSPS	Resistor Value (k)
1	50
5 to 10	100
15 to 20	200
>20	500

POWER CONTROL

Power consumed by the AD9203 may be reduced by placing a resistor between the PWRCON pin and ground. This function will be valuable to users who do not need the AD9203's high conversion rate, but do need even lower power consumption. The external resistor sets the programming of the analog current mirrors. Table 5 illustrates the relationship between programmed power and performance.

At lower clock rates, less power is required within the analog sections of the AD9203. Placing an external resistor on the PWRCON pin will shunt control current away from some of the current mirrors. This enables the ADC to convert low data rates with extremely low power consumption.

INTERFACING TO 5 V SYSTEMS

The AD9203 can be integrated into 5 V systems. This is accomplished by deriving a 3 V power supply from the existing 5 V analog power line through an AD3307-3 linear regulator.

Care must be maintained so that logic inputs do not exceed the maximum rated values listed on the Specifications page.

CLOCK INPUT AND CONSIDERATIONS

The AD9203 internal timing uses the two edges of the clock input to generate a variety of internal timing signals. Sampling occurs on the falling edge. The clock input to the AD9203 operating at 40 MSPS may have a duty cycle between 45% to 55% to meet this timing requirement since the minimum specified t_{CH} and t_{CL} is 11.25 ns. For clock rates below 40 MSPS, the duty cycle may deviate from this range to the extent that both t_{CH} and t_{CL} are satisfied. See Figure 31 for dynamics vs. duty cycle.

High-speed, high-resolution A/Ds are sensitive to the quality of the clock input. The degradation in SNR at a given full-scale input frequency (f_{IN}) due only to aperture jitter (t_A) can be calculated with the following equation:

$$SNR\ degradation = 20 \log_{10} [1/2\pi f_{IN} t_A]$$

In the equation, the rms aperture jitter, t_A, represents the rootsum square of all the jitter sources, which include the clock input, analog input signal, and A/D aperture jitter specification. Undersampling applications are particularly sensitive to jitter.

Clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9203. Power supplies for clock drivers should be separated from the A/D output driver supplies to avoid modulating the clock signal with digital noise. Low jitter crystal controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing or another method), it should be retimed by the original clock at the last step.

The clock input is referred to the analog supply. Its logic threshold is AVDD/2.

DIGITAL INPUTS AND OUTPUTS

Each of the AD9203 digital control inputs, 3-STATE, DFS, and STBY are referenced to analog ground. CLK is also referenced to analog ground. A low power mode feature is provided such that for STBY = HIGH and the static power of the AD9203 drops to 0.65 mW.

Asserting the DFS pin high will invert the MSB pin, changing the data to a twos complement format.

The AD9203 has an OTR (out of range) function. If the input voltage is above or below full scale by 1 LSB, the OTR flag will go high. See Figure 32.

OTR	DATA OUTPUTS	
1	11111	11111
0	11111	11111
0	11111	11110
0	00000	00001
0	00000	00000
1	00000	00000

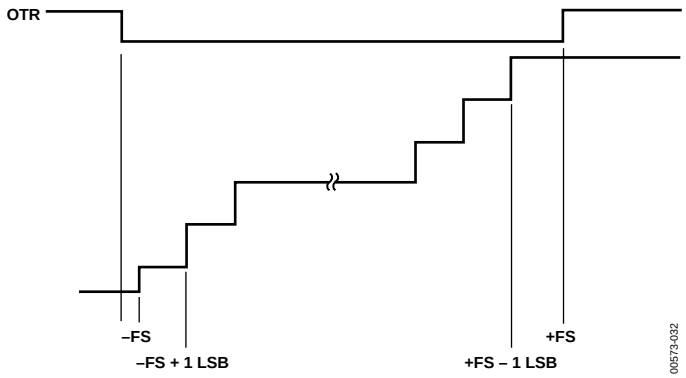

Figure 32. Output Data Format

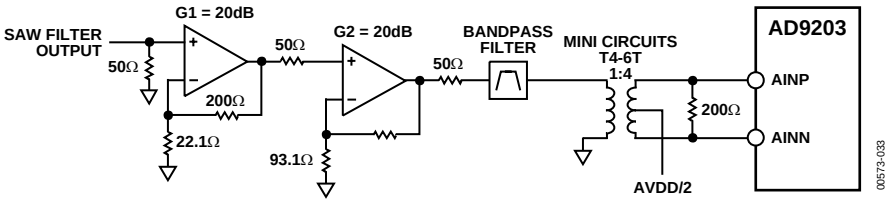

Figure 33. Simplified IF Sampling Circuit

APPLICATIONS

DIRECT IF DOWN CONVERSION

Sampling IF signals above an ADC's baseband region (i.e., dc to FS/2) is becoming increasingly popular in communication applications. This process is often referred to as direct IF down conversion or undersampling. There are several potential benefits in using the ADC to alias (or mix) down a narrow band or wide band IF signal. First and foremost is the elimination of a complete mixer stage with its associated amplifiers and filters, reducing cost and power dissipation. Second is the ability to apply various DSP techniques to perform such functions as filtering, channel selection, quadrature demodulation, data reduction, detection, etc. A detailed discussion on using this technique in digital receivers can be found in Analog Devices Application Notes AN-301 and AN-302.

In direct IF down conversion applications, one exploits the inherent sampling process of an ADC in which an IF signal lying outside the baseband region can be aliased back into the baseband region in a manner similar to a mixer downconverting an IF signal. Similar to the mixer topology, an image rejection filter is required to limit other potential interfering signals from also aliasing back into the ADC's baseband region.

A trade-off exists between the complexity of this image rejection filter and the ADC's sample rate and dynamic range.

The AD9203 is well suited for various IF sampling applications. Its low distortion input SHA has a full-power bandwidth extending to 130 MHz, thus encompassing many popular IF frequencies. Only the 2 V span should be used for undersampling beyond 20 MHz. A DNL of ±0.25 LSB combined with low thermal input referred noise allows the AD9203 in the 2 V span to provide >59 dB of SNR for a baseband input sine wave. Also, its low aperture jitter of 1.2 ps rms ensures minimum SNR degradation at higher IF frequencies. In fact, the AD9203 is capable of still maintaining 58 dB of SNR at an IF of 70 MHz with a 2 V input span.

To maximize its distortion performance, the AD9203 should be configured in the differential mode with a 2 V span using a transformer. The center-tap of the transformer is biased to the reference output of the AD9203. Preceding the AD9203 and transformer is an optional bandpass filter as well as a gain stage. A low Q passive bandpass filter can be inserted to reduce out of band distortion and noise that lies within the AD9203's 390 MHz bandwidth. A large gain stage(s) is often required to compensate for the high insertion losses of a SAW filter used for channel selection and image rejection. The gain stage will also provide adequate isolation for the SAW filter from the charge kick back currents associated with the AD9203's switched capacitor input stage.

The distortion and noise performance of an ADC at the given IF frequency is of particular concern when evaluating an ADC for a narrowband IF sampling application. Both single tone and dual tone SFDR vs. amplitude are very useful in assessing an ADC's dynamic and static nonlinearities. SNR vs. amplitude performance at the given IF is useful in assessing the ADC's noise performance and noise contribution due to aperture jitter. In any application, one is advised to test several units of the same device under the same conditions to evaluate the given applications sensitivity to that particular device. Figure 34 and Figure 35 combine the dual tone SFDR as well as single tone SFDR and SNR performances at IF frequencies of 70 MHz, and 130 MHz. Note, the SFDR vs. amplitude data is referenced to dBFS while the single tone SNR data is referenced to dBc. The performance characteristics in these figures are representative of the AD9203 without any preceding gain stage. The AD9203 was operated in the differential mode (via transformer) with a 2 V span and a sample rate of 40 MSPS. The analog supply (AVDD) and the digital supply (DRVDD) were set to 3.0 V.

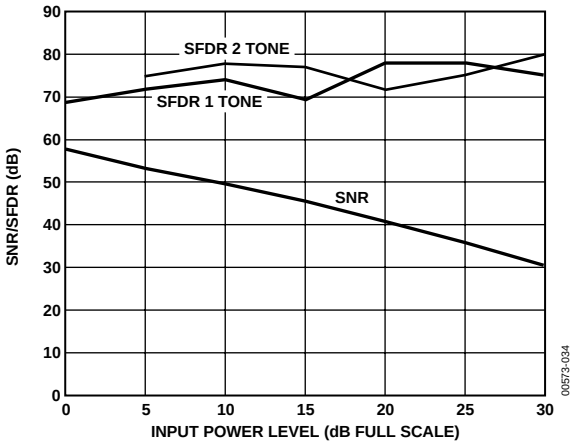

Figure 34. SNR/SFDR for IF @ 70 MHz (Clock = 40 MSPS)

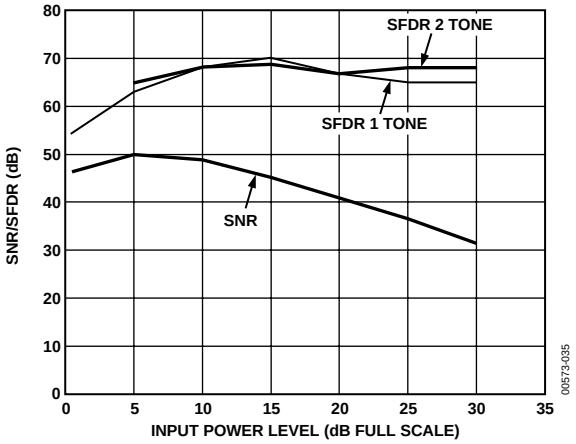

Figure 35. SNR/SFDR for IF @ 130 MHz (Clock = 40 MSPS)

ULTRASOUND APPLICATIONS

The AD9203 provides excellent performance in 10-bit ultrasound applications. This is demonstrated by its high SNR with analog input frequencies up to and including Nyquist. The presence of spurs near the base of a fundamental frequency bin is demonstrated by Figure 37. Note that the spurs near the noise floor are more than 80 dB below f_{IN}. This is especially valuable in Doppler ultrasound applications where low frequency shifts from the fundamental are important.

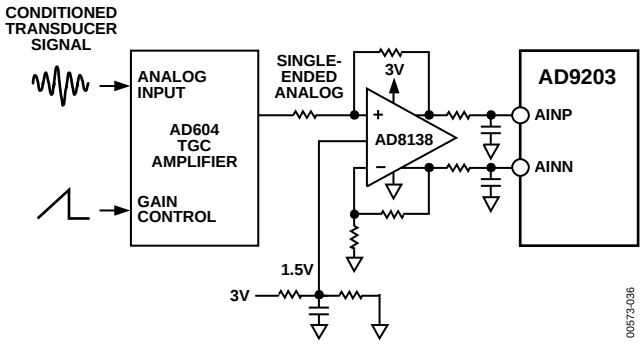

Figure 36. Ultrasound Connection for the AD9203

Figure 36 illustrates the AD604 variable gain amplifier configured for time gain compensation (TGC). The low power AD9203 is powered from a 3 V supply rail while the high performance AD604 is powered from 5 V supply rails. An AD8138 is used to drive the AD9203. This is implemented due to the ability of differential drive techniques to cancel common-mode noise and input anomalies.

The 74 mW power consumption gives the 40 MSPS AD9203 an order of magnitude improvement over older generation components.

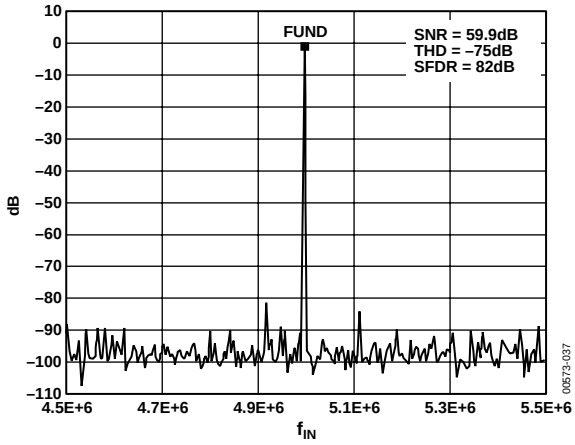

Figure 37. SFDR Performance Near the Fundamental Signal (8192 Point FFT, f_{IN} = 5 MHz, F_S = 40 MSPS)

EVALUATION BOARD

The AD9203 evaluation board is shipped wired for 2 V differential operation. The board should be connected to power and test equipment as shown in Figure 38. It is easily configured for single-ended and differential operation as well as 1 V and 2 V spans. Refer to Figure 39.

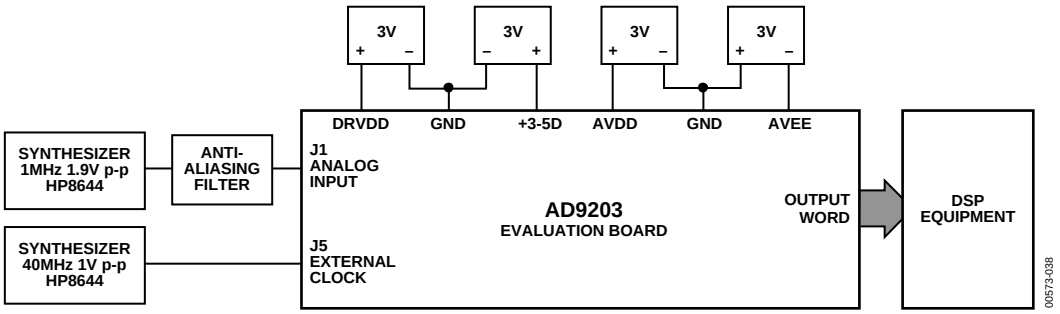

Figure 38. Evaluation Board Connection

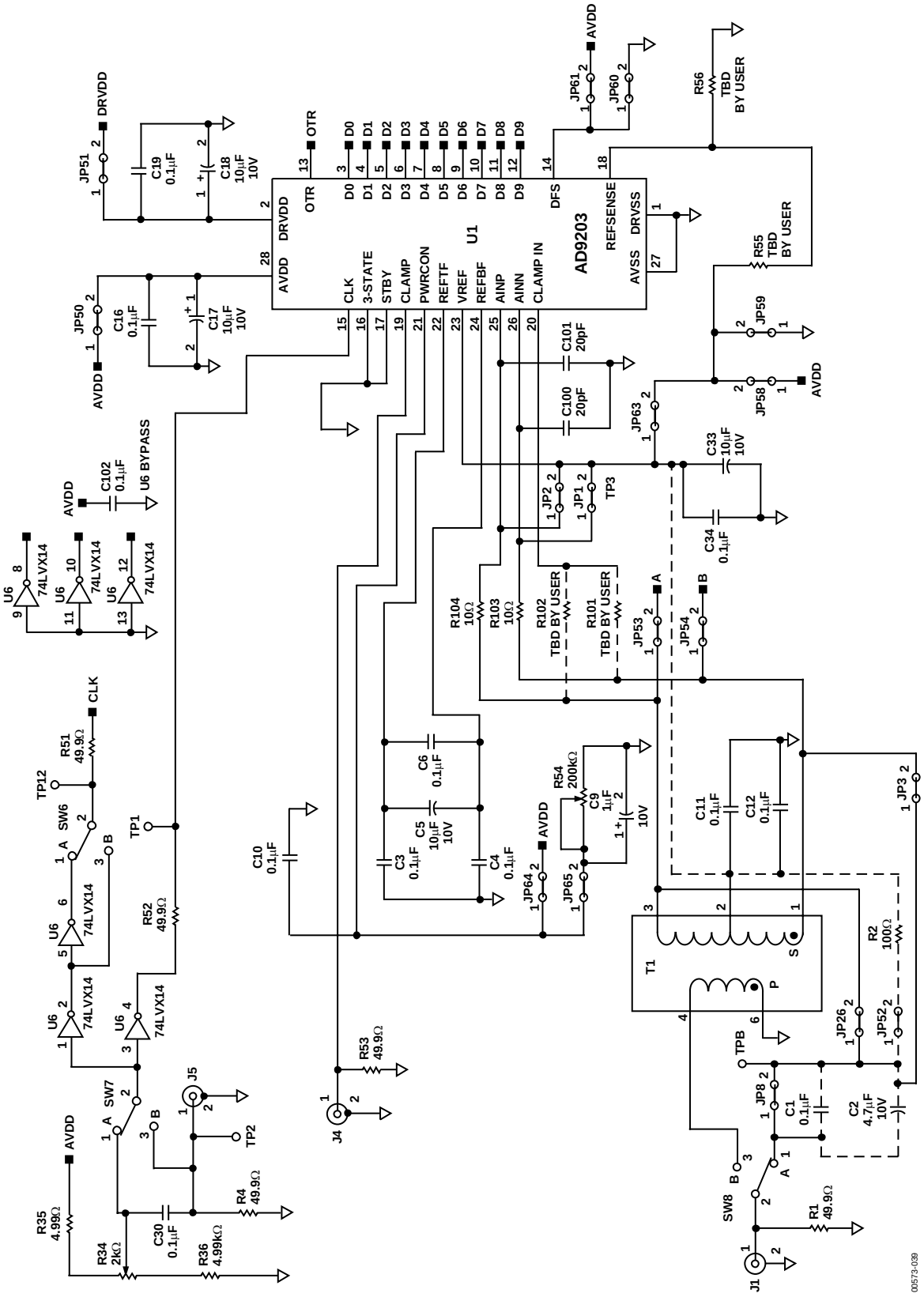

Figure 39. Evaluation Board (Rev. C)

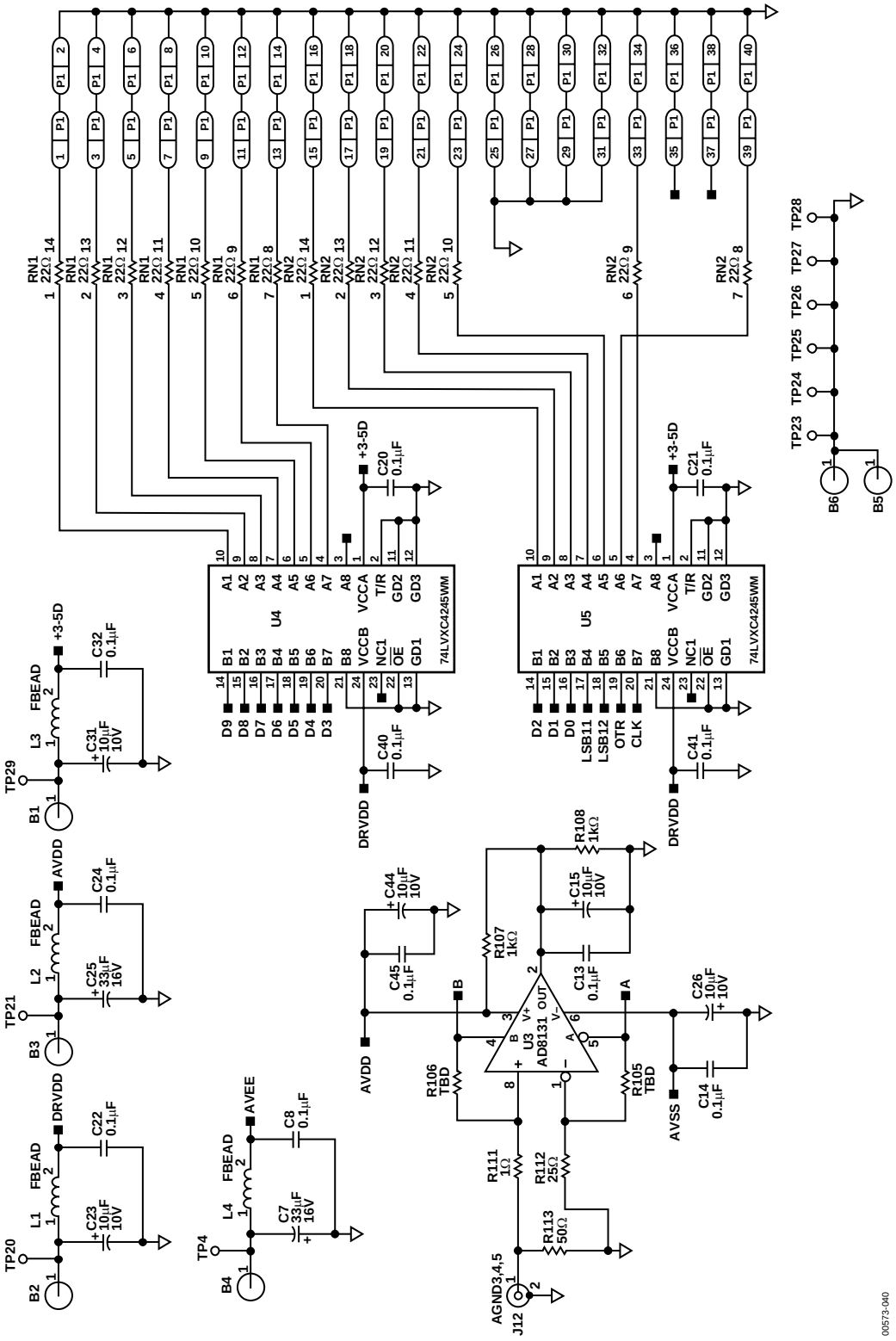

Figure 40. Evaluation Board (Rev. C)

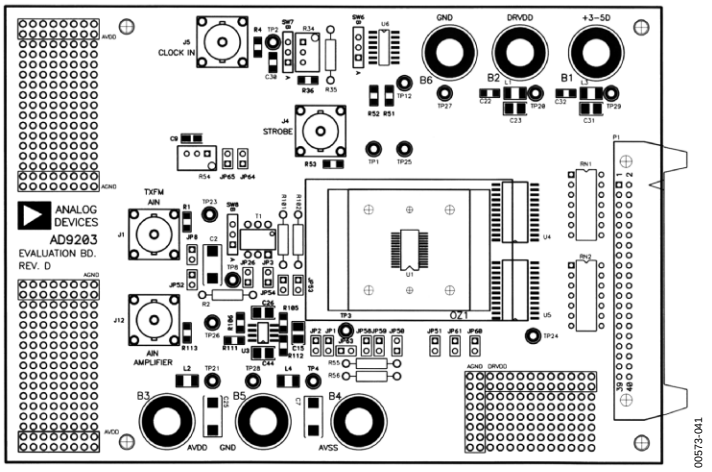

Figure 41. Evaluation Board Component Side Assembly (Not to Scale)

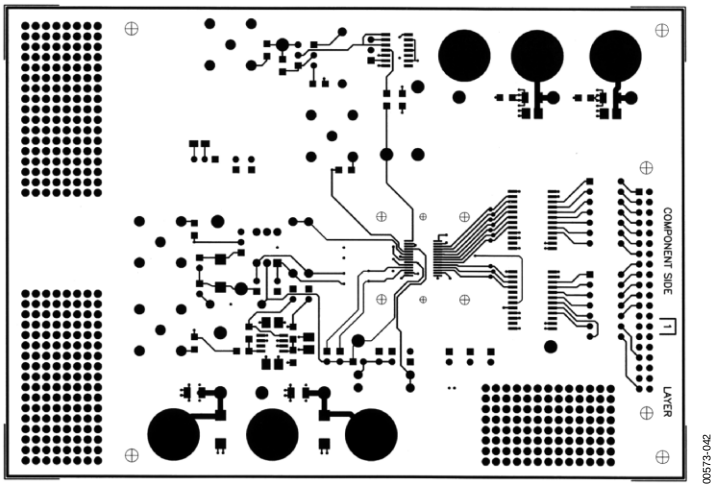

Figure 42. Evaluation Board Component Side (Not to Scale)

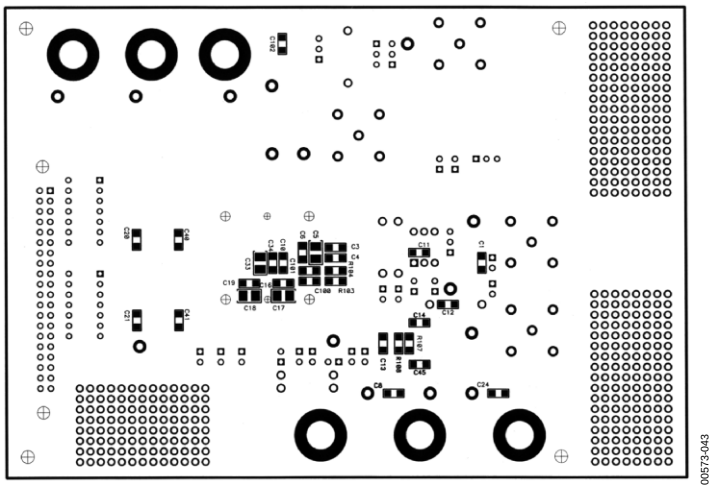

Figure 43. Evaluation Board Solder Side Assembly (Not to Scale)

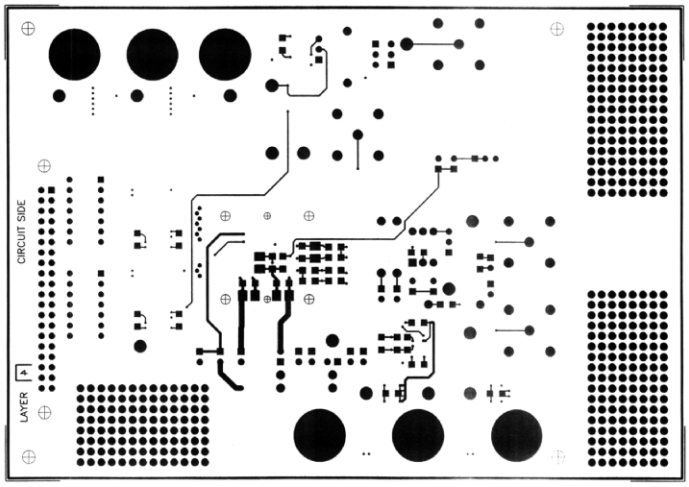

Figure 44. Evaluation Board Solder Side (Not to Scale)

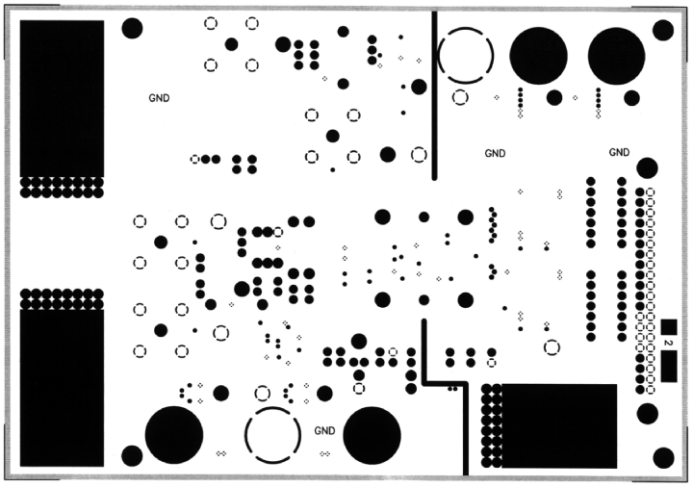

Figure 45. Evaluation Board Ground Plane (Not to Scale)

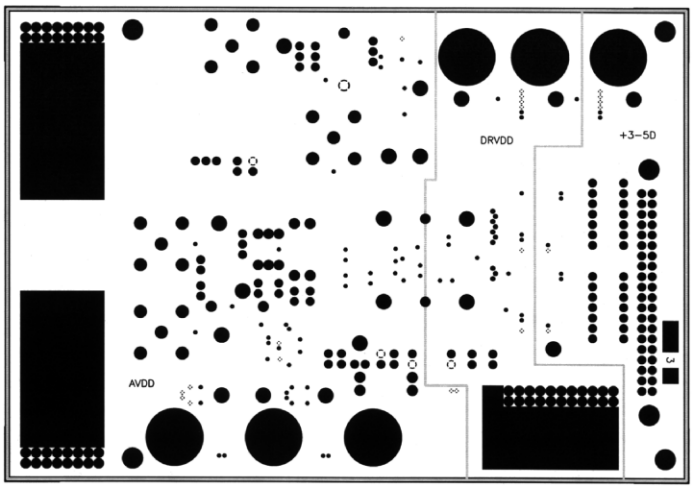

Figure 46. Evaluation Board Power Plane (Not to Scale)

OUTLINE DIMENSIONS

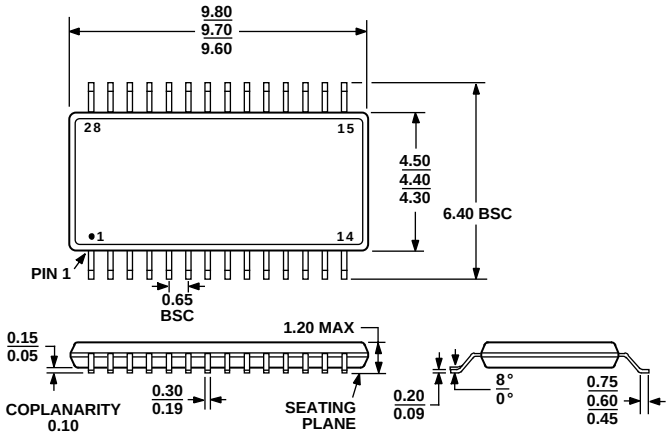

Figure 47. 28-Lead Thin Shrink Small Outline Package (RU-28)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9203ARU	−40°C to +85°C	28-Lead Thin Shrink Small Outline	RU-28
AD9203ARURL7	−40°C to +85°C	28-Lead Thin Shrink Small Outline	RU-28
AD9203ARUZ[1]	−40°C to +85°C	28-Lead Thin Shrink Small Outline	RU-28
AD9203ARUZRL7[1]	−40°C to +85°C	28-Lead Thin Shrink Small Outline	RU-28
AD9203-EB		Evaluation Board	

[1] Z = Pb-free part.

NOTES

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C00573–0–8/04(B)