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REVISION HISTORY

7/08—Rev. A to Rev. B	
Changes to Phase Inversion Section	10
Deleted Figure 33.....	10
Added Figure 33 and Figure 34.....	10
Updated Outline Dimensions	12
7/07—Rev. 0 to Rev. A	
Change to Figure 21	8
Change to Figure 31	9

10/06—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15.0\text{ V}$, $T_A = 25^\circ\text{C}$, $V_{CM} = 0\text{ V}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$+25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		0.35	1	mV
AD8682		$-40^\circ\text{C} \leq T_A \leq +25^\circ\text{C}$			2.5	mV
AD8684		$+25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			3	mV
		$-40^\circ\text{C} \leq T_A \leq +25^\circ\text{C}$			3.5	mV
Input Bias Current	I_B	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		6	20	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			125	pA
		$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			20	pA
		$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			100	pA
Input Voltage Range			-11		+15	V
Common-Mode Rejection Ratio	CMRR	$-11\text{ V} \leq V_{CM} \leq +15\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	70	90		dB
Large Signal Voltage Gain	A_{VO}	$R_L = 10\text{ k}\Omega$	20			V/mV
		$R_L = 10\text{ k}\Omega$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	15			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			10		$\mu\text{V}/^\circ\text{C}$
Bias Current Drift	$\Delta I_B/\Delta T$			8		$\text{pA}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 10\text{ k}\Omega$	13.5	13.9		V
Output Voltage Low	V_{OL}	$R_L = 10\text{ k}\Omega$		-13.9	-13.5	V
Short-Circuit Limit	I_{SC}	Source	3	10		mA
		Sink		-12	-8	mA
Open-Loop Output Impedance	Z_{OUT}	$f = 1\text{ MHz}$		200		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5\text{ V}$ to $\pm 18\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	92	114		dB
Supply Current/Amplifier	I_{SY}	$V_O = 0\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		210	250	μA
Supply Voltage Range	V_S		± 4.5		± 18	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 10\text{ k}\Omega$	7	9		$\text{V}/\mu\text{s}$
Full-Power Bandwidth	BW_P	1% distortion		125		kHz
Settling Time	t_S	To 0.01%		1.6		μs
Gain Bandwidth Product	GBP			3.5		MHz
Phase Margin	ϕ_M			55		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		1.3		μV p-p
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		36		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	i_n			0.01		$\text{pA}/\sqrt{\text{Hz}}$

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	± 18 V
Input Voltage	± 18 V
Differential Input Voltage ¹	36 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	-65°C to $+150^{\circ}\text{C}$
Operating Temperature Range	-40°C to $+85^{\circ}\text{C}$
Junction Temperature Range	-65°C to $+150^{\circ}\text{C}$
Lead Temperature (Soldering, 60 sec)	300°C

¹ For supply voltages less than ± 18 V, the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 3.

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP [RM-8]	210	45	$^{\circ}\text{C}/\text{W}$
8-Lead SOIC_N [R-8]	158	43	$^{\circ}\text{C}/\text{W}$
14-Lead TSSOP [RU-14]	180	35	$^{\circ}\text{C}/\text{W}$
14-Lead SOIC_N [R-14]	120	36	$^{\circ}\text{C}/\text{W}$

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

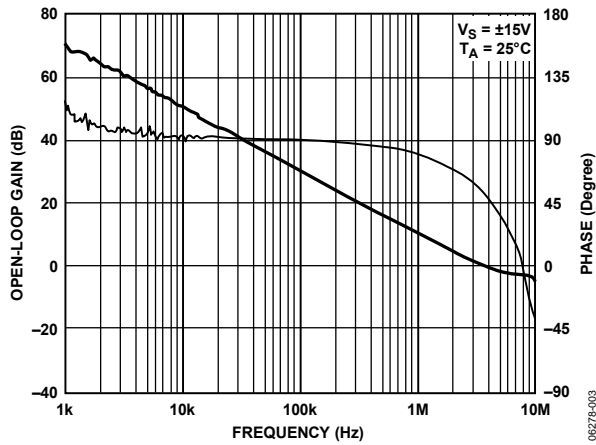


Figure 3. AD8682 Open-Loop Gain and Phase vs. Frequency

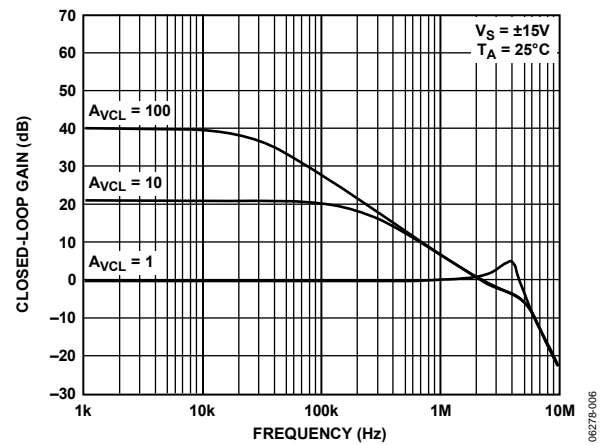


Figure 6. AD8682 Closed-Loop Gain vs. Frequency

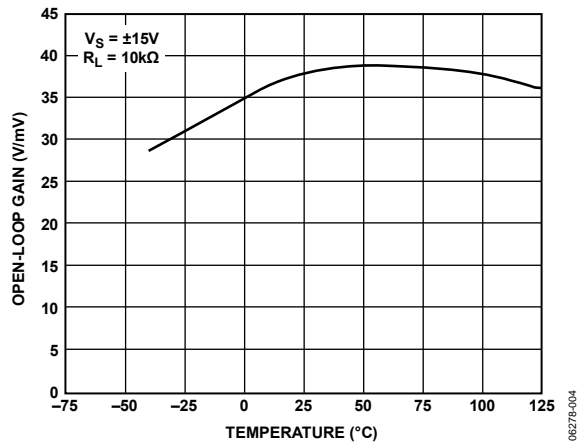


Figure 4. AD8682 Open-Loop Gain vs. Temperature

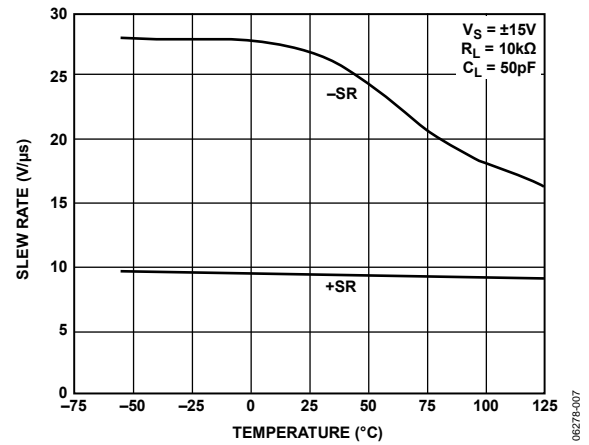


Figure 7. Slew Rate vs. Temperature

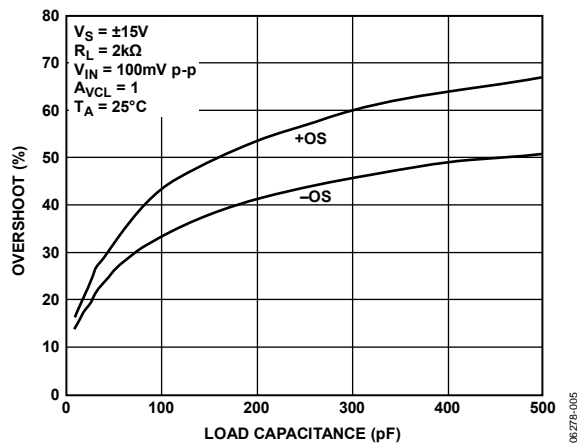


Figure 5. Small Signal Overshoot vs. Load Capacitance

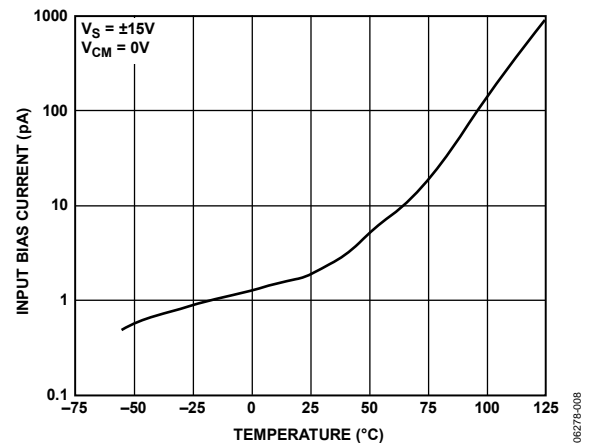


Figure 8. AD8682 Input Bias Current vs. Temperature

AD8682/AD8684

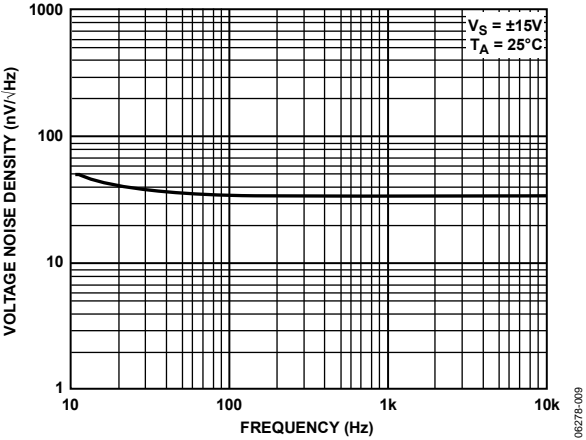


Figure 9. Voltage Noise Density vs. Frequency

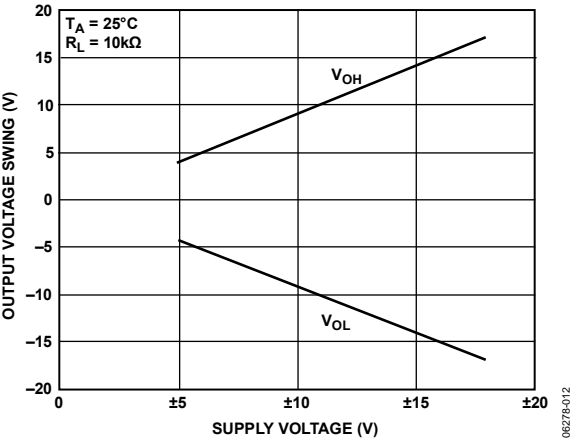


Figure 12. Output Voltage Swing vs. Supply Voltage

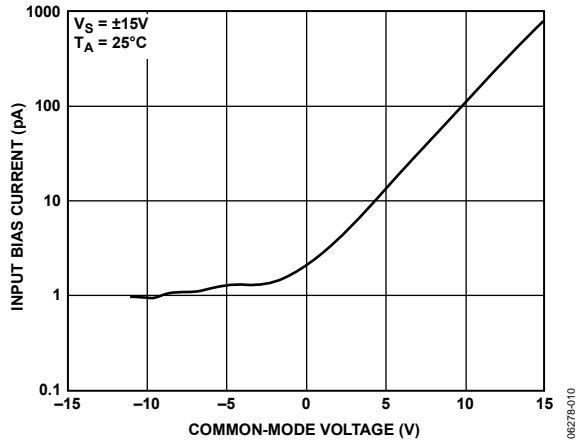


Figure 10. Input Bias Current vs. Common-Mode Voltage

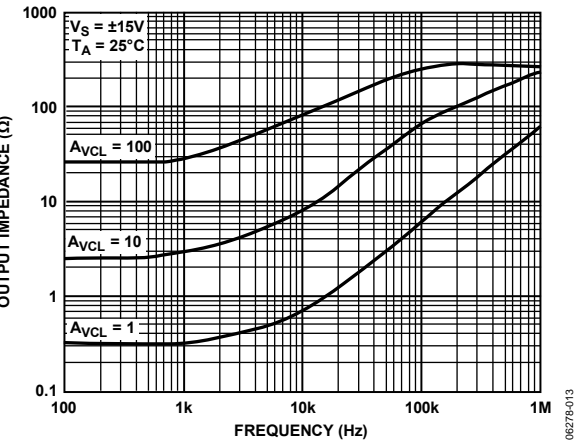


Figure 13. Closed-Loop Output Impedance vs. Frequency

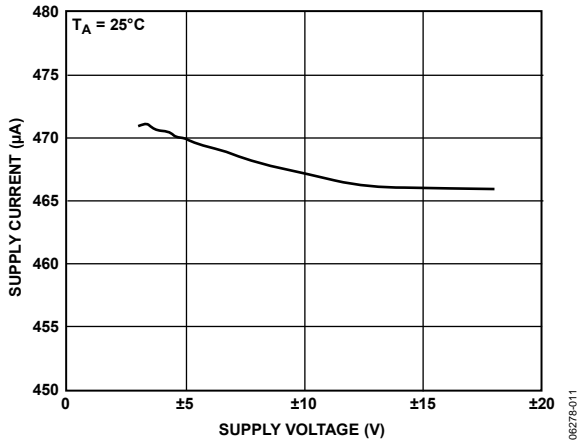


Figure 11. AD8682 Supply Current vs. Supply Voltage

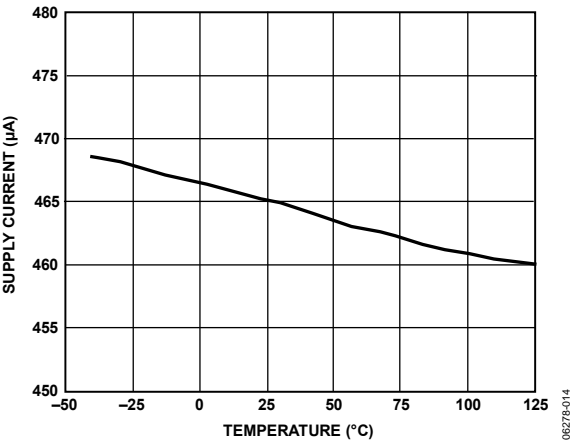


Figure 14. AD8682 Supply Current vs. Temperature

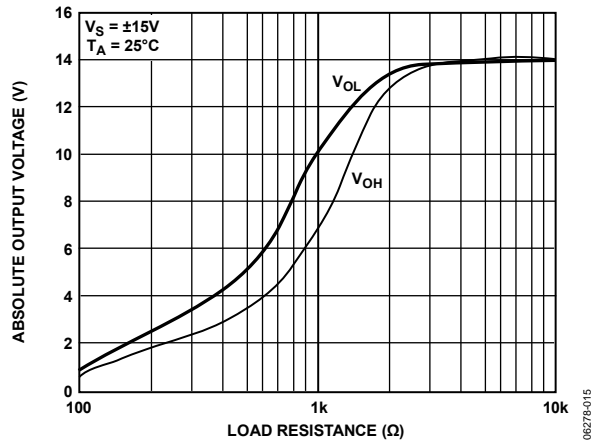


Figure 15. Absolute Output Voltage vs. Load Resistance

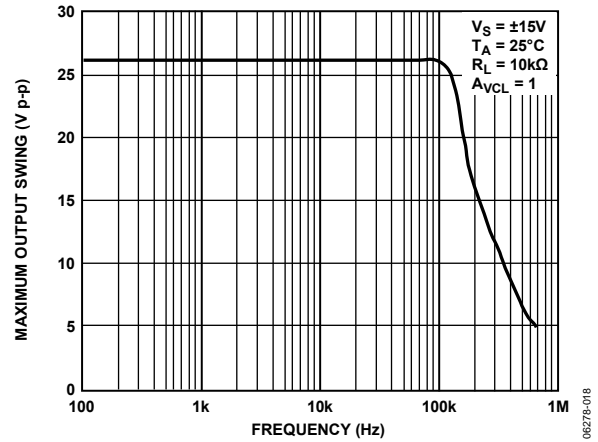


Figure 18. Maximum Output Swing vs. Frequency

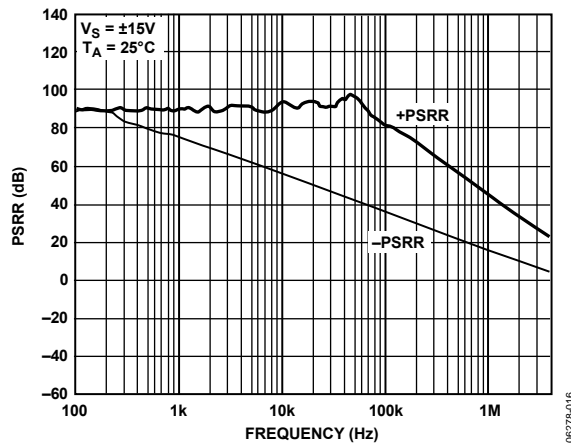


Figure 16. AD8682 PSRR vs. Frequency

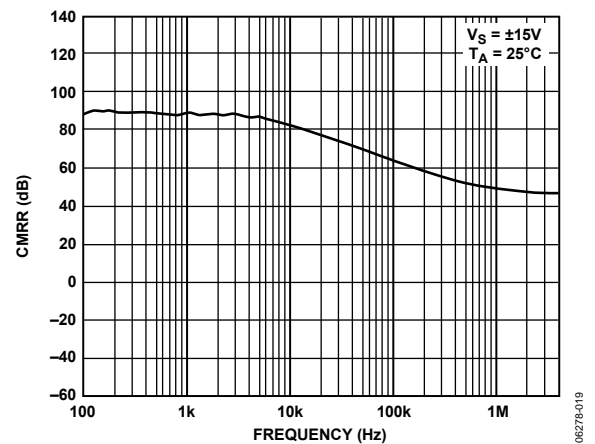


Figure 19. AD8682 CMRR vs. Frequency

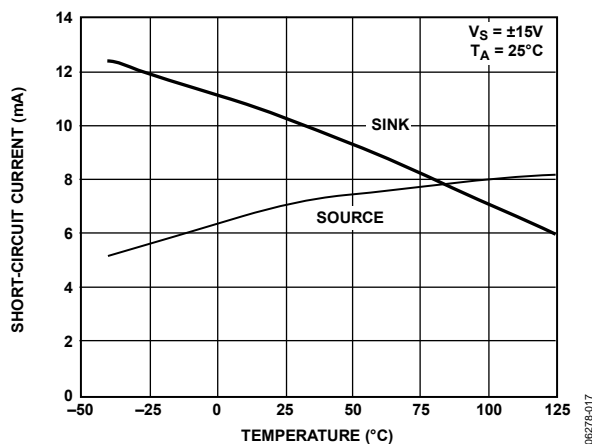


Figure 17. AD8682 Short-Circuit Current vs. Temperature

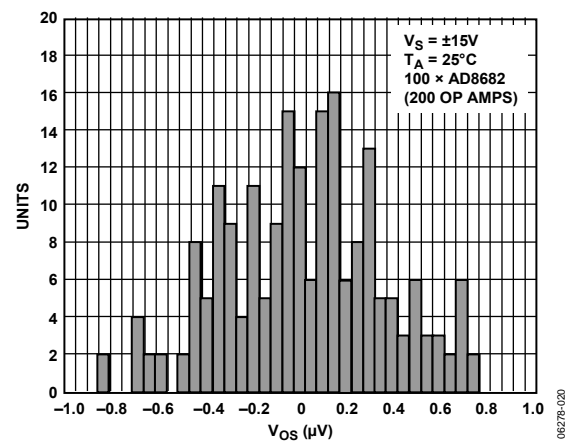


Figure 20. AD8682 VOS Distribution

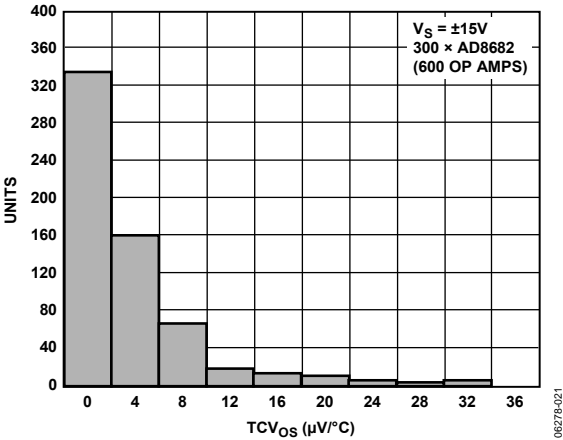


Figure 21. AD8682 TCVOS Distribution SOIC_N Package

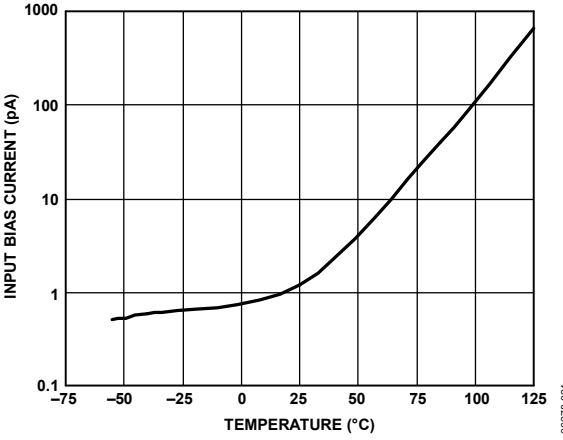


Figure 24. AD8684 Input Bias Current vs. Temperature

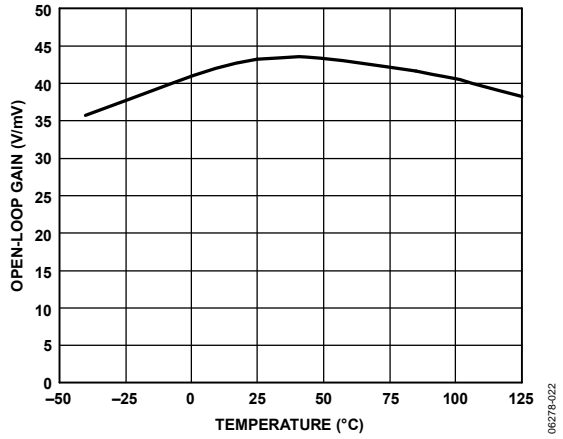


Figure 22. AD8684 Open-Loop Gain vs. Temperature

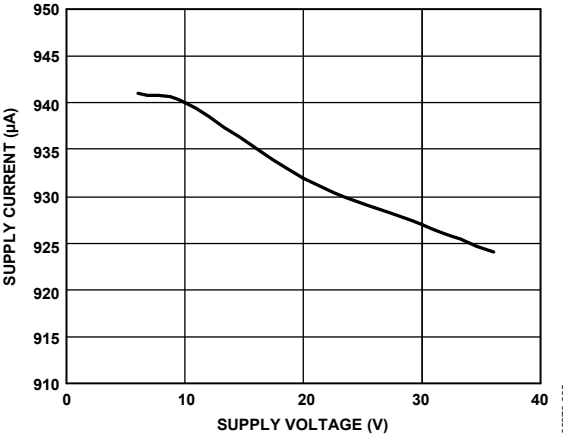


Figure 25. AD8684 Relative Supply Current vs. Supply Voltage

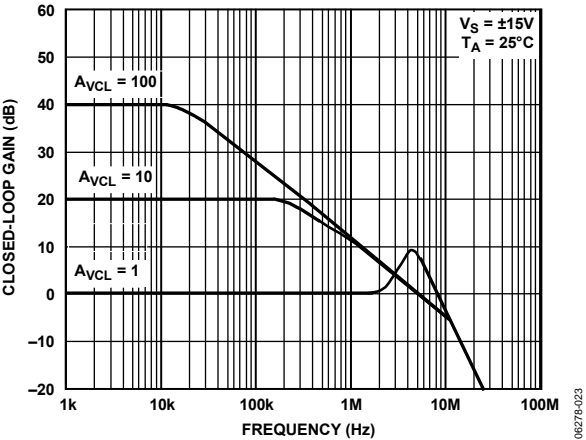


Figure 23. AD8684 Closed-Loop Gain vs. Frequency

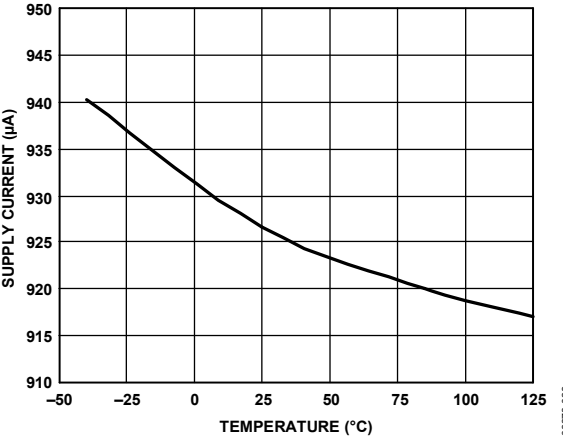


Figure 26. AD8684 Supply Current vs. Temperature

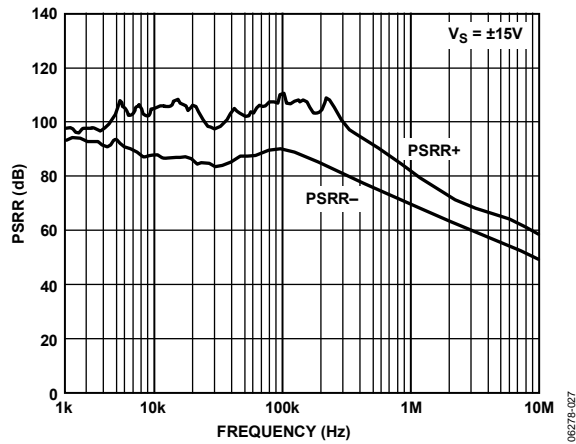


Figure 27. AD8684 PSRR vs. Frequency

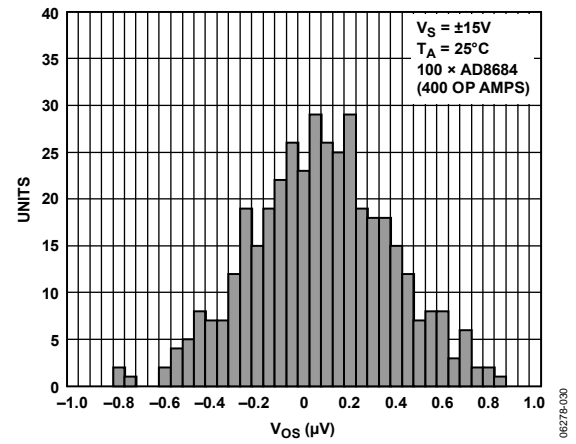


Figure 30. AD8684 VOS Distribution Package

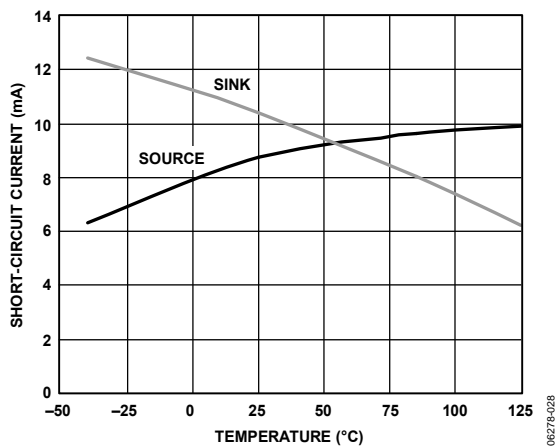


Figure 28. AD8684 Short-Circuit Current vs. Temperature

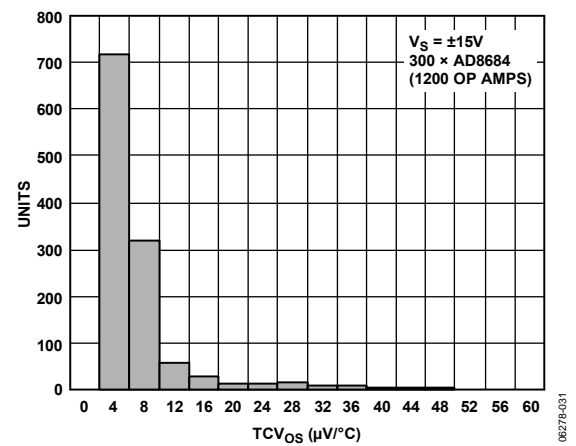


Figure 31. AD8684 TCVOS Distribution Package

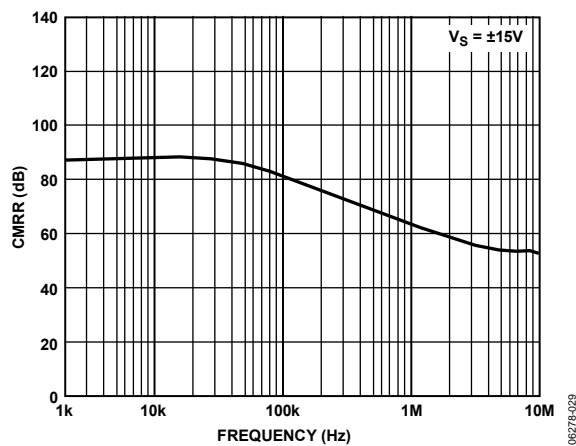


Figure 29. AD8684 CMRR vs. Frequency

APPLICATIONS INFORMATION

The AD8682 and AD8684 are dual and quad JFET op amps that are optimized for high speed at low power. This combination makes these amplifiers excellent choices for battery-powered or low power applications that require above average performance. Applications benefiting from this performance combination include telecommunications, geophysical exploration, portable medical equipment, and navigational instrumentation.

HIGH-SIDE SIGNAL CONDITIONING

There are many applications requiring the sensing of signals near the positive rail. The AD8682 and the AD8684 were tested and are guaranteed over a common-mode range ($-11\text{ V} \leq V_{CM} \leq +15\text{ V}$) that includes the positive supply.

The AD8682/AD8684 are commonly used in the sensing of power supply currents and in current sensing applications, such as the partial circuit shown in Figure 32. In this circuit, the voltage drop across a low value resistor, such as the $0.1\text{ }\Omega$ shown here, is amplified and compared to 7.5 V . The output can then be used for current limiting.

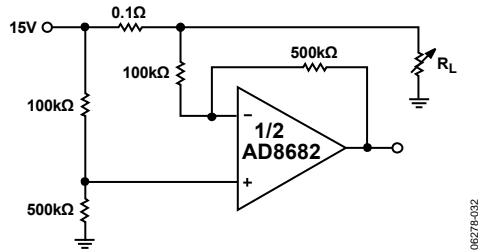


Figure 32. High-Side Signal Conditioning

PHASE INVERSION

Most JFET input amplifiers invert the phase of the input signal if either input exceeds the input common-mode range. For the AD8682/AD8684, a negative signal in excess of 11 V causes phase inversion. This is caused by saturation of the input stage leading to the forward-biasing of a gate-drain diode. Phase reversal in AD8682/AD8684 can be prevented by using Schottky diodes to clamp the input terminals to each other and to the supplies. In the simple buffer circuit below, D1 protects the op amp against phase reversal. R1, D2, and D3 limit the input

current when the input exceeds the supply rail. The resistor should be selected to limit the amount of input current below the absolute maximum rating.

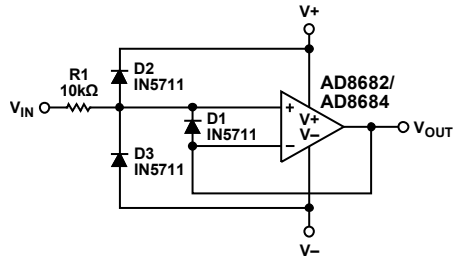


Figure 33. Phase Reversal Solution Circuit

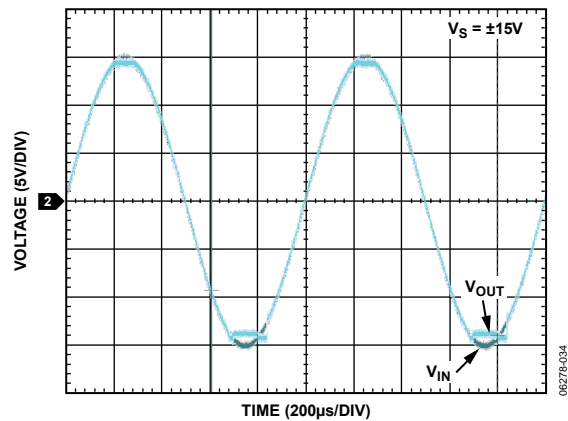


Figure 34. No Phase Reversal

ACTIVE FILTERS

The wide bandwidth and high slew rates of the AD8682/AD8684 make either one an excellent choice for many filter applications. There are many active filter configurations, but the four most popular configurations are: Butterworth, elliptic, Bessel, and Chebyshev. Each type has a response that is optimized for a given characteristic, as shown in Table 4.

Table 4.

Type	Selectivity	Overshoot	Phase	Amplitude (Pass Band)	Amplitude (Stop Band)
Butterworth	Moderate	Good	Nonlinear	Maximum flat	Equal ripple
Chebyshev	Good	Moderate		Equal ripple	
Elliptic	Best	Poor		Equal ripple	
Bessel (Thompson)	Poor	Best	Linear		

PROGRAMMABLE STATE VARIABLE FILTER

The circuit shown in Figure 35 can be used to accurately program the Q factor; the cutoff frequency (f_c); and the gain of a two-pole state variable filter. The AD8684 has been used in this design because of its high bandwidth, low power, and low noise. This circuit takes only three packages to build because of the quad configuration of the op amps and DACs.

The DACs shown are used in voltage mode; therefore, many values are dependent on the accuracy of the DAC only and not on the absolute values of the DAC resistive ladders. As a result, this makes the circuit unusually accurate for a programmable filter.

Adjusting DAC 1 changes the signal amplitude across R1; therefore, the DAC attenuation \times R1 determines the amount of signal current that charges the integrating capacitor, C1.

This cutoff frequency can be expressed as

$$f_c = \frac{1}{2\pi R1C1} \left(\frac{D1}{256} \right)$$

where $D1$ is the digital code for the DAC.

DAC 3 is used to set the gain. The gain equation is

$$Gain = \frac{R4}{R5} \left(\frac{D3}{256} \right)$$

DAC 2 is used to set the Q of the circuit. Adjusting this DAC controls the amount of feedback from the band-pass node to the input summing node. Note that the digital value of the DAC is in the numerator; therefore, zero code is not a valid operating point.

$$Q = \frac{R2}{R3} \left(\frac{256}{D2} \right)$$

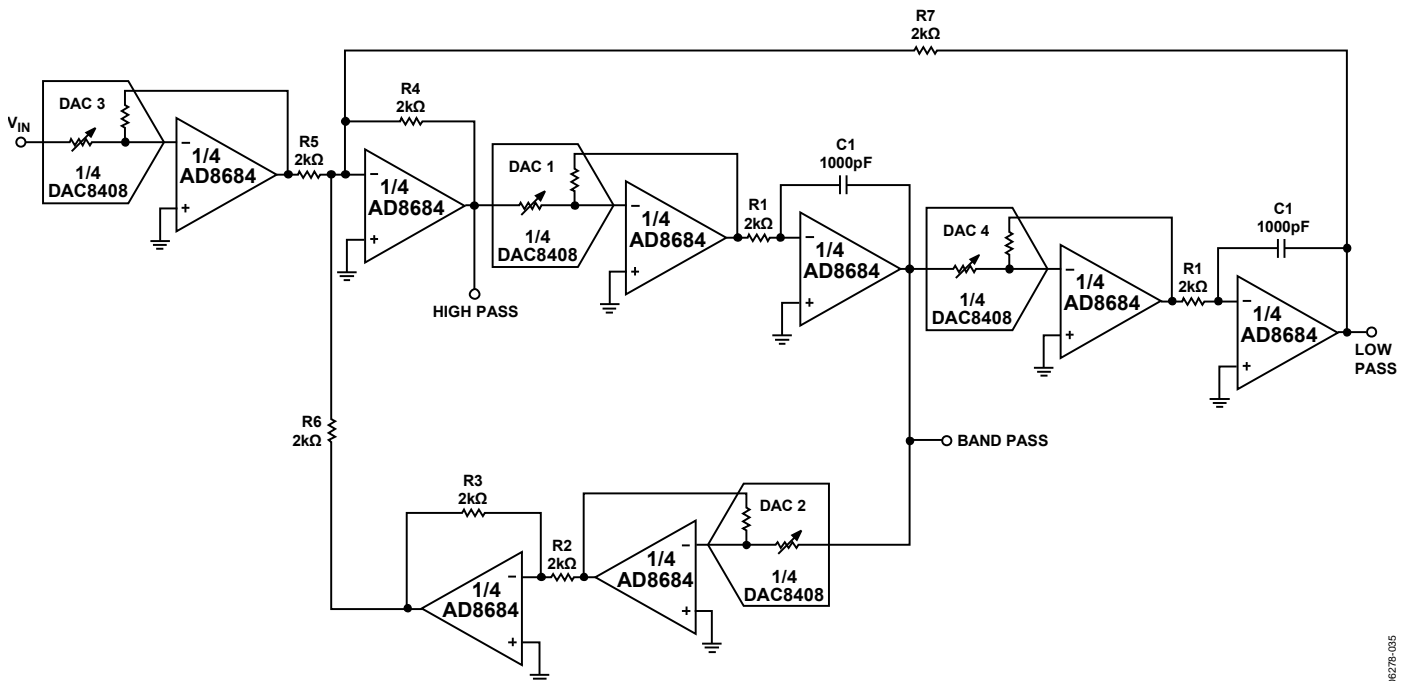
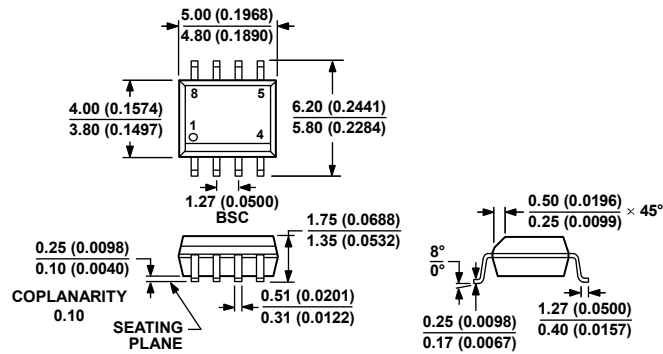


Figure 35. Programmable State Variable Filter

OUTLINE DIMENSIONS

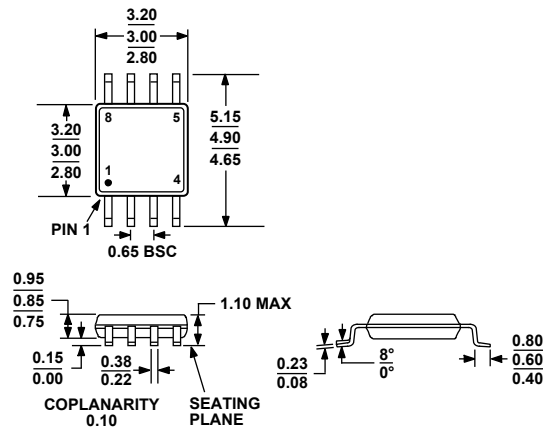


COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 36. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)

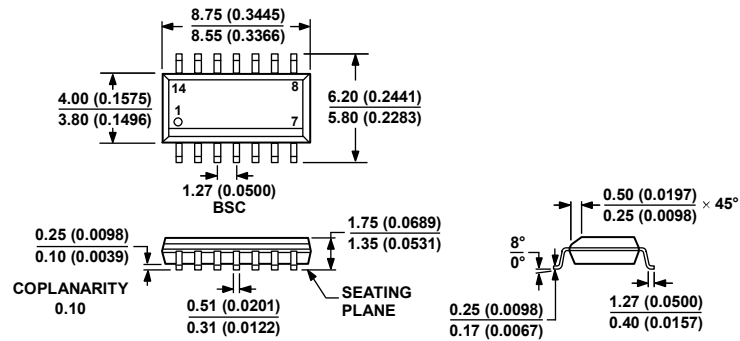
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 37. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)

Dimensions shown in millimeters

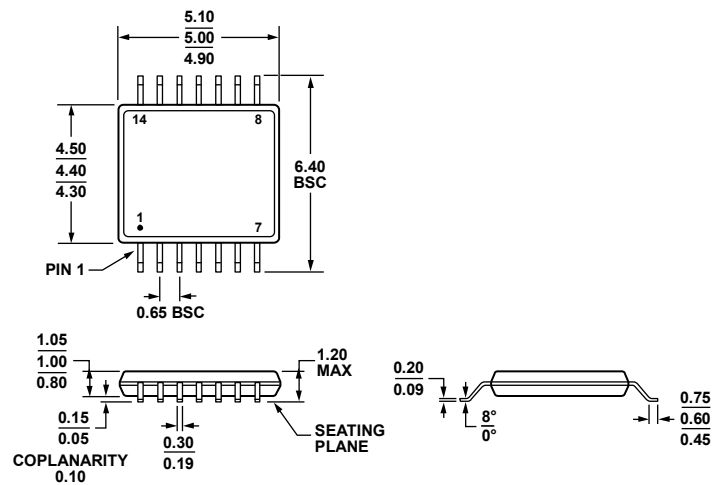


COMPLIANT TO JEDEC STANDARDS MS-012-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 38. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)

Dimensions shown in millimeters and (inches)

060606-A



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 39. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)

Dimensions shown in millimeters

061908-A

AD8682/AD8684

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8682ARZ ¹	–40°C to +85°C	8-Lead SOIC_N	R-8	A1K A1K
AD8682ARZ-REEL ¹	–40°C to +85°C	8-Lead SOIC_N	R-8	
AD8682ARZ-REEL7 ¹	–40°C to +85°C	8-Lead SOIC_N	R-8	
AD8682ARMZ-R2 ¹	–40°C to +85°C	8-Lead MSOP	RM-8	
AD8682ARMZ-REEL ¹	–40°C to +85°C	8-Lead MSOP	RM-8	
AD8684ARZ ¹	–40°C to +85°C	14-Lead SOIC_N	R-14	
AD8684ARZ-REEL ¹	–40°C to +85°C	14-Lead SOIC_N	R-14	
AD8684ARZ-REEL7 ¹	–40°C to +85°C	14-Lead SOIC_N	R-14	
AD8684ARUZ ¹	–40°C to +85°C	14-Lead TSSOP	RU-14	
AD8684ARUZ-REEL ¹	–40°C to +85°C	14-Lead TSSOP	RU-14	

¹ Z = RoHS Compliant Part.

NOTES

NOTES