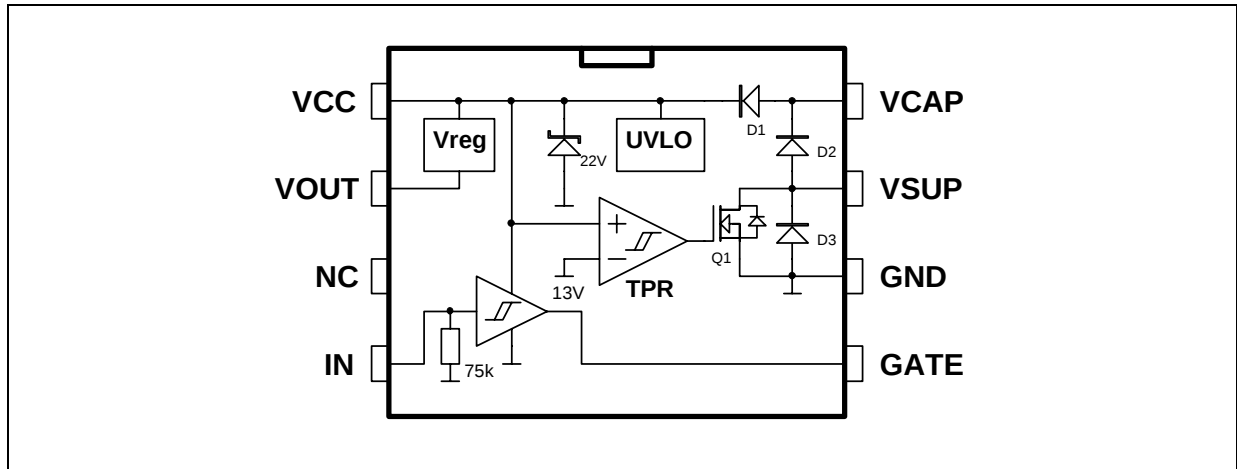


1 BLOCK DIAGRAM



Pin Description

Name	Pin Number	Type	Function
VCC	1	Power supply	Supply capacitor and startup resistor
VOUT	2	Analog output	+3.3V (TD220) or +5V (TD221) voltage regulator
IN	4	Digital input	Input signal for gate drive
GATE	5	Analog output	Gate drive output
GND	6	Power supply	Signal ground
VSUP	7	Power supply	Charge pump input
VCAP	8	Power supply	Capacitor for charge pump

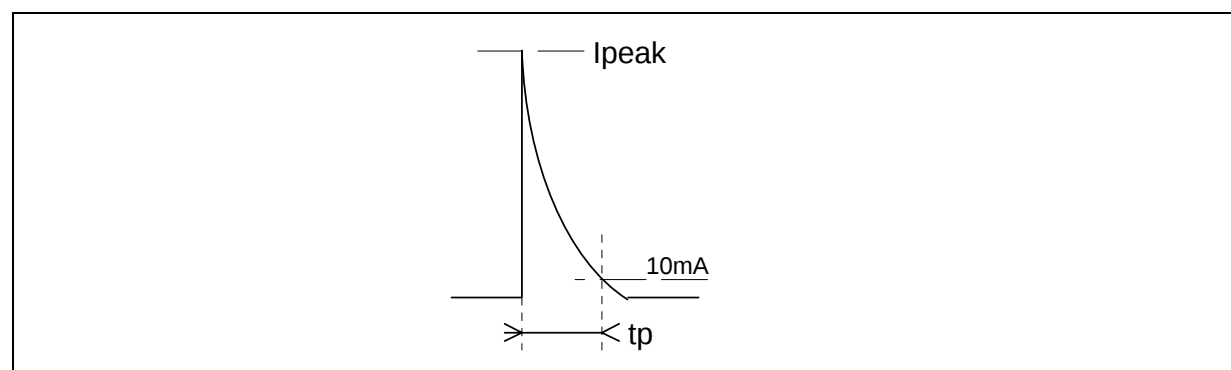
2 ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
VCC	DC Supply Voltage ($I_{CC} < 5\text{mA}$)	-0.3 to selflimit	V
Vout	Voltage on GATE and VCAP pins	-0.3 to VCC+0.3	V
Vin	Voltage on IN and VOUT pins	-0.3 to 7	V
Isup	Continuous current in VSUP pin	-200 to 200	mA
Ipeak	Peak current in VSUP pin ($t_p \leq 1\mu\text{s}$, $f \leq 150\text{kHz}$, see waveform below)	-1.0 to 1.0	A
Pd	Power dissipation	500	mW
Tstg	Storage temperature	-55 to 150	°C
Tj	Maximum Junction Temperature	150	°C
Rhja	Thermal Resistance Junction-Ambient	150	°C/W
Rhjc	Thermal Resistance Junction-Case	40	°C/W
ESD	Electrostatic discharge (HBM)	2	kV

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
VCC	Supply Voltage	UVLO to 17	V
Isup	Continuous current in VSUP pin	0 to 200	mA
Ipeak	Peak current in VSUP pin ($t_p \leq 1\mu\text{s}$, $f \leq 150\text{kHz}$, see waveform below)	-1.0 to 1.0	A
Tj	Junction Temperature	-25 to 125	°C

Typical waveform of current in VSUP pin



3 ELECTRICAL CHARACTERISTICS

Tamb = 25°C, VCC=13V unless otherwise specified

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Supply						
Icc	Supply current	no load at any pin, Vin<1V Tamb=25°C -25°C<Tj<125°C		0.7	1.0 1.2	mA mA
Icc2		1nF GATE load, 300kHz IN signal	4	5	6	mA
Istby	Standby current	UVLO active Tamb=25°C -25°C<Tj<125°C		160	230	μA μA
Vclamp	Clamp voltage	Icc<5mA	20	22	24	V
Input						
Vton	IN Turn-on Threshold Voltage		1.8		2.1	V
Vtoff	IN Turn-off Threshold Voltage		1.0		1.3	V
Vh	IN Hysteresis		0.5			V
Iinpl	IN Input current low	Vin<0.5V			20	μA
Iinph	IN Input current high	Vin=3.3V			100	μA
Voltage regulator						
Vout	Voltage reference	Iout=10mA TD220 TD221	3.20 4.85	3.30 5	3.40 5.15	V V
RegLoad	Load Regulation	Iout change from 10mA to 25mA			50	mV
Ipeak	Peak output current	Vout=1V	100			mA
dVout	Temperature coefficient	Iout=10mA			250	ppm/°C
Cout	Allowed capacitive load - Note 1	Iout=10mA	0.1		1	μF
Ileak	Leakage current in UVLO state	Vout=1V			10	μA
Vrip	Ripple rejection - Note 1	f=100Hz f=10kHz	40 20			dB dB
Vnoise	Noise voltage	100Hz<f<100kHz		1		mV
tstartup	Startup time (Vout>3.1V)	Cout=1μF			0.1	ms
tsettle	Settling time (1% final value)	Cout=1μF		2		ms
Two Point Regulator (TPR)						
VTPRON	Turn-on level				13.6	V
VTPROff	Turn-off level		12.4			V
VTPRH	Hysteresis	=VTPRON-VTPROff	0.23	0.29	0.35	V
VF	Forward voltage D1	IF=200mA			1.5	V

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Gate Output						
VOL	Output low voltage	I _{gate} =10mA			0.5	V
VOH	Output high voltage	I _{gate} =-10mA	V _{CC} -2.0			V
Isink	Output sink current	V _{gate} =6V T _j =25°C -25°C < T _j < 125°C	120	300		mA mA
Isrc	Output source current	V _{gate} =3V T _j =25°C -25°C < T _j < 125°C	60	150		mA mA
VOL2	Output low voltage in UVLO state	V _{cc} =6V, I _{gate} =1mA			2	V
tgmin	Minimum output pulse width ¹	C _{gate} =10pF			80	ns
tpd	IN to GATE propagation delay			200		ns
Under Voltage Lockout (UVLO)						
UVLOH	UVLO top threshold				15	V
UVLOL	UVLO bottom threshold		7.8		8.7	V
Vhyst	UVLO Hysteresis	V _{hyst} =UVLOH-UVLOL	5			V

1) Not 100% tested. Guaranteed by design.

4 TIMING DIAGRAMS

Fig. 1: Power up and power down

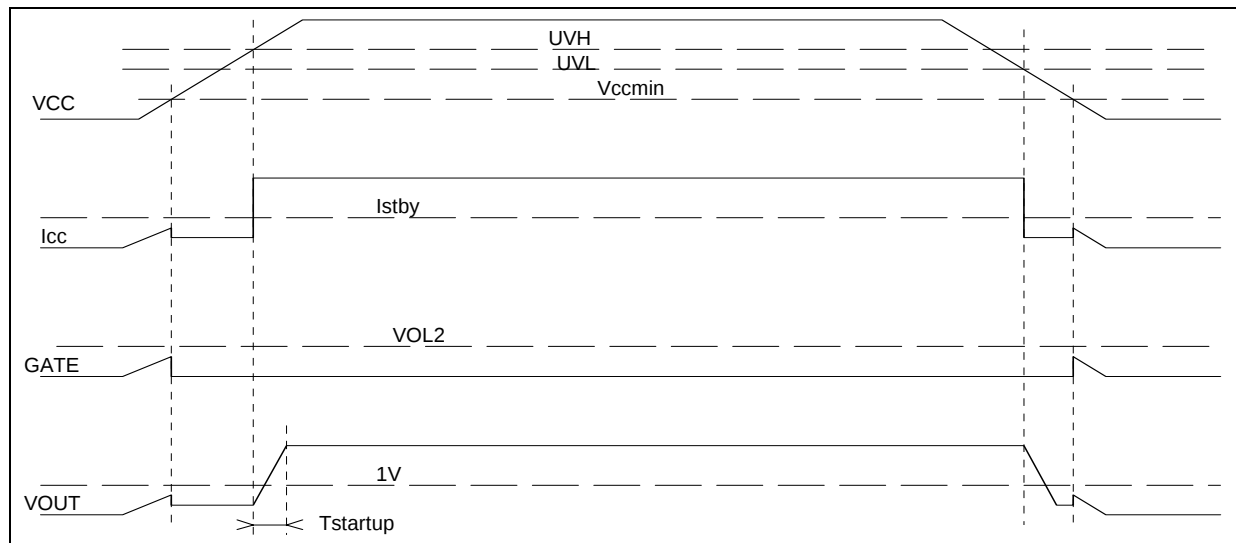
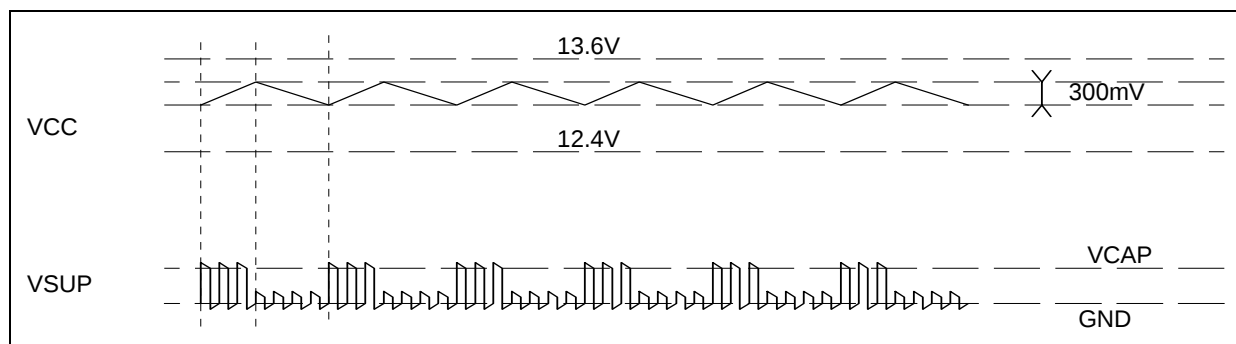
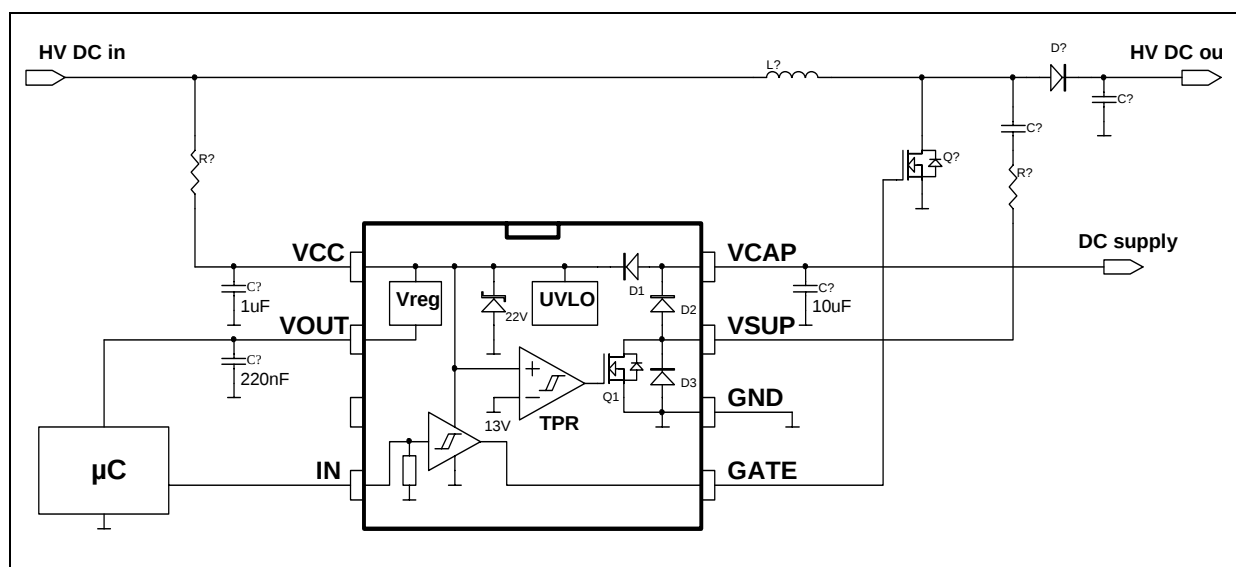


Fig. 2: Two point regulator



APPLICATION DIAGRAM



5 TYPICAL PERFORMANCE CURVES

Fig. 3: Supply Current vs Temperature

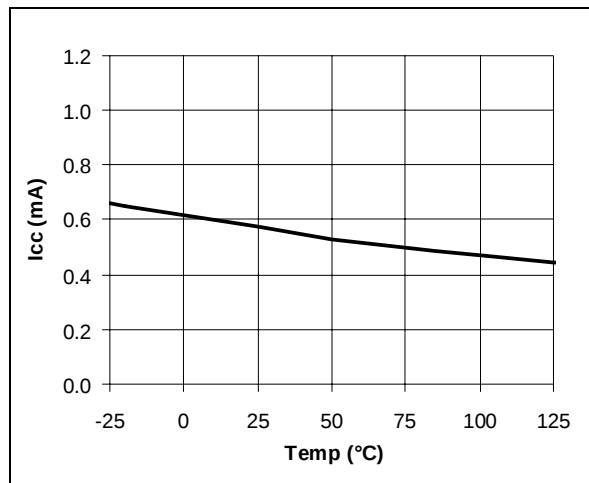


Fig. 6: Standby Current vs Temperature

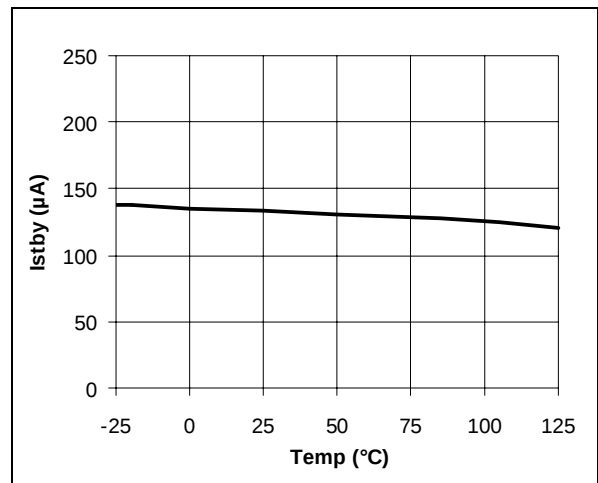


Fig. 4: Gate Drive Sink Current vs Temperature

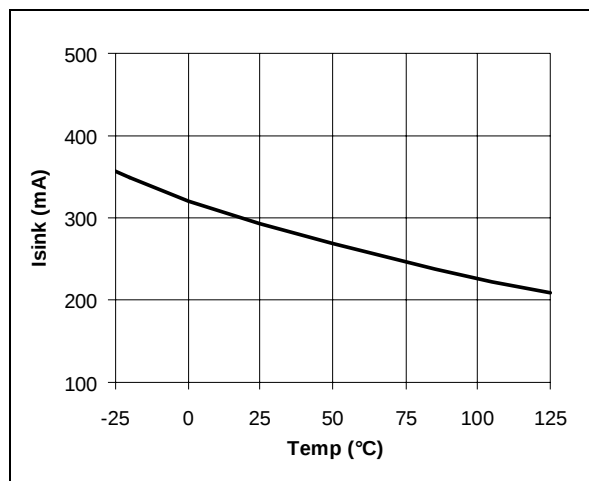


Fig. 7: Gate Drive Source Current vs Temp.

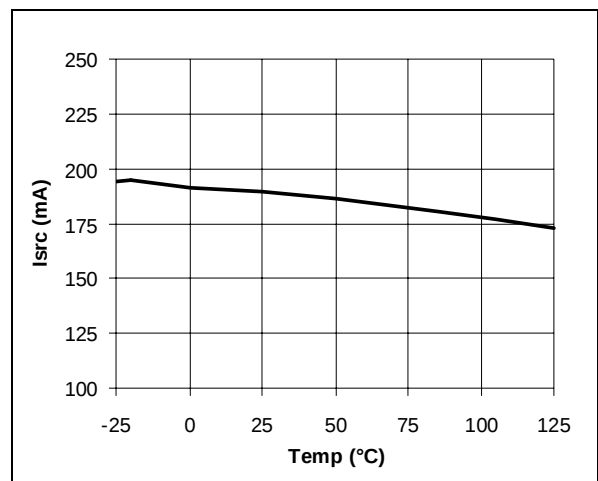
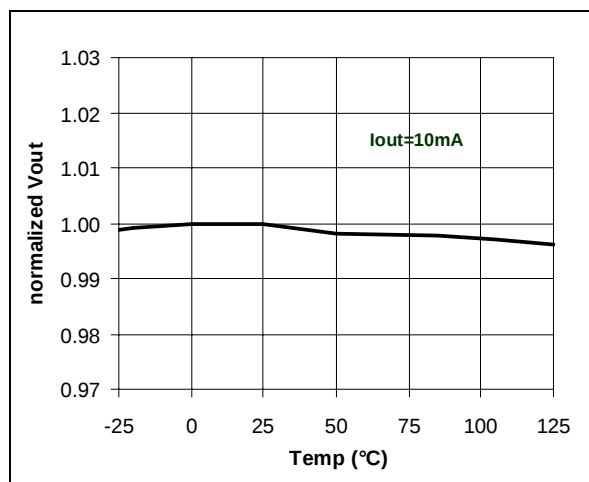


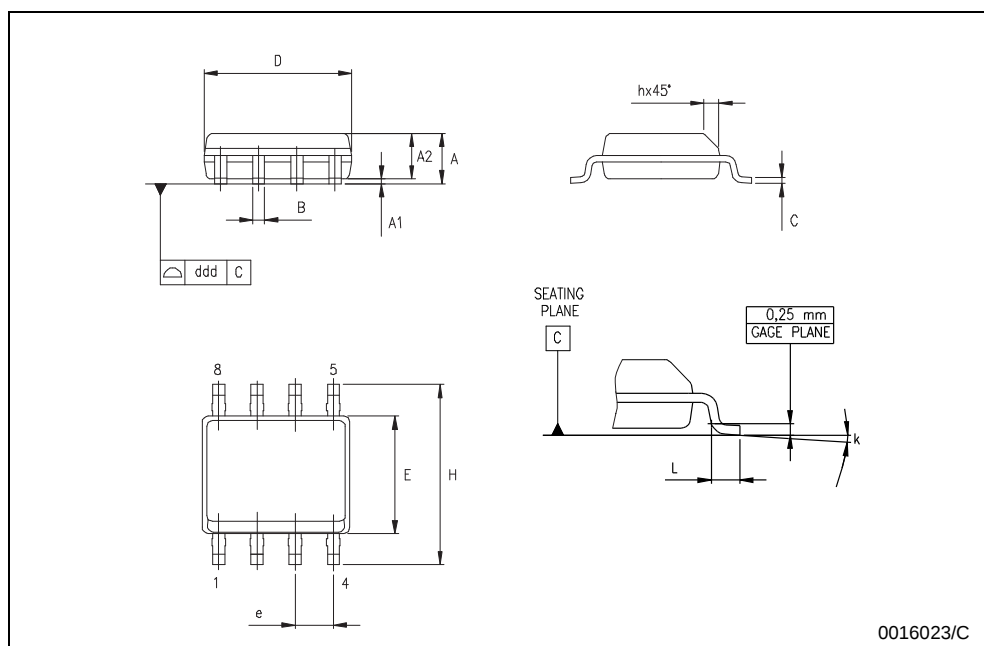
Fig. 5: Vreg Output Voltage vs Temperature



6 PACKAGE MECHANICAL DATA

SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics

© 2003 STMicroelectronics - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom
<http://www.st.com>