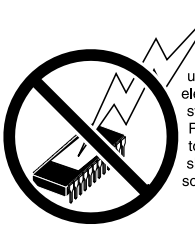
ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

V_{CC}.....-0.3V to 6.0V
V_{BATT}.....-0.3V to 6.0V
All Other Inputs (NOTE 1).....-0.3V to (V_{CC} to 0.3V)
Input Current:
V_{CC}.....250mA
V_{BATT}.....50mA
GND.....20mA
Output Current:
V_{OUT}.....Short-Circuit Protected for up to 10sec
All Other Inputs.....20mA

Rate of Rise, V_{CC}, V_{BATT}.....100V/µs
Continuous Power Dissipation.....500mW
Storage Temperature.....-65°C to +160°C
Lead Temperature(soldering,10sec).....+300°C
ESD Rating.....4KV



CAUTION:
ESD (ElectroStatic Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

ELECTRICAL CHARACTERISTICS

V_{cc}=4.75v to 5.50V for SP690A/SP802L/SP805L, V_{CC}=4.50V to 5.50V for SP692A/SP802M/SP805M, V_{BATT}=2.80V, T_A=T_{MIN} to T_{MAX}, typical specified at 25°C, unless otherwise noted.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Operating Voltage Range, V_{CC} or V_{BATT}, Note 2	0		5.5	Volts	
Supply Current, I_{SUPPLY},		35	60	µA	excluding I_{OUT}
I_{SUPPLY} in Battery Backup Mode, V_{CC} = 0V, V_{BATT} = 2.8V		0.001	0.6	µA	
V_{BATT} Standby Current, NOTE 3	-0.1		0.02	µA	V_{CC} > V_{BATT} + 0.2V
V_{OUT} Output	V_{CC} - 0.1	V_{CC} - 0.03 V_{CC} - 0.15		Volts	I_{OUT} = 50mA I_{OUT} = 250mA
V_{OUT} in Battery-Backup Mode V_{CC} < V_{BATT} - 0.2V	V_{BATT} -0.15	V_{BATT} - 0.04 V_{BATT} - 0.20		Volts	I_{OUT} = 5mA I_{OUT} = 25mA
Battery Switch Threshold, V_{CC} to V_{BATT}		20 -20		mV	Power-up Power-down
Battery Switchover Hysteresis		40		mV	Peak to Peak
Reset Threshold	4.50 4.25 4.55 4.30	4.65 4.40	4.75 4.50 4.70 4.45	Volts	SP690A, SP802L, SP805L SP692A, SP802M, SP805M SP802L, T_A = +25° C, V_{CC} falling SP802M, T_A = +25° C, V_{CC} falling

ELECTRICAL CHARACTERISTICS

V_{cc}=4.75v to 5.50V for SP690A/SP802L/SP805L, V_{CC}=4.50V to 5.50V for SP692A/SP802M/SP805M, V_{BATT}=2.80V, T_A=T_{MIN} to T_{MAX}, typical specified at 25°C, unless otherwise noted.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Reset Threshold Hysteresis		40		mV	Peak to Peak
Reset Pulse Width, t_{RS}	140	200	280	ms	
$\overline{RESET}$ Output Voltage, NOTE 5	V_{CC} - 1.5 	 0.1 0.004	 0.4 0.3	 Volts 	I_{SOURCE} = 800µA I_{SINK} = 3.2mA I_{SINK} = 50µA, V_{CC} = 1.0
RESET Output Voltage, NOTE 6	0.8 V_{CC} - 1.5 	 0.1	 0.4	 Volts 	I_{SOURCE} = 4µA, V_{CC} = 1.0V, I_{SOURCE} = 800µA I_{SINK} = 3.2mA
Watchdog Timeout, t_{WD}	1.00	1.60	2.25	sec	
WDI Pulse Width, t_{WP} NOTE 7	50			ns	V_{IL} = 0.4V, V_{IH} = (0.8)(V_{CC})
WDI Input Threshold, V_{CC} = 5V, NOTE 4	 3.5		0.8	Volts	Logic low Logic high
WDI Input Current	 -150	50 -50	150	µA	WDI =V_{CC} WDI = 0V
PFI Input Threshold	1.200 1.225	1.250 1.250	1.300 1.275	Volts	SP690A/692A, SP805L/M SP802L/M
PFI Input Current	-25	0.01	25	nA	
$\overline{PFO}$ Output Voltage	V_{CC} - 1.5	 0.1	 0.4	Volts	I_{SOURCE} = 800µA I_{SINK} = 3.2mA

NOTE 1: The input voltage limits on PFI (pin 4) and WDI (pin 6) may be exceeded if the current into these pins is limited to less than 10 mA.
NOTE 2: Either V_{CC} or V_{BATT} can go to 0V if the other is greater than 2.0V.
NOTE 3: "-" equals the battery-charging current, "+" equals the battery-discharging current.
NOTE 4: WDI is guaranteed to be in an intermediate, non-logic level state if WDI is floating and V_{CC} is in the operating voltage range. WDI is internally biased to 35% of V_{CC} with an input impedance of 50KΩ.
NOTE 5: SP690A, SP692A, SP802L, and SP802M only.
NOTE 6: SP805L and SP805M only.
NOTE 7: WDI Minimum Rise/Fall time is 2µs.

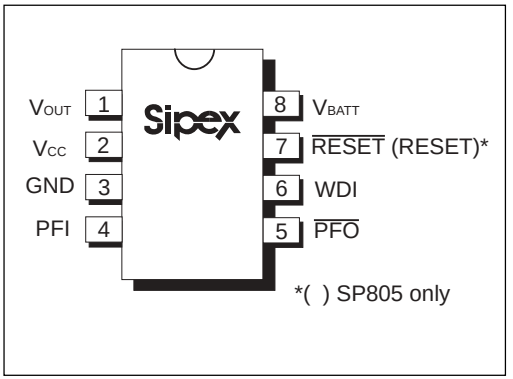


Figure 10. Pinout

PIN ASSIGNMENTS

Pin 1 —V_{OUT} — Output Supply Voltage. V_{OUT} connects to V_{CC} when V_{CC} is greater than V_{BATT} and V_{CC} is above the reset threshold. When V_{CC} falls below V_{BATT} and V_{CC} is below the reset threshold, V_{OUT} connects to V_{BATT}. Connect a 0.1µF capacitor from V_{OUT} to GND.

Pin 2 — V_{CC} — +5V Supply Input

Pin3 — GND — Ground reference for all signals

Pin 4 — PFI — Power-Fail Input. This is the noninverting input to the power-fail comparator. When PFI is less than 1.25V, $\overline{PFO}$ goes low. Connect PFI to GND or V_{OUT} when not used.

Pin 5 — $\overline{PFO}$ — Power-Fail Output.

Pin 6 — WDI — Watchdog Input. WDI is a three level input. If WDI remains high or low for 1.6sec, the internal watchdog timer triggers a reset. If WDI is left floating or connected to a high-impedance tri-state buffer, the watchdog feature is disabled. The internal watchdog timer clears whenever reset is asserted.

Pin 7 for **SP690A/692A/802 only** — $\overline{RESET}$ (Active Low)– Reset Output. $\overline{RESET}$ Output goes low whenever V_{CC} falls below the reset threshold or whenever WDI remains high or low longer than 1.6 seconds. $\overline{RESET}$ remains low for 200ms after V_{CC} crosses the reset threshold voltage on power-up or after being triggered by WDI.

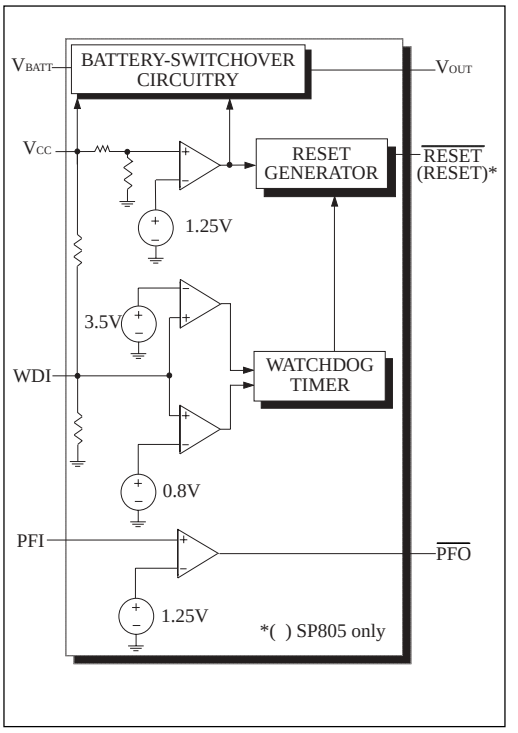
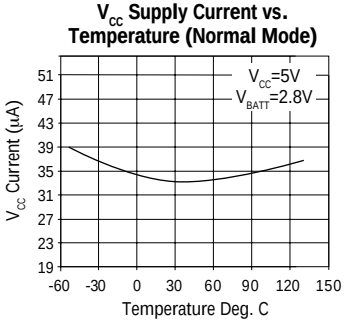


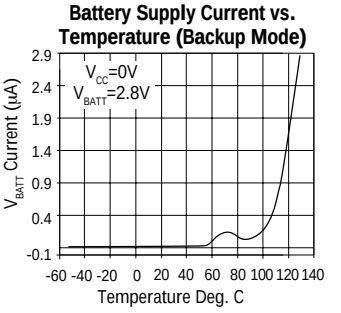
Figure 11. Internal Block Diagram

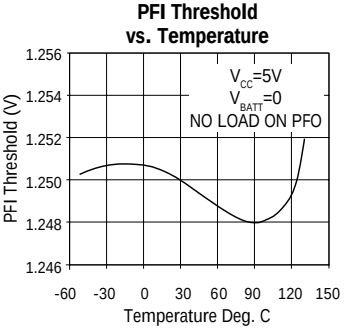
Pin 7 for **SP805 only** — RESET (Active High)– Reset Output is the inverse of $\overline{RESET}$; when RESET is asserted, the RESET output voltage = V_{CC} or V_{BATT}, whichever is higher.

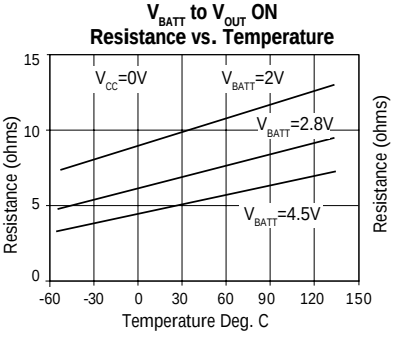
Pin 8 — V_{BATT} — Backup-Battery Input. When V_{CC} falls below the reset threshold, V_{BATT} will be switched to V_{OUT} if V_{BATT} is 20mV greater than V_{CC}. When V_{CC} rises 20mV above V_{BATT}, V_{OUT} will be reconnected to V_{CC}. The 40mV hysteresis prevents repeated switching if V_{CC} falls slowly.

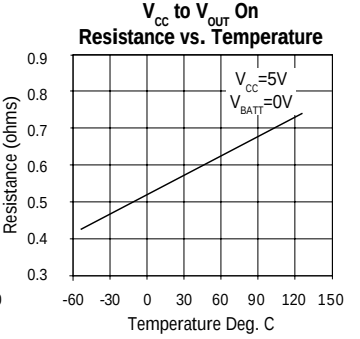
TYPICAL PERFORMANCE CHARACTERISTICS

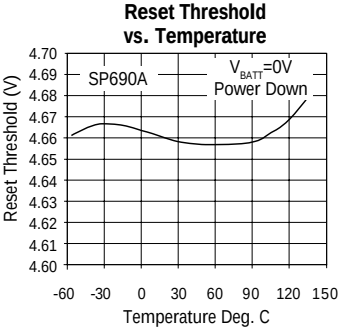


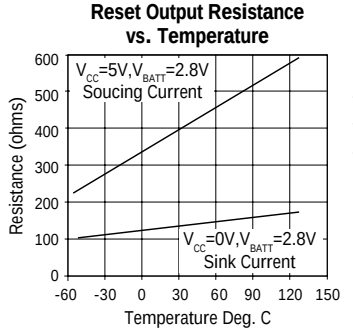


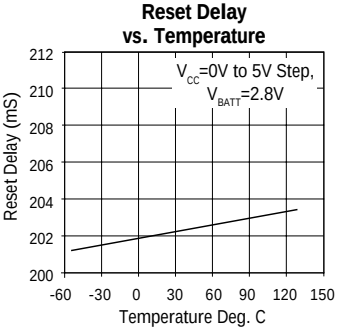


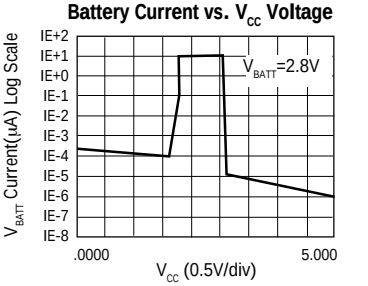












(25°C, unless otherwise noted)

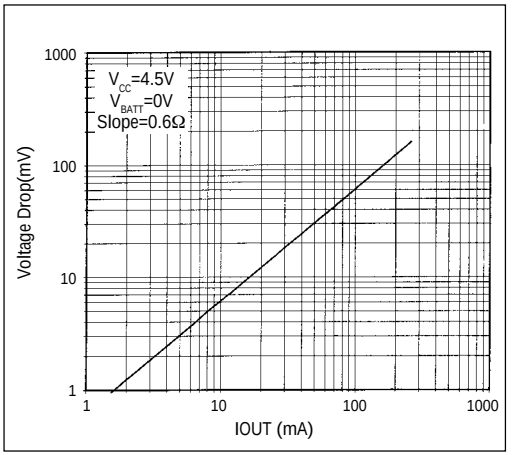


Figure 1. V_{CC} to V_{OUT} Vs. Output Current

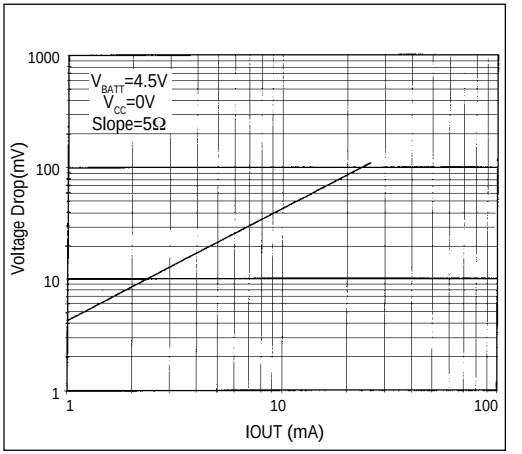


Figure 2. V_{BATT} to V_{OUT} Vs. Output Current

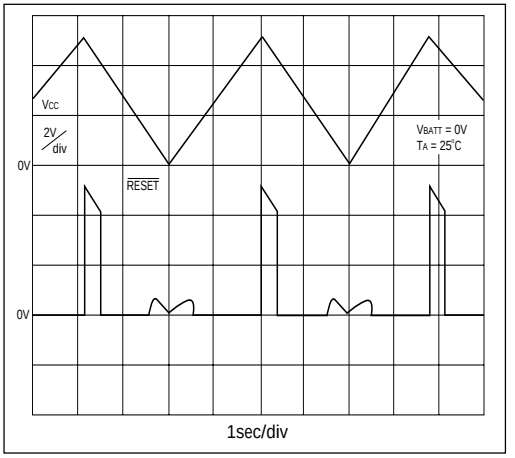


Figure 3A. SP690A $\overline{RESET}$ Output Voltage vs. Supply Voltage

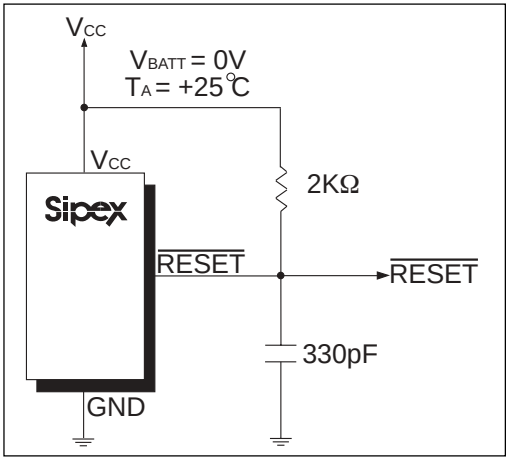


Figure 3B. Circuit for the SP690A/802L $\overline{RESET}$ Output Voltage vs. Supply Voltage

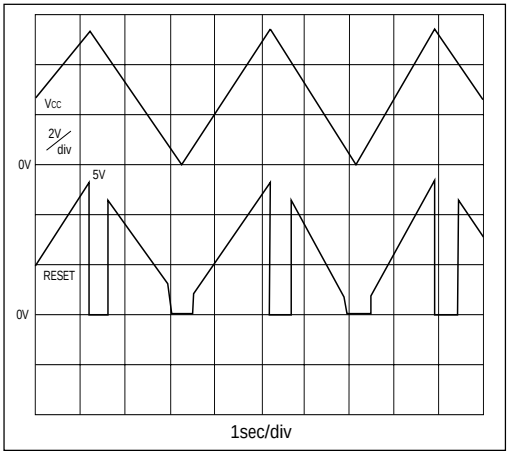


Figure 4A. SP805L RESET Output Voltage vs. Supply Voltage

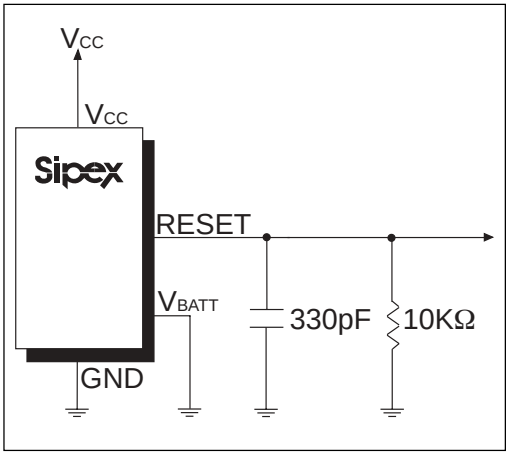


Figure 4B. Circuit for the SP805 RESET Output Voltage vs. Supply Voltage

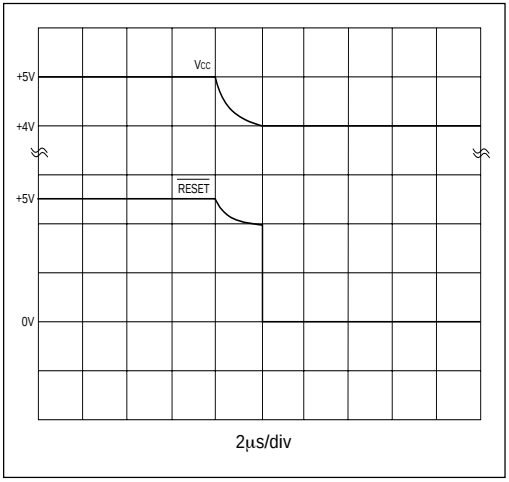


Figure 5A. SP690A $\overline{RESET}$ Response Time

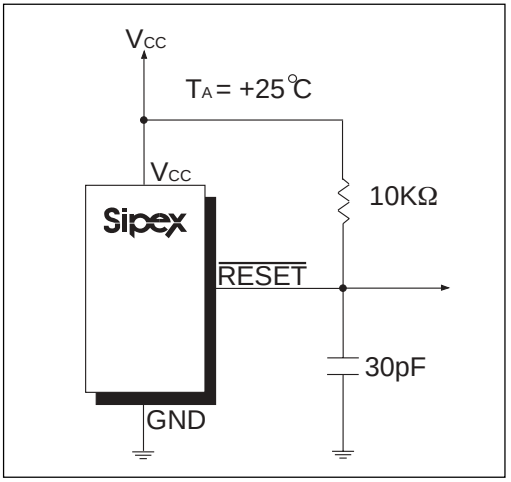


Figure 5B. Circuit for the SP690A/802L $\overline{RESET}$ Response Time

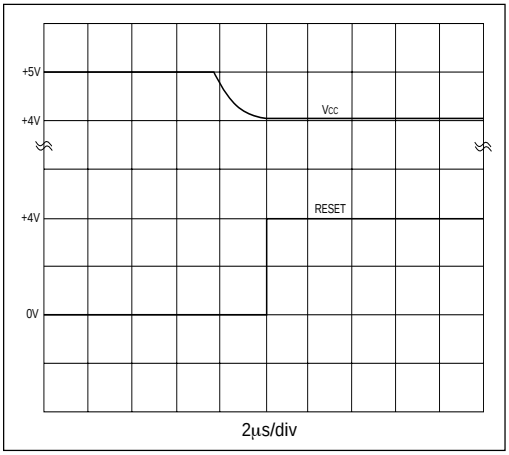


Figure 6A. SP805L RESET Response Time

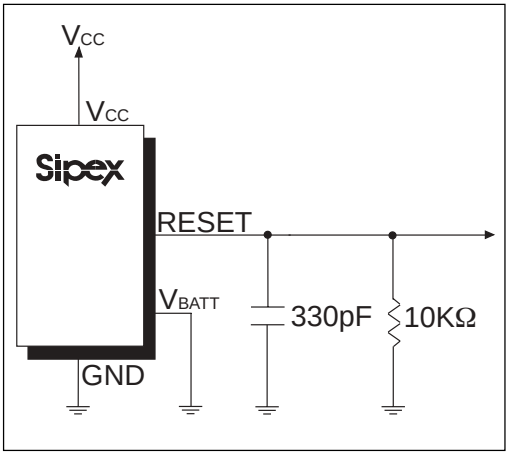


Figure 6B. Circuit for the SP805 RESET Response Time

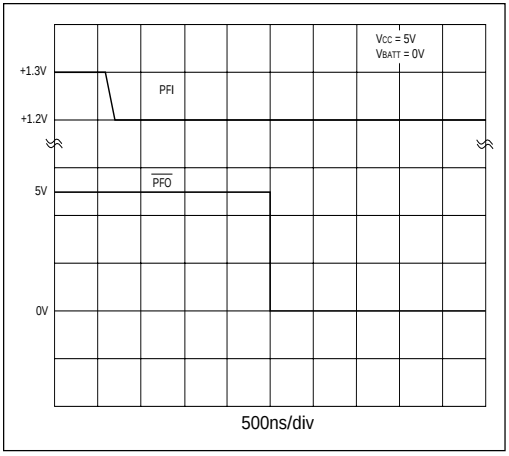


Figure 7A. Power-Fail Comparator Response Time (FALL)

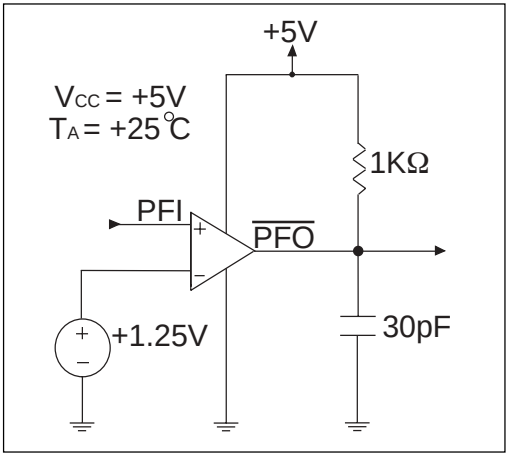


Figure 7B. Circuit for the Power-Fail Comparator Response Time (FALL)

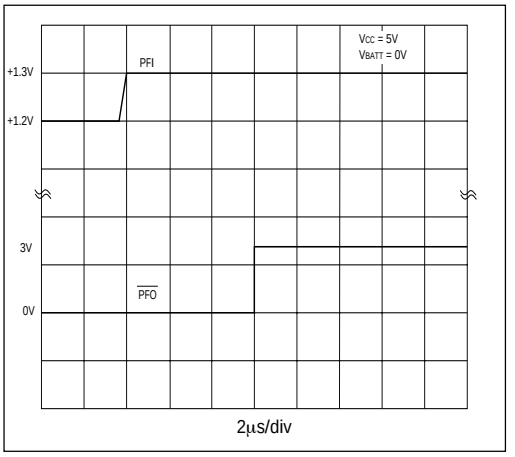


Figure 8A. Power-Fail Comparator Response Time (RISE)

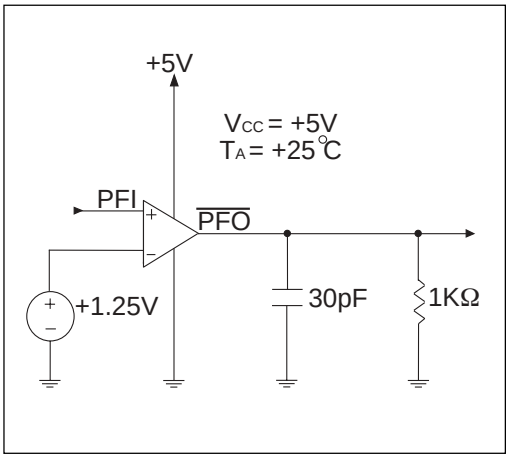


Figure 8B. Circuit for the Power-Fail Comparator Response Time (RISE)

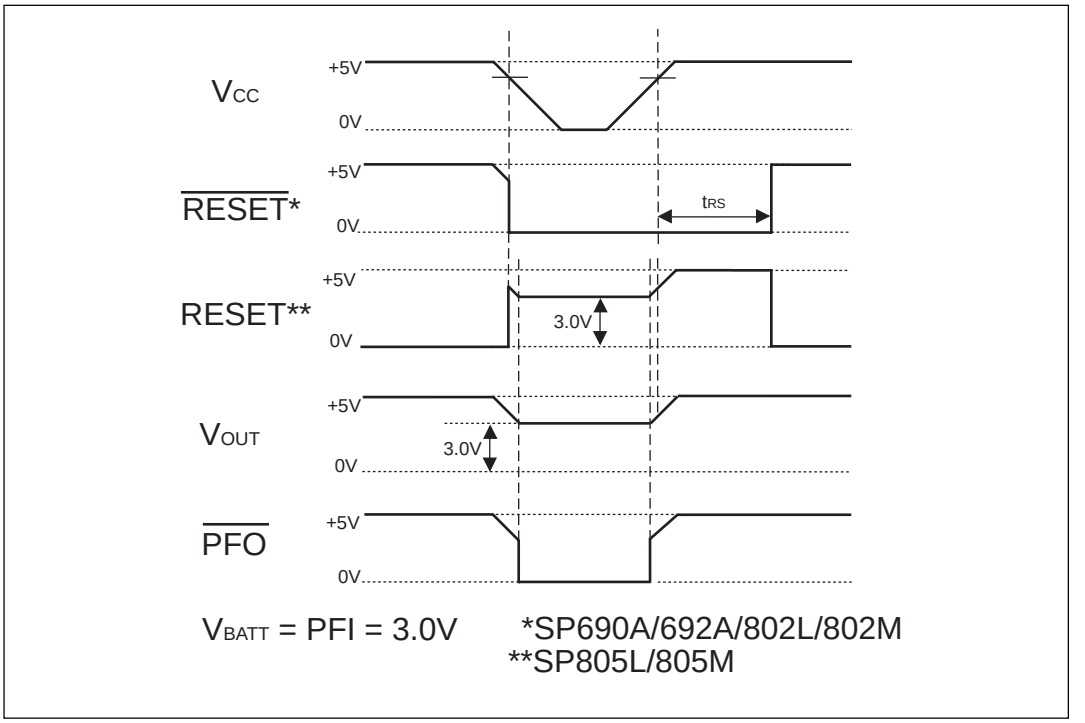


Figure 9. Timing Diagram

FEATURES

The **SP690A/692A/802L/802M/805L/805M** provide four key functions:
1. A battery backup switching for CMOS RAM, CMOS microprocessors, or other logic.
2. A reset output during power-up, power-down and brownout conditions.
3. A reset pulse if the optional watchdog timer has not been toggled within a specified time.
4. A 1.25V threshold detector for power-fail warning, low battery detection, or to monitor a power supply other than +5V.

The parts differ in their reset-voltage threshold levels and reset outputs. The **SP690A/802L/805L** generate a reset when the supply voltage drops below 4.65V. The **SP692A/802M/805M** generate a reset below 4.40V.

The **SP690A/692A/802L/802M/805L/805M** are ideally suited for applications in automotive systems, intelligent instruments, and battery-powered computers and controllers. All designs into an environment where it is critical to monitor the power supply to the µP and it's related digital components will find the **SSP690A/692A/802L/802M/805L/805M** ideal.

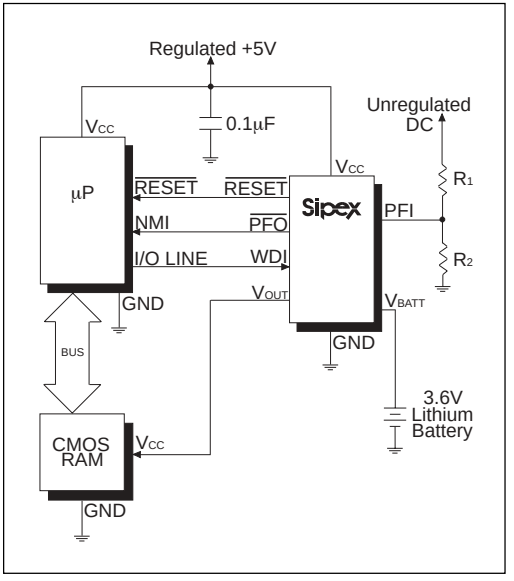


Figure 12. Typical Operating Circuit

THEORY OF OPERATION

The **SP690A/692A/802L/802M/805L/805M** microprocessor (µP) supervisory circuits monitor the power supplied to digital circuits such as microprocessors, microcontrollers, or memory. The series is an ideal solution for portable, battery-powered equipment that requires power supply monitoring. Implementing this series will reduce the number of components and overall complexity. The watchdog functions of this product family will continuously oversee the operational status of a system. The operational features and benefits of the **SP690A/692A/802L/802M/805L/805M** are described in more detail below.

Reset Output

The microprocessor's (µP's) reset input starts the µP in a known state. When the µP is in an unknown state, it should be held in reset. The **SP690A/SP692A/SP802** assert reset during power-up and prevent code execution errors during power-down or brownout conditions.

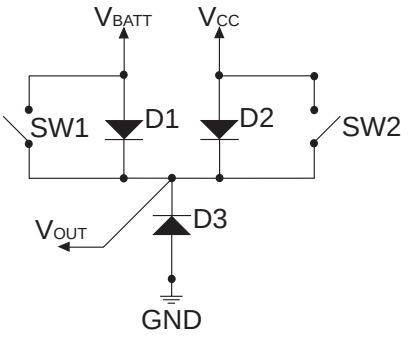
On power-up, once V_{CC} reaches 1V, $\overline{RESET}$ is guaranteed to be a logic low. As V_{CC} rises, $\overline{RESET}$ remains low. When V_{CC} exceeds the reset threshold, $\overline{RESET}$ will remain low for 200ms, *Figure 9*. If a brownout condition occurs and V_{CC} dips below the reset threshold, $\overline{RESET}$ is triggered. Each time $\overline{RESET}$ is triggered, it stays low for the reset pulse width interval. If a brownout condition interrupts a previously initiated reset pulse, the reset pulse continues for another 200ms. On power-down, once V_{CC} goes below the threshold, $\overline{RESET}$ is guaranteed to be logic low until V_{CC} drops below 1V.

$\overline{RESET}$ is also triggered by a watchdog timeout. If WDI remains either high or low for a period that exceeds the watchdog timeout period (1.6 sec), $\overline{RESET}$ pulses low for 200mS. As long as $\overline{RESET}$ is asserted, the watchdog timer remains clear. When $\overline{RESET}$ comes high, the watchdog resumes timing and must be serviced within 1.6sec. If WDI is tied high or low, a $\overline{RESET}$ pulse is triggered every 1.8sec (t_{WD} plus t_{RS}).

The **SP805L/M** active-high RESET output is the inverse of the **SP690A/SP692A/SP802** RESET output, and is valid with V_{CC} down to 1V. Some µP's, such as Intel's 80C51, require an active-high reset pulse.

Watchdog Input

The watchdog circuit monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within 1.6sec, a reset pulse is triggered. The internal 1.6sec timer is cleared by either a reset pulse or by floating the WDI input. As long as RESET is asserted or the WDI input is floating, the timer remains cleared and does not count. As soon as RESET is released and WDI is driven high or low, the timer starts counting. It can detect pulses as short as 50ns.



CONDITION	SW1	SW2
V_{CC} > Reset Threshold	Open	Closed
V_{CC} < Reset Threshold and V_{CC} > V_{BATT}	Open	Closed
V_{CC} < Reset Threshold and V_{CC} < V_{BATT}	Closed	Open

Reset Threshold = 4.65V in SP690A/802L/805L
Reset Threshold = 4.40V in SP692A/802M/805M

Figure 13. BACKUP-BATTERY Switchover Block Diagram

Power-Fail Comparator

The Power-Fail Comparator can be used as an under-voltage detector to signal the failing of a power supply (it is completely separate from the rest of the circuitry and does not need to be dedicated to this function). The PFI input is compared to an internal 1.25V reference. If PFI is less than 1.25V, $\overline{PFO}$ goes low. The external voltage divider drives PFI to sense the unregulated DC input to the +5V regulator. The voltage-divider ratio can be chosen such that the voltage at PFI falls below 1.25V just before the +5V regulator drops out. $\overline{PFO}$ then triggers an interrupt which signals the µP to prepare for power-down.

When V_{BATT} connects to V_{OUT}, the power-fail comparator is turned off and $\overline{PFO}$ is forced low to conserve backup-battery power.

Backup-Battery Switchover

In the event of a brownout or power failure, it may be necessary to preserve the contents of RAM. With a backup battery installed at V_{BATT}, the RAM is assured to have power if V_{CC} fails. As long as V_{CC} exceeds the reset threshold, V_{OUT} connects to V_{CC} through a 0.6Ω PMOS power switch. Once V_{CC} falls below the reset threshold, V_{CC} or V_{BATT}, whichever is higher, switches to V_{OUT}. V_{BATT} connects to V_{OUT} through a 5Ω switch only when V_{CC} is below the reset threshold and V_{BATT} is greater than V_{CC}.

When V_{CC} exceeds the reset threshold, it is connected to V_{OUT}, regardless of the voltage applied to V_{BATT} *Figure 13*. During this time, the diode (D1) between V_{BATT} and V_{OUT} will conduct current from V_{BATT} to V_{OUT} if V_{BATT} is more than .6V above V_{OUT}.

When V_{BATT} connects to V_{OUT}, backup mode is activated and the internal circuitry will be powered from the battery *Figure 14*. When V_{CC} is just below V_{BATT}, in the backup mode the current drawn from V_{BATT} will be typically 30µA. When V_{CC} drops to more than 1V below V_{BATT}, the internal switchover comparator shuts off and the supply current falls to less than 0.6µA.

SIGNAL	STATUS
V_{CC}	Disconnected from V_{OUT}
V_{OUT}	Connected to V_{BATT} through an internal 8Ω PMOS switch
V_{BATT}	Connected to V_{OUT}. Current drawn from the battery is less than 0.6µA, as long as $V_{CC} < V_{BATT}$ - 1V.
PFI	Power-fail comparator is disabled.
$\overline{PFO}$	Logic low
$\overline{RESET}$	Logic low
RESET	Logic high (SP805 only)
WDI	Watchdog timer is disabled

Figure 14. Input and Output Status in Battery-Backup Mode. *To enter the Battery-Backup mode, V_{CC} must be less than the Reset threshold and less than V_{BATT}.*

Using a High Capacity Capacitor as a Backup Power Source

VBATT has the same operating voltage range as VCC, and the battery-switchover threshold voltages are typically +20mV centered at VBATT, allowing use of a capacitor and a simple charging circuit as a backup source (see *Figure 16)*.

PART NUMBER	MAXIMUM BACKUP-BATTERY VOLTAGE [V]
SP690A SP802L SP805L	4.80
SP692A SP802M SP805M	4.55

Figure 15. Allowable BACKUP-BATTERY Voltages

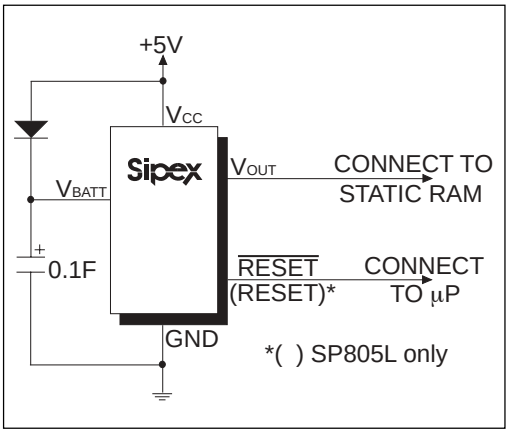


Figure 16. Backup Power Source Using High Capacity Capacitor with SP690A/802L/805L and a +5V ±5% Supply

If VCC is above the reset threshold and VBATT is 0.5V above VCC, current flows to VOUT and VCC from VBATT until the voltage at VBATT is less than 0.5V above VCC.

Leakage current through the capacitor charging diode and the **SP690A/SP802L/SP805L** internal power diode eventually discharges the capacitor to VCC. Also, if VCC and VBATT start from 0.5V above the reset threshold and power is lost at VCC, the capacitor on VBATT discharges through VCC until VBATT reaches the reset threshold; the **SP690A/SP802L/SP805L** then switches to battery-backup mode.

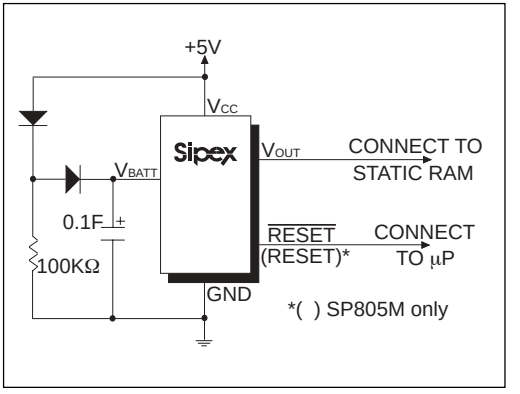


Figure 17. Backup Power Source Using High Capacity Capacitor with SP692A/802M/805M and a +5V ±10% Supply

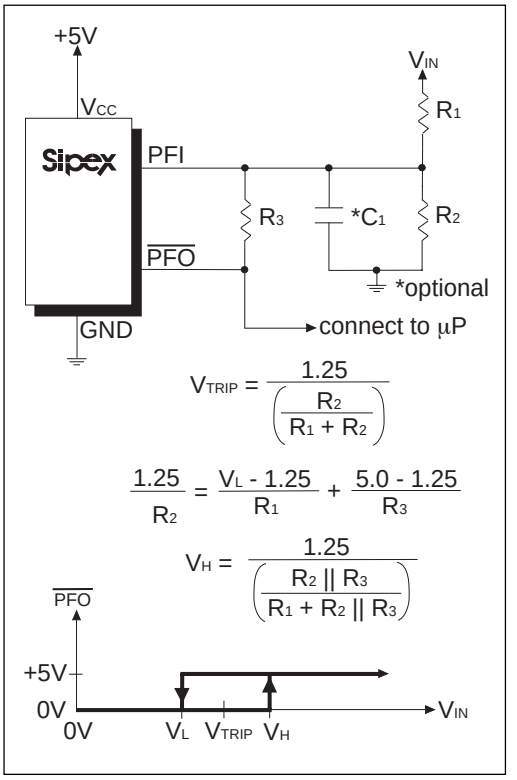


Figure 18. Adding Hysteresis to the POWER-FAIL Comparator

Allowable Backup Power-Source Batteries

Lithium batteries work very well as backup batteries due to very low self-discharge rate and high energy density. Single lithium batteries with open-circuit voltages of 3.0V to 3.6V are ideal. Any battery with an open-circuit voltage less than the minimum reset threshold plus 0.3V can be connected directly to the V_{BATT} input of this series with no additional circuitry; see FIGURE 12. However, batteries with open-circuit voltages that are greater than this value cannot be used for backup, as current is sourced into V_{OUT} through the diode *(D1 in Figure 13)* when V_{CC} is close to the reset threshold.

Operation Without a Backup Power Source

If a backup power source is not used, ground V_{BATT} and connect V_{OUT} to V_{CC}. Since there is no need to switch over to any backup power source, V_{OUT} does not need to be switched. A direct connection to V_{CC} eliminates any voltage drops across the switch which may push V_{OUT} below V_{CC}.

Replacing the Backup Battery

The backup battery can be removed while V_{CC} remains valid, without danger of triggering RESET/RESET. As long as V_{CC} stays above the reset threshold, battery-backup mode cannot be entered.

Adding Hysteresis to the Power-Fail Comparator

Hysteresis adds a noise margin to the power-fail comparator and prevents repeated triggering of PFO when V_{IN} is close to its trip point. *Figure 18* shows how to add hysteresis to the power-fail comparator. Select the ratio of R_1 and R_2 such that PFI sees 1.25V when V_{IN} falls to its trip point (V_{TRIP}). R_3 adds the hysteresis. It will typically be an order of magnitude greater (about 10 times) than R_1 or R_2. The current through R_1 and R_2 should be at least 1µA to ensure that the 25nA (max) PFI input current does not shift the trip point. R_3 should be larger than 10KΩ so it does not load down the PFO pin. Capacitor C1 adds additional noise rejection.

Monitoring a Negative Voltage

The power-fail comparator can be used to monitor a negative supply rail using the circuit of *Figure 19.* When the negative rail is valid, PFO is low. When the negative supply voltage drops, PFO goes high. This circuit's accuracy is affected by the PFI threshold tolerance, the V_{CC} voltage, and the resistors, R1 and R2.

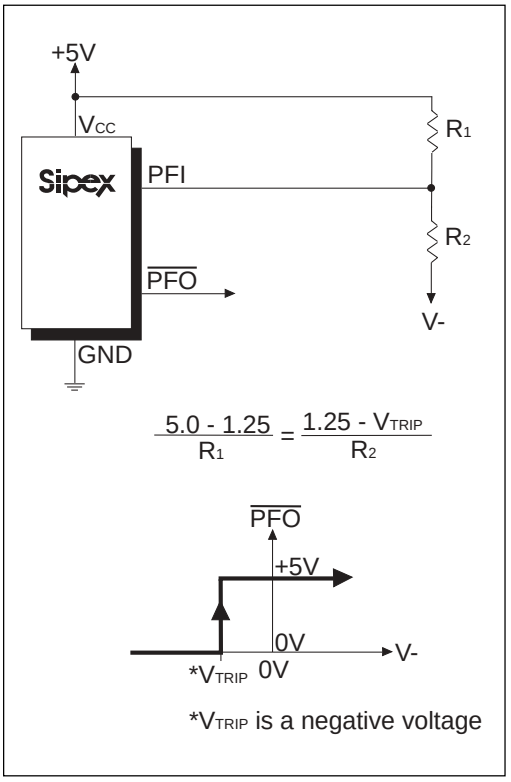


Figure 19. Monitoring a Negative Voltage

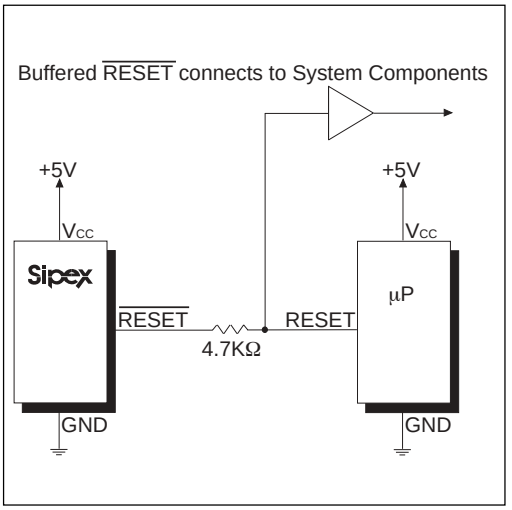
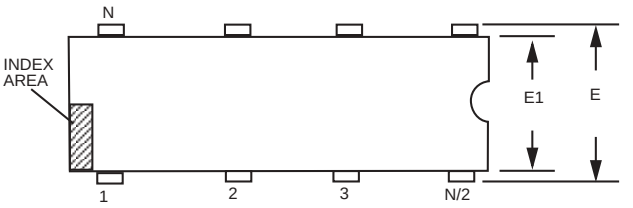
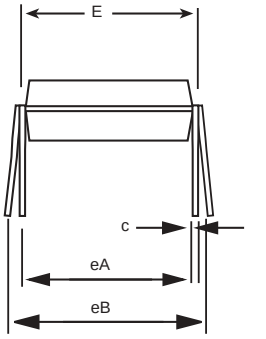


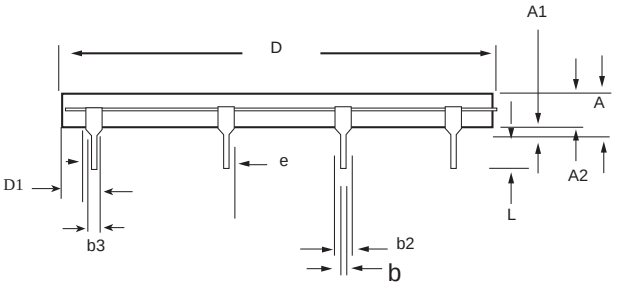
Figure 20. Interfacing to Microprocessors with Bidirectional RESET I/O

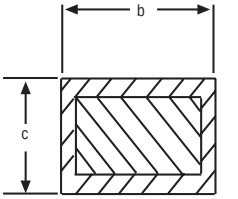
Interfacing to Microprocessors with Bidirectional Reset Pins

Microprocessors with bidirectional reset pins, such as the Motorola 68HC11 series, can contend with this series' RESET output. If, for example, the RESET output is driven high and the μP wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7KΩ resistor between the RESET output and the μP reset I/O, as in *Figure 20*. Buffer the RESET output to other system components.



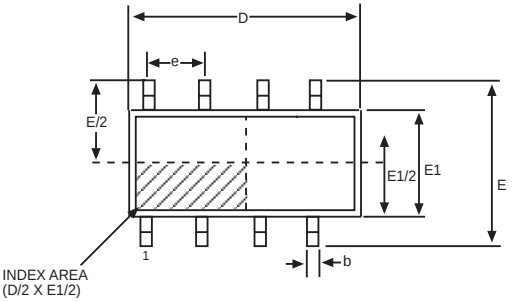




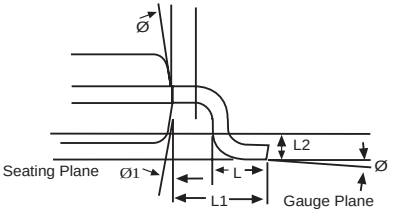


8 PIN PDIP JEDEC MS-001 (BA) Variation			
SYMBOL	MIN	NOM	MAX
A	-	-	0.21
A1	0.15	-	-
A2	0.115	0.13	0.195
b	0.014	0.018	0.022
b2	0.045	0.06	0.07
b3	0.3	0.039	0.045
c	0.008	0.01	0.014
D	0.355	0.365	0.4
D1	0.005	-	-
E	0.3	0.31	0.325
E1	0.24	0.25	0.28
e	.100 BSC		
eA	.300 BSC		
eB	-	-	0.43
L	0.115	0.13	0.15

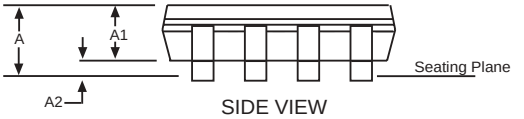
Note: Dimensions in (mm)



TOP VIEW



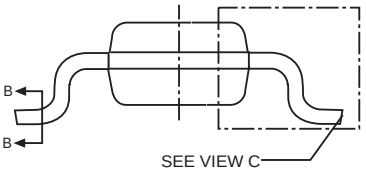
VIEW C

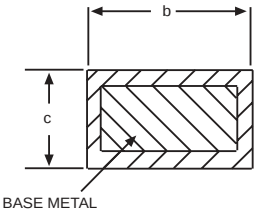


SIDE VIEW

8 Pin NSOIC JEDEC MO-012 (AA) Variation			
SYMBOL	MIN	NOM	MAX
A	1.35	-	1.75
A1	0.1	-	0.25
A2	1.25	-	1.65
b	0.31	-	0.51
c	0.17	-	0.24
D		4.90 BSC	
E		6.00 BSC	
E1		3.90 BSC	
e		1.27 BSC	
L	0.4	-	1.27
L1		1.04 REF	
L2		0.25 BSC	
ø	0º	-	8º
ø1	5º	-	15º

Note: Dimensions in (mm)





SECTION B-B
WITH PLATING

ORDERING INFORMATION

Model	Temperature Range	Package Types
SP690ACN	0°C to +70°C	8-Pin NSOIC
SP690ACN/TR	0°C to +70°C	8-Pin NSOIC
SP690ACP	0°C to +70°C	8-Pin PDIP
SP690AEN	-40°C to +85°C	8-Pin NSOIC
SP690AEN/TR	-40°C to +85°C	8-Pin NSOIC
SP690AEP	-40°C to +85°C	8-Pin PDIP
SP692ACN	0°C to +70°C	8-Pin NSOIC
SP692ACN/TR	0°C to +70°C	8-Pin NSOIC
SP692ACP	0°C to +70°C	8-Pin PDIP
SP692AEN	-40°C to +85°C	8-Pin NSOIC
SP692AEN/TR	-40°C to +85°C	8-Pin NSOIC
SP692AEP	-40°C to +85°C	8-Pin PDIP
SP802LCN	0°C to +70°C	8-Pin NSOIC
SP802LCN/TR	0°C to +70°C	8-Pin NSOIC
SP802LCP	0°C to +70°C	8-Pin PDIP
SP802LEN	-40°C to +85°C	8-Pin NSOIC
SP802LEN/TR	-40°C to +85°C	8-Pin NSOIC
SP802LEP	-40°C to +85°C	8-Pin PDIP
SP802MCN	0°C to +70°C	8-Pin NSOIC
SP802MCN/TR	0°C to +70°C	8-Pin NSOIC
SP802MCP	0°C to +70°C	8-Pin PDIP
SP802MEN	-40°C to +85°C	8-Pin NSOIC
SP802MEN/TR	-40°C to +85°C	8-Pin NSOIC
SP802MEP	-40°C to +85°C	8-Pin PDIP
SP805LCN	0°C to +70°C	8-Pin NSOIC
SP805LCN/TR	0°C to +70°C	8-Pin NSOIC
SP805LCP	0°C to +70°C	8-Pin PDIP
SP805LEN	-40°C to +85°C	8-Pin NSOIC
SP805LEN/TR	-40°C to +85°C	8-Pin NSOIC
SP805LEP	-40°C to +85°C	8-Pin PDIP
SP805MCN	0°C to +70°C	8-Pin NSOIC
SP805MCN/TR	0°C to +70°C	8-Pin NSOIC
SP805MCP	0°C to +70°C	8-Pin PDIP
SP805MEN	-40°C to +85°C	8-Pin NSOIC
SP805MEN/TR	-40°C to +85°C	8-Pin NSOIC
SP805MEP	-40°C to +85°C	8-Pin PDIP

Available in lead free packaging. To order add “-L” suffix to part number.

Example: SP802LCN/TR = standard; SP802LCN-L/TR = lead free

/TR = Tape and Reel

Pack quantity 2,500 for NSOIC.

CLICK HERE TO ORDER SAMPLES

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ANALOG EXCELLENCE

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