THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient (MOSFET)[b, d]	t ≤ 5 s	R_{thJA}	62	74	°C/W
Maximum Junction-to-Foot (Drain) (MOSFET)	Steady State	R_{thJF}	32	40	
Maximum Junction-to-Ambient (Schottky)[b, e]	t ≤ 5 s	R_{thJA}	77	95	
Maximum Junction-to-Foot (Drain) (Schottky)	Steady State	R_{thJF}	33	40	

Notes:
a. Based on T_C = 25 °C.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 5 s
d. Maximum under steady state conditions is 115 °C/W.
e. Maximum under steady state conditions is 130 °C/W.
f. Package limited.
g. See Solder Profile (www.vishay.com/doc?73257). The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed an is not required to ensure adequate bottom side soldering interconnection.
h. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = - 250 µA		- 20		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			3		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 0.6		- 1.5	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 12 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 20 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 20 V, V_{GS} = 0 V, T_J = 55 °C			- 10	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≤ 5 V, V_{GS} = - 10 V	- 15			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 10 V, I_D = - 3.7 A		0.070	0.084	Ω
		V_{GS} = - 4.5 V, I_D = - 3.2 A		0.090	0.108	
		V_{GS} = - 2.5 V, I_D = - 2.5 A		0.140	0.175	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 10 V, I_D = - 3.7 A		6		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = - 10 V, V_{GS} = 0 V, f = 1 MHz		330		pF
Output Capacitance	C_{oss}			80		
Reverse Transfer Capacitance	C_{rss}			57		
Total Gate Charge	Q_g	V_{DS} = - 10 V, V_{GS} = - 10 V, I_D = - 3.7 A		8	12	nC
		V_{DS} = - 10 V, V_{GS} = - 4.5 V, I_D = - 3.7 A		4	6	
Gate-Source Charge	Q_{gs}			0.8		
Gate-Drain Charge	Q_{gd}			1.4		
Gate Resistance	R_g	f = 1 MHz	1.2	6	12	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 10 V, R_L = 3.4 Ω $I_D \cong$ - 2.9 A, V_{GEN} = - 10 V, R_g = 1 Ω		3	6	ns
Rise Time	t_r			10	20	
Turn-Off DelayTime	$t_{d(off)}$			16	24	
Fall Time	t_f			8	15	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 10 V, R_L = 3.4 Ω $I_D \cong$ - 2.9 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		18	27	
Rise Time	t_r			40	60	
Turn-Off DelayTime	$t_{d(off)}$			18	27	
Fall Time	t_f			10	15	

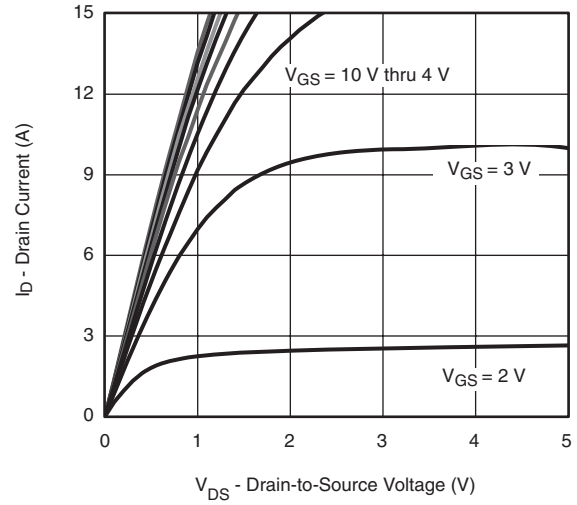
SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			- 1.2	A
Pulse Diode Forward Current	I_{SM}				- 15	
Body Diode Voltage	V_{SD}	I_S = - 2.9 A, V_{GS} = 0 V		- 0.75	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = - 2.9 A, dI/dt = 100 A/µs, T_J = 25 °C		23	35	ns
Body Diode Reverse Recovery Charge	Q_{rr}			14	21	nC
Reverse Recovery Fall Time	t_a			11		ns
Reverse Recovery Rise Time	t_b			12		

Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

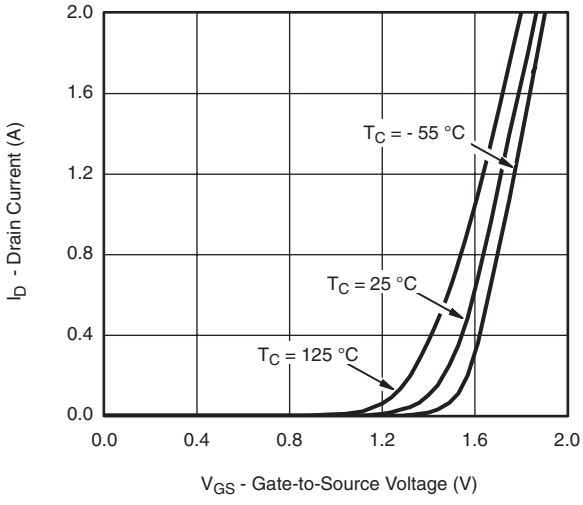
SCHOTTKY SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Forward Voltage Drop	V_F	I_F = 1 A		0.42	0.50	V
		I_F = 1 A, T_J = 125 °C		0.36	0.43	
Maximum Reverse Leakage Current	I_{rm}	V_r = 5 V		0.015	0.08	mA
		V_r = 5 V, T_J = 85 °C		0.50	5.00	
		V_r = 20 V		0.02	0.10	
		V_r = 20 V, T_J = 85 °C		0.7	7.00	
		V_r = 20 V, T_J = 125 °C		5	50	
Junction Capacitance	C_T	V_r = 10 V		60		pF

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

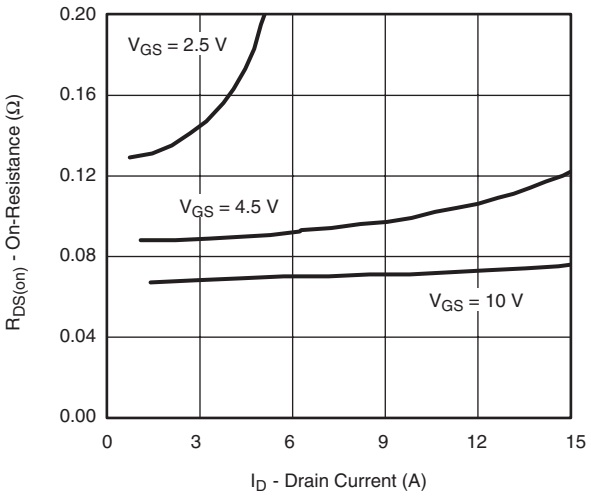
MOSFET TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted



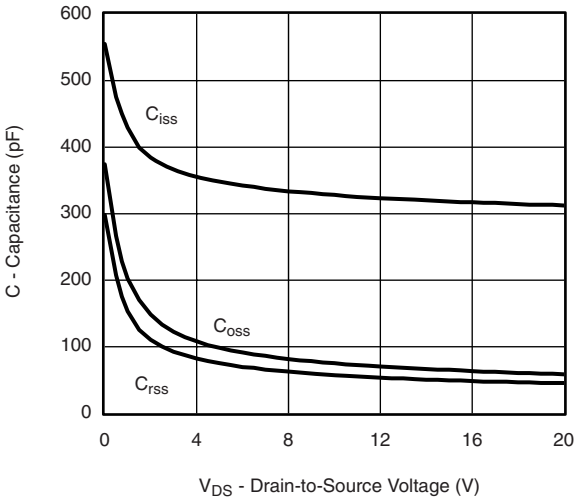
Output Characteristics



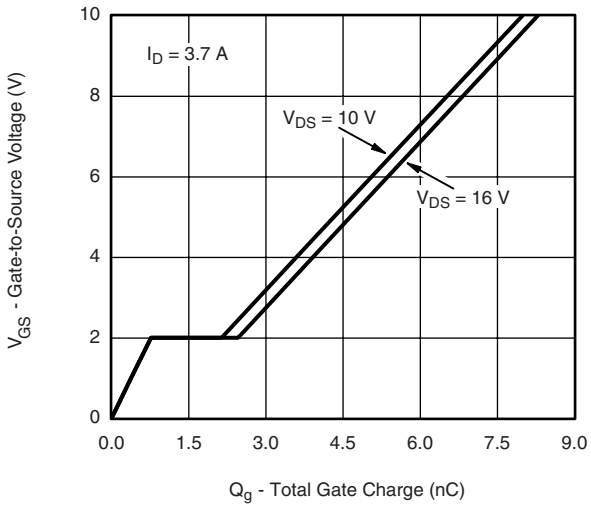
Transfer Characteristics



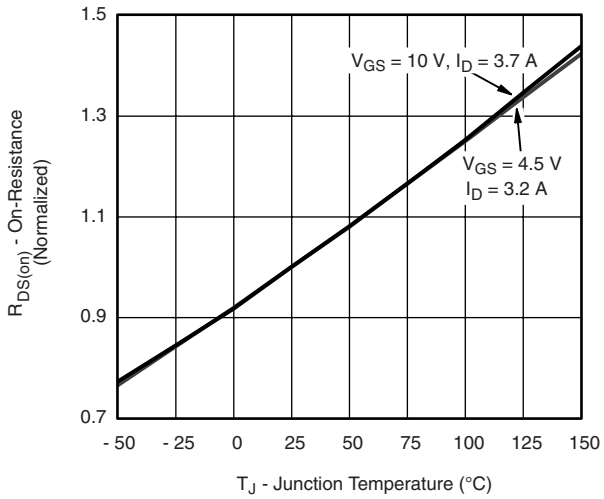
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

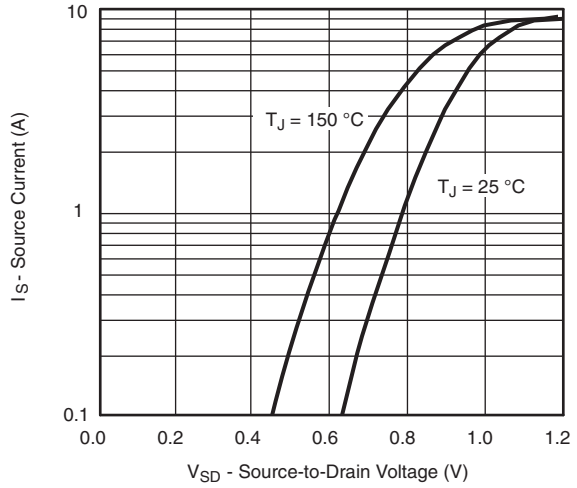


Gate Charge

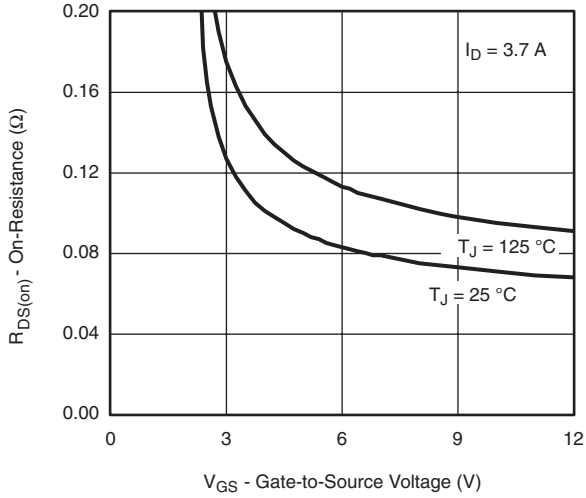


On-Resistance vs. Junction Temperature

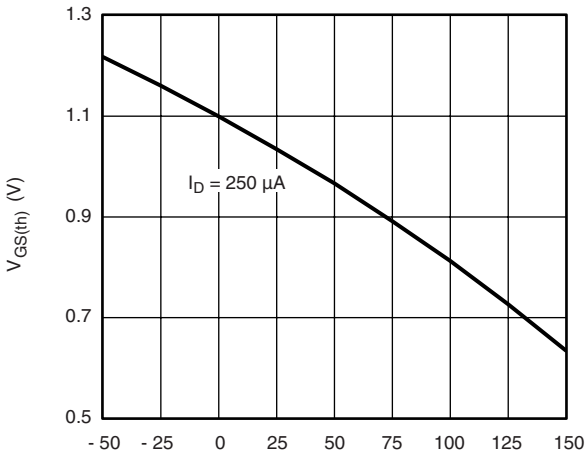
MOSFET TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted



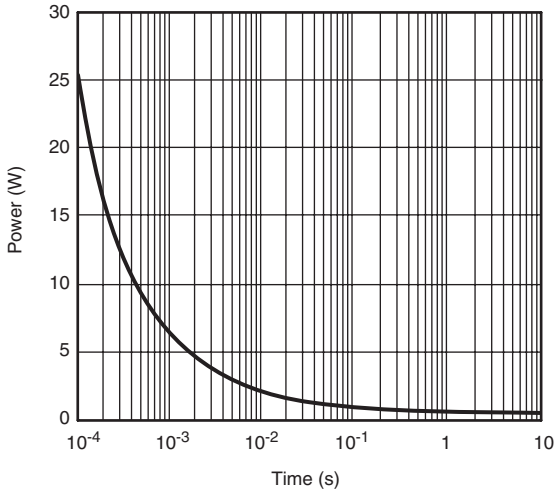
Soure-Drain Diode Forward Voltage



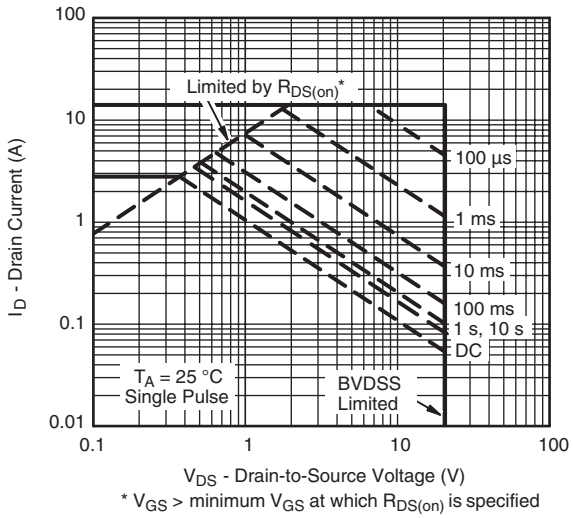
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



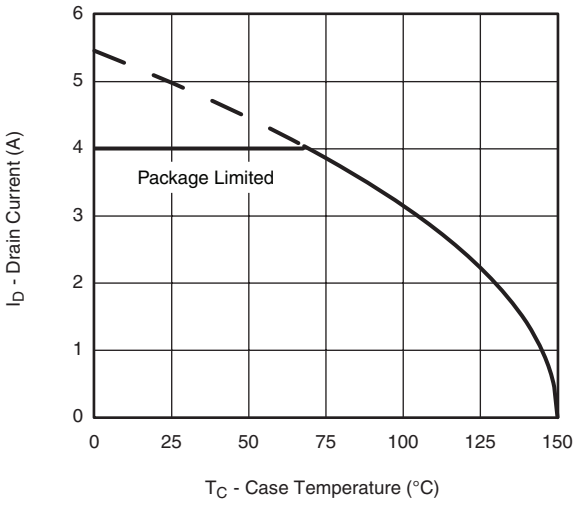
Single Pulse Power, Junction-to-Ambient



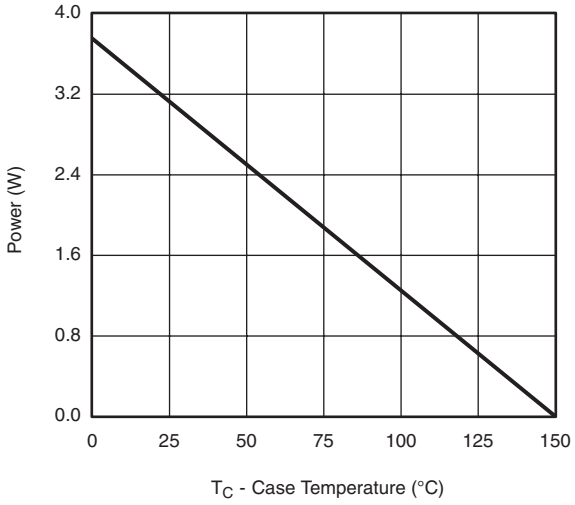
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Case

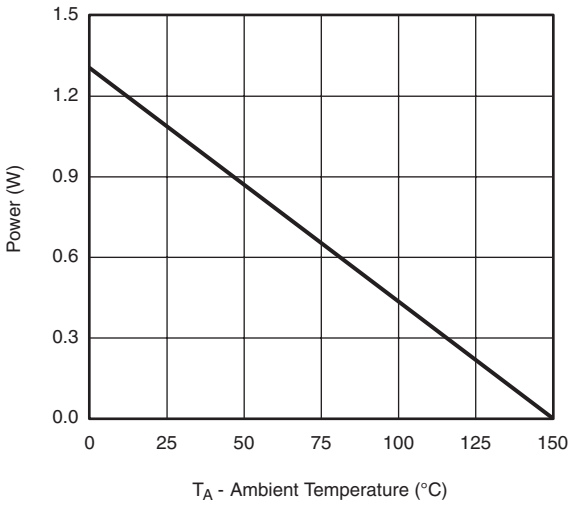
MOSFET TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted



Current Derating*



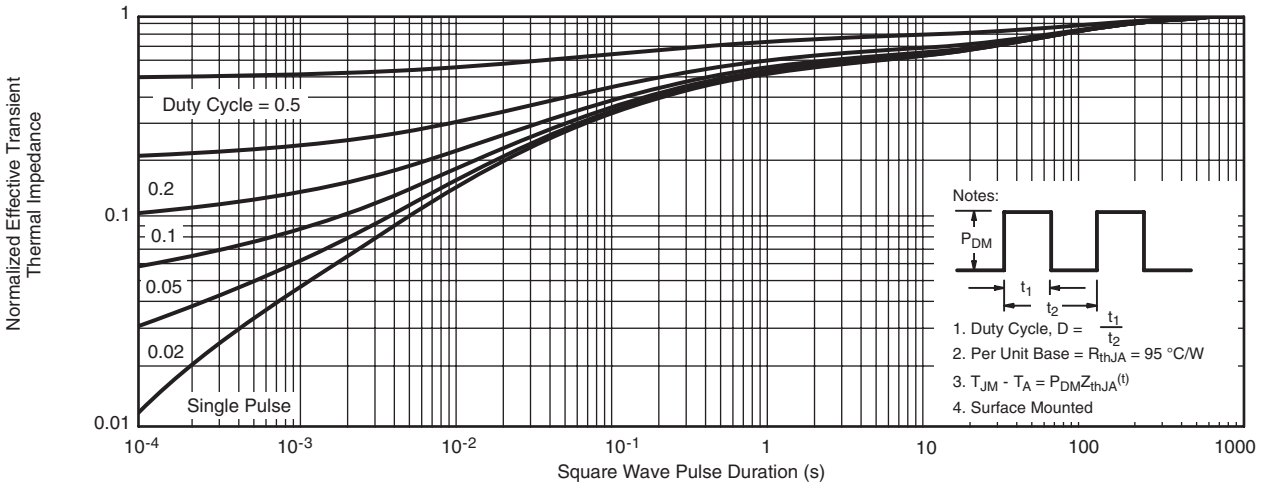
Power Derating, Junction-to-Foot



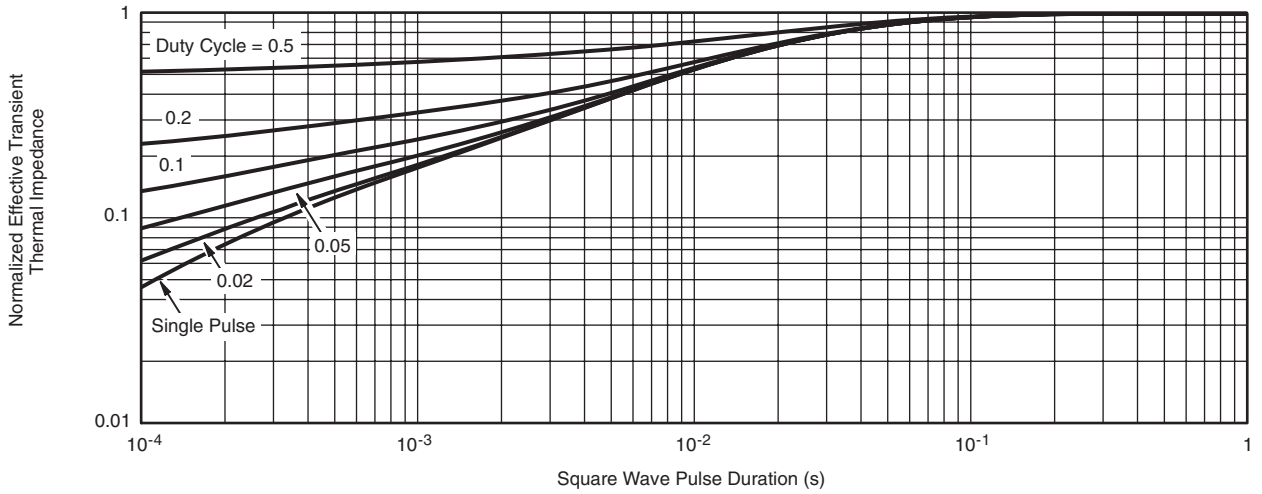
Power Derating, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

MOSFET TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted

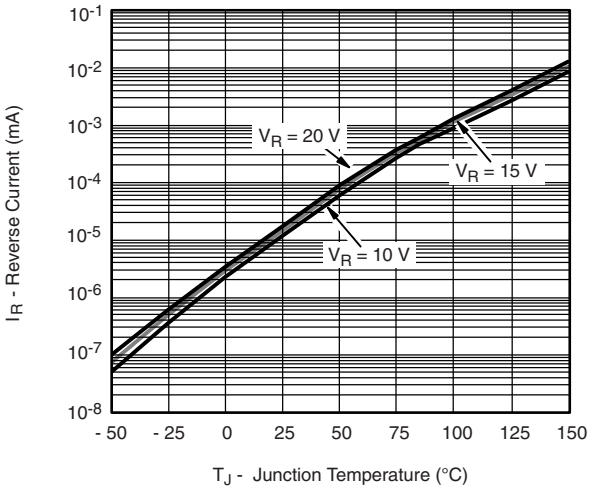


Normalized Thermal Transient Impedance, Junction-to-Ambient

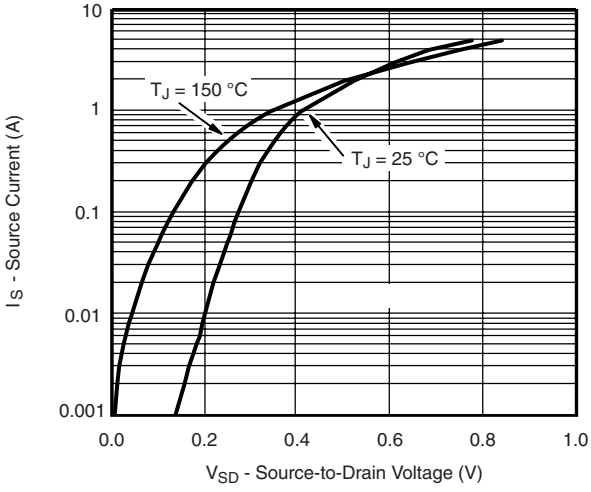


Normalized Thermal Transient Impedance, Junction-to-Foot

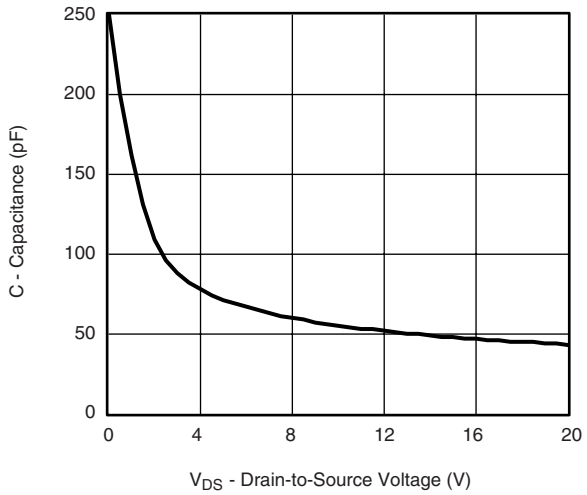
SCHOTTKY TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted



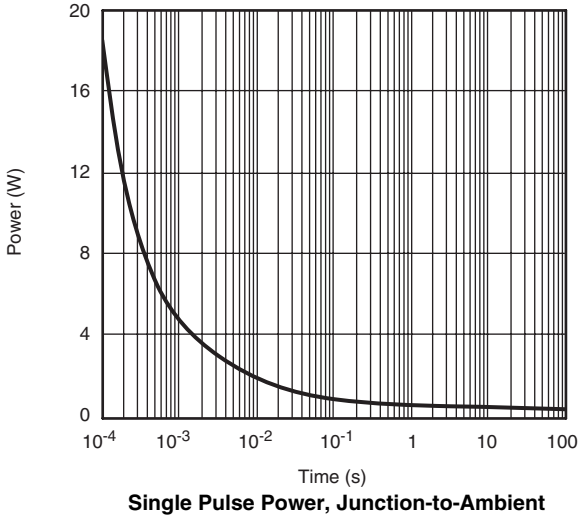
Reverse Current vs. Junction Temperature



Forward Diode Voltage

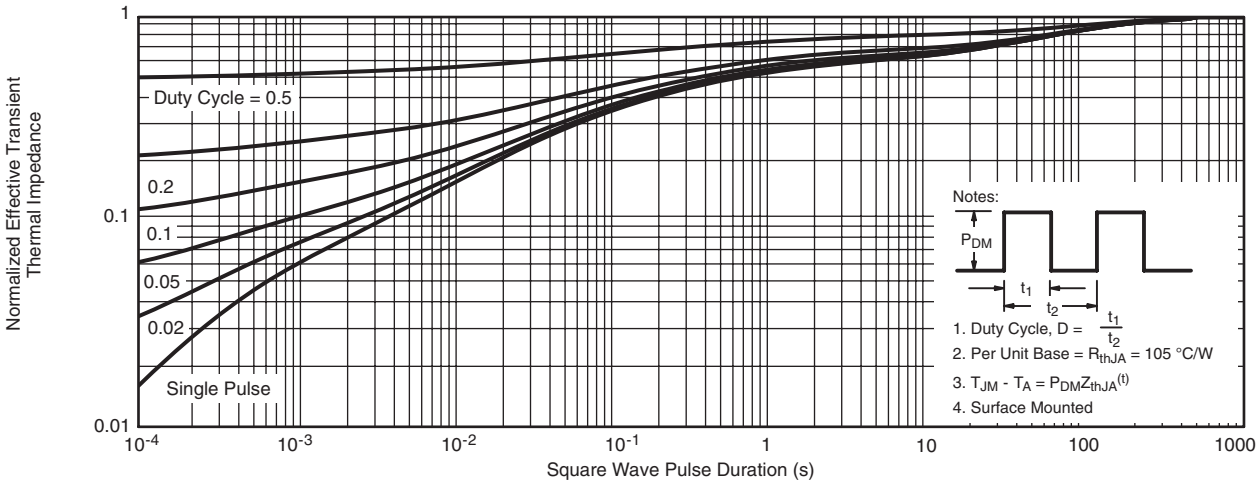


Capacitance

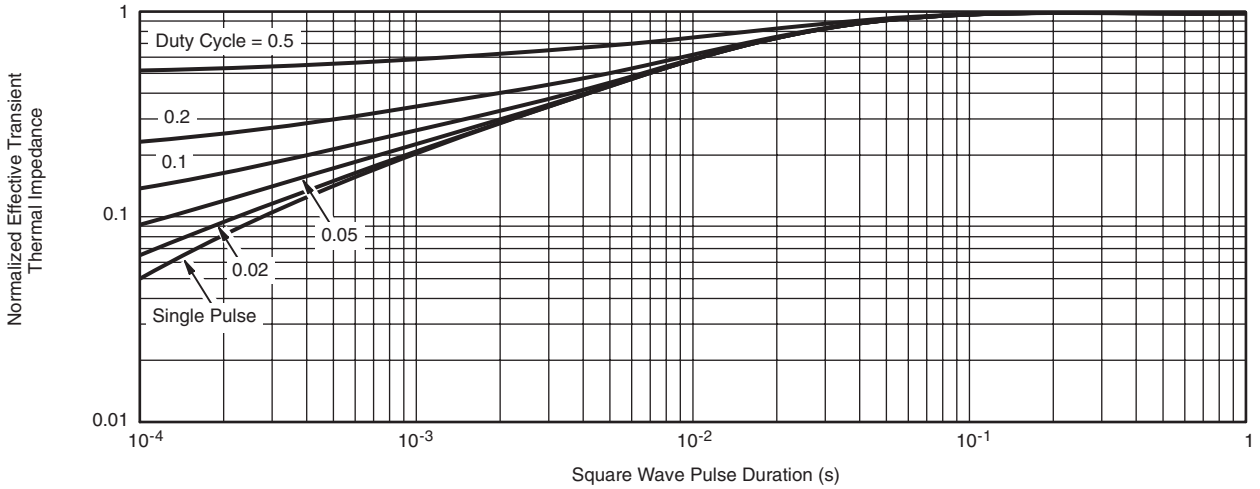


Single Pulse Power, Junction-to-Ambient

SCHOTTKY TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted



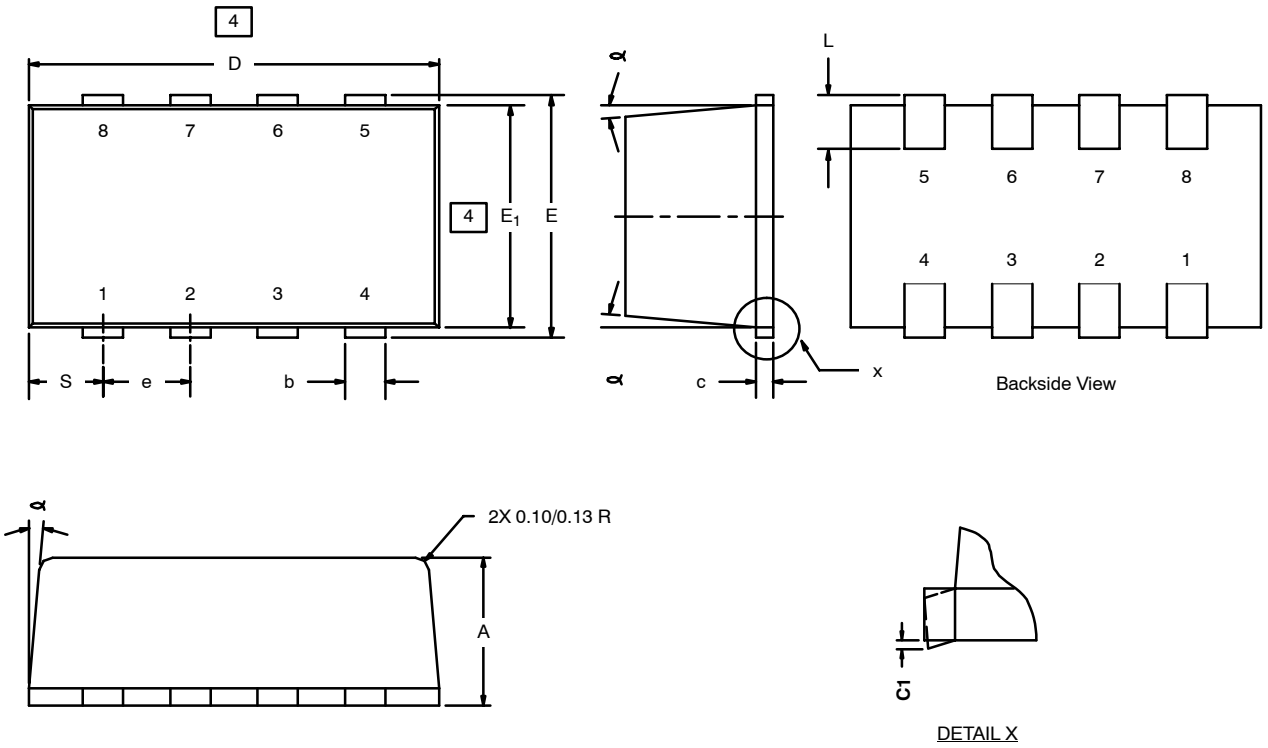
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?68920.

1206-8 ChipFET®



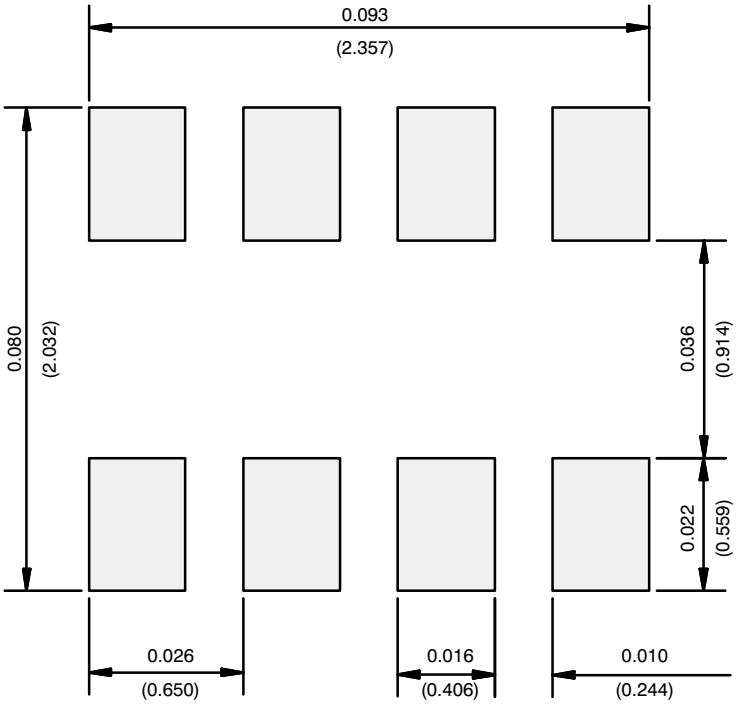
NOTES:

1. All dimensions are in millimeaters.
2. Mold gate burrs shall not exceed 0.13 mm per side.
3. Leadframe to molded body offset is horizontal and vertical shall not exceed 0.08 mm.
4. Dimensions exclusive of mold gate burrs.
5. No mold flash allowed on the top and bottom lead surface.

Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	1.00	–	1.10	0.039	–	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.1	0.15	0.20	0.004	0.006	0.008
c1	0	–	0.038	0	–	0.0015
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.825	1.90	1.975	0.072	0.075	0.078
E_1	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.0256 BSC		
L	0.28	–	0.42	0.011	–	0.017
S	0.55 BSC			0.022 BSC		
α	5°Nom			5°Nom		

ECN: C-03528—Rev. F, 19-Jan-04
DWG: 5547

RECOMMENDED MINIMUM PADS FOR 1206-8 ChipFET®



Recommended Minimum Pads
Dimensions in Inches/(mm)

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