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Si473x-B20

1. Product Overview

The Si473x receivers are the industry's first fully-integrated multiband radio receiver ICs from antenna input to audio output. They require minimal external components with no factory alignment. The Si473x receivers reduce the receiver footprint by >90% versus traditional AM/FM solutions. The Si473x also offer best-in-class performance with the most features. The high integration and complete system production test simplifies design-in, increases system quality, and improves manufacturability.

The Si473x receivers include advanced seek algorithms, adjustable soft mute, auto-calibrated digital tuning, and FM stereo processing. In addition, the Si473x ICs provide a programmable reference clock and an I2C-compatible 2-wire control interface.

The Si4731/35/37/39 incorporates a digital processor for the European Radio Data System (RDS) and the North American Radio Broadcast Data System (RBDS), including all required symbol decoding, block synchronization, error detection, and error correction functions. Using these features, the Si4731/35/37/39 enables broadcast data such as station identification and song name to be displayed to the end user.

2. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.7	—	5.5	V
Interface Supply Voltage	V_{IO}		1.5	—	3.6	V
Power Supply Powerup Rise Time	V_{DDRISE}		10	—	—	μ s
Interface Power Supply Powerup Rise Time	V_{IORISE}		10	—	—	μ s
Ambient Temperature	T_A		-20	25	85	°C
Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at $V_{DD} = 3.3$ V and 25 °C unless otherwise stated. Parameters are tested in production unless otherwise stated.						

Table 2. Absolute Maximum Ratings^{1,2}

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.5 to 5.8	V
Interface Supply Voltage	V_{IO}	–0.5 to 3.9	V
Input Current ³	I_{IN}	10	mA
Input Voltage ³	V_{IN}	–0.3 to ($V_{IO} + 0.3$)	V
Operating Temperature	T_{OP}	–40 to 95	°C
Storage Temperature	T_{STG}	–55 to 150	°C
RF Input Level ⁴		0.4	V_{PK}

Notes:

1. Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. The Si473x devices are high-performance RF integrated circuits with certain pins having an ESD rating of < 2 kV HBM. Handling and assembly of these devices should only be done at ESD-protected workstations.
3. For input pins SCLK, SEN, SDIO, RST, RCLK, DCLK, DFS, GPO1, GPO2, and GPO3.
4. At RF input pins, FMI and AMI.

Si473x-B20

Table 3. DC Characteristics

($V_{DD} = 2.7$ to 5.5 V, $V_{IO} = 1.5$ to 3.6 V, $T_A = -20$ to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
FM Mode						
Supply Current	I_{FM}		—	19.2	22	mA
Supply Current ¹	I_{FM}	Low SNR level	—	19.8	23	mA
RDS Supply Current ²	I_{FM}		—	19.9	23	mA
WB Mode (Si4736/37/38/39 only)						
Supply Current	I_{FM}		—	19.2	22	mA
Supply Current ¹	I_{FM}	Low SNR level	—	19.8	23	mA
AM Mode (Si4730/31/34/35/36/37 only)						
Supply Current	I_{AM}		—	17.3	20.5	mA
Supplies and Interface						
Interface Supply Current	I_{IO}		—	320	600	μA
V_{DD} Powerdown Current	I_{DDPD}		—	10	20	μA
V_{IO} Powerdown Current	I_{IOPD}	SCLK, RCLK inactive	—	1	10	μA
High Level Input Voltage ³	V_{IH}		$0.7 \times V_{IO}$	—	$V_{IO} + 0.3$	V
Low Level Input Voltage ³	V_{IL}		−0.3	—	$0.3 \times V_{IO}$	V
High Level Input Current ³	I_{IH}	$V_{IN} = V_{IO} = 3.6$ V	−10	—	10	μA
Low Level Input Current ³	I_{IL}	$V_{IN} = 0$ V, $V_{IO} = 3.6$ V	−10	—	10	μA
High Level Output Voltage ⁴	V_{OH}	$I_{OUT} = 500$ μA	$0.8 \times V_{IO}$	—	—	V
Low Level Output Voltage ⁴	V_{OL}	$I_{OUT} = -500$ μA	—	—	$0.2 \times V_{IO}$	V
Notes: 1. LNA is automatically switched to higher current mode for optimum sensitivity in weak signal conditions. 2. Specifications are guaranteed by characterization. 3. For input pins SCLK, SEN, SDIO, RST, RCLK, DCLK, and DFS. 4. For output pins SDIO, DOUT, GPO1, GPO2, and GPO3.						

Table 4. Reset Timing Characteristics^{1,2}(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = -20 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{\text{RST}}$ Pulse Width and GPO1, GPO2/ $\overline{\text{INT}}$ Setup to $\overline{\text{RST}}\uparrow^3$	t_{SRST}	100	—	—	μs
GPO1, GPO2/ $\overline{\text{INT}}$ Hold from $\overline{\text{RST}}\uparrow$	t_{HRST}	30	—	—	ns

Important Notes:

1. When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of $\overline{\text{RST}}$.
2. When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{\text{RST}}$, and stays high until after the first start condition.
3. If GPO1 and GPO2 are actively driven by the user, then minimum t_{SRST} is only 30 ns. If GPO1 or GPO2 is hi-Z, then minimum t_{SRST} is 100 μs to provide time for on-chip 1 M Ω devices (active while $\overline{\text{RST}}$ is low) to pull GPO1 high and GPO2 low.

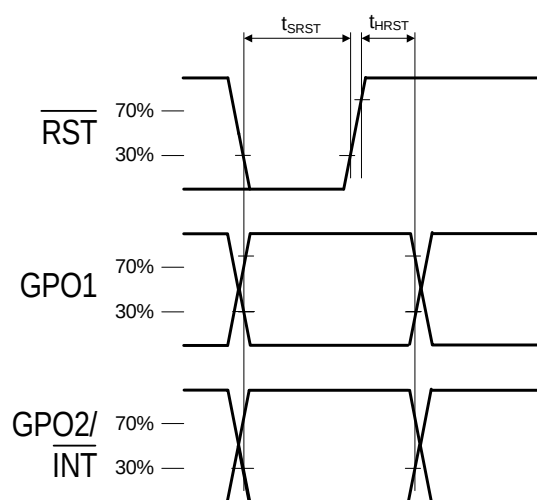
**Figure 1. Reset Timing Parameters for Busmode Select**

Table 5. 2-Wire Control Interface Characteristics^{1,2,3}

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = -20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f _{SCL}		0	—	400	kHz
SCLK Low Time	t _{LOW}		1.3	—	—	μs
SCLK High Time	t _{HIGH}		0.6	—	—	μs
SCLK Input to SDIO ↓ Setup (START)	t _{SU:STA}		0.6	—	—	μs
SCLK Input to SDIO ↓ Hold (START)	t _{HD:STA}		0.6	—	—	μs
SDIO Input to SCLK ↑ Setup	t _{SU:DAT}		100	—	—	ns
SDIO Input to SCLK ↓ Hold ^{4,5}	t _{HD:DAT}		0	—	900	ns
SCLK input to SDIO ↑ Setup (STOP)	t _{SU:STO}		0.6	—	—	μs
STOP to START Time	t _{BUF}		1.3	—	—	μs
SDIO Output Fall Time	t _{f:OUT}		$20 + 0.1 \frac{C_b}{1\text{pF}}$	—	250	ns
SDIO Input, SCLK Rise/Fall Time	t _{f:IN} t _{r:IN}		$20 + 0.1 \frac{C_b}{1\text{pF}}$	—	300	ns
SCLK, SDIO Capacitive Loading	C _b		—	—	50	pF
Input Filter Pulse Suppression	t _{SP}		—	—	50	ns

Notes:

1. When V_{IO} = 0 V, SCLK and SDIO are low impedance.
2. When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of RST.
3. When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of RST, and stays high until after the first start condition.
4. The Si473x delays SDIO by a minimum of 300 ns from the V_{IH} threshold of SCLK to comply with the minimum t_{HD:DAT} specification.
5. The maximum t_{HD:DAT} has only to be met when f_{SCL} = 400 kHz. At frequencies below 400 KHz, t_{HD:DAT} may be violated as long as all other timing parameters are met.

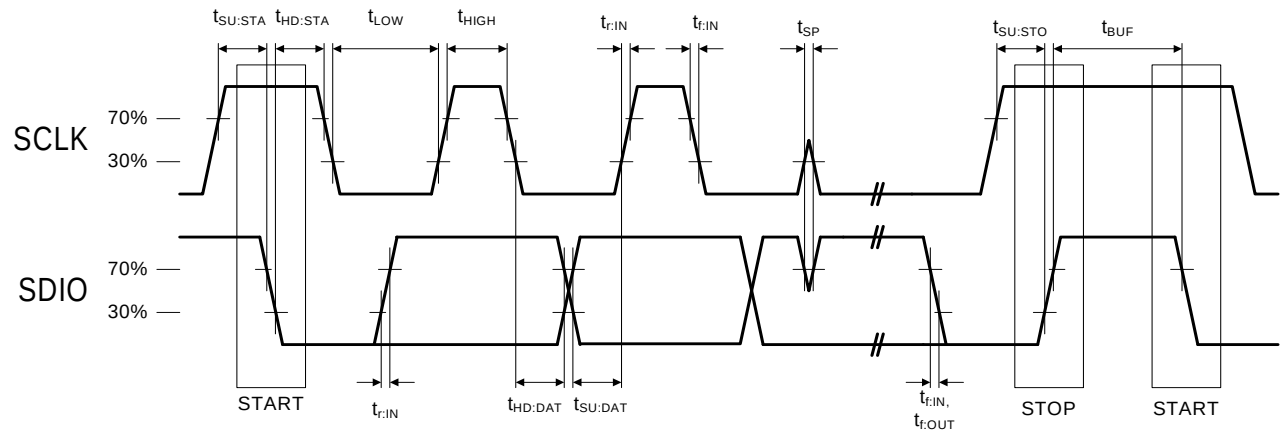


Figure 2. 2-Wire Control Interface Read and Write Timing Parameters

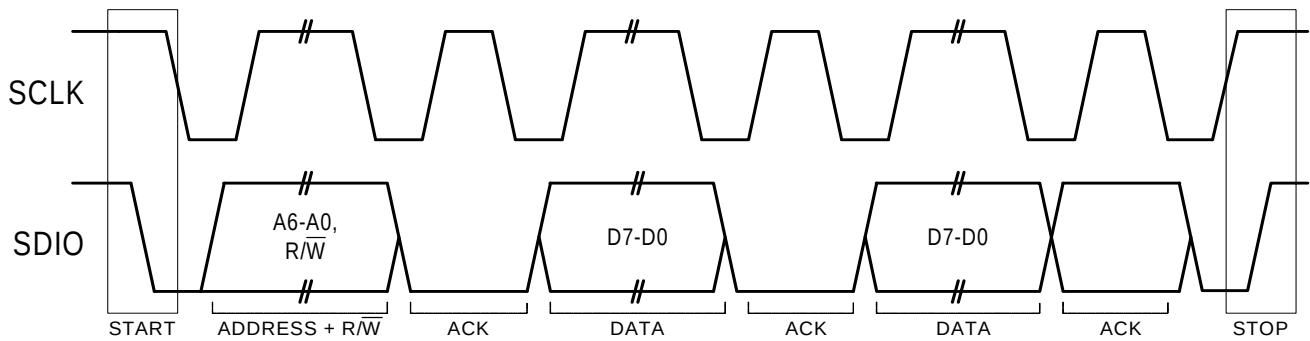


Figure 3. 2-Wire Control Interface Read and Write Timing Diagram

Table 6. Digital Audio Interface Characteristics

($V_{DD} = 2.7$ to 5.5 V, $V_{IO} = 1.5$ to 3.6 V, $T_A = -20$ to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DCLK Cycle Time	t_{DCT}		26	—	1000	ns
DCLK Pulse Width High	t_{DCH}		10	—	—	ns
DCLK Pulse Width Low	t_{DCL}		10	—	—	ns
DFS Set-up Time to DCLK Rising Edge	$t_{SU:DFS}$		5	—	—	ns
DFS Hold Time from DCLK Rising Edge	$t_{HD:DFS}$		5	—	—	ns
DOUT Propagation Delay from DCLK Falling Edge	$t_{PD:DOUT}$		0	—	12	ns

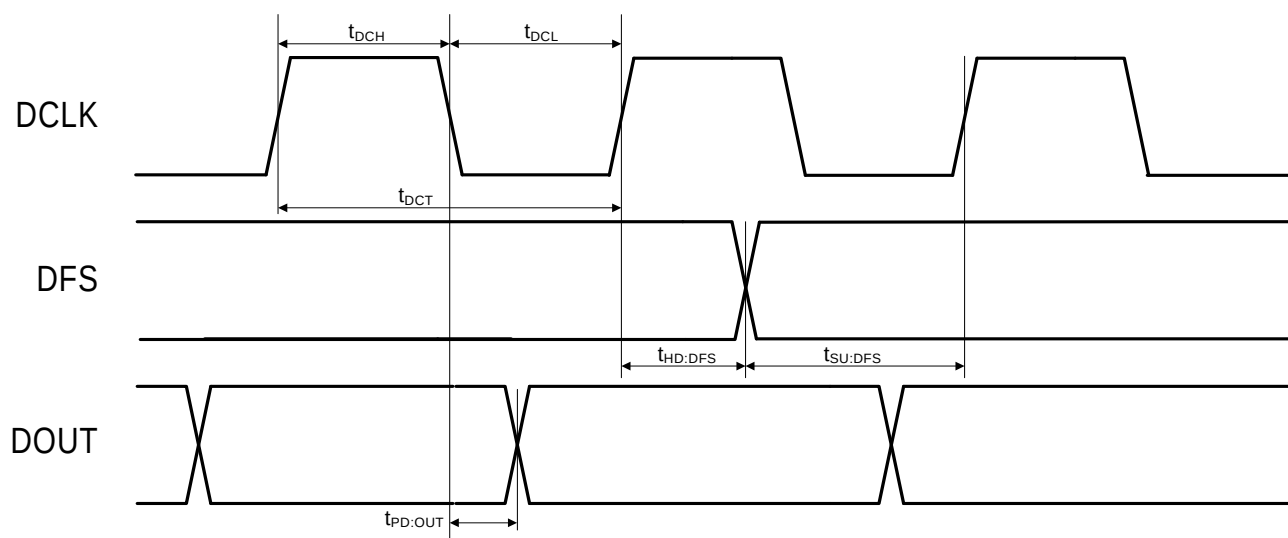


Figure 4. Digital Audio Interface Timing Parameters, I²S Mode

Table 7. FM Receiver Characteristics^{1,2}(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = -20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency	f _{RF}		76	—	108	MHz
Sensitivity with Headphone Network ^{3,4,5}		(S+N)/N = 26 dB	—	2.2	3.5	μV EMF
Sensitivity with 50 Ω Network ^{3,4,5,6}		(S+N)/N = 26 dB	—	1.1	—	μV EMF
RDS Sensitivity ⁶		Δf = 2 kHz, RDS BLER < 5%	—	15	—	μV EMF
LNA Input Resistance ^{6,7}			3	4	5	kΩ
LNA Input Capacitance ^{6,7}			4	5	6	pF
Input IP3 ^{6,8}			100	105	—	dBμV EMF
AM Suppression ^{3,4,6,7}		m = 0.3	40	50	—	dB
Adjacent Channel Selectivity		±200 kHz	35	50	—	dB
Alternate Channel Selectivity		±400 kHz	60	70	—	dB
Spurious Response Rejection ⁶		In-band	35	—	—	dB
Audio Output Voltage ^{3,4,7}			72	80	90	mV _{RMS}
Audio Output L/R Imbalance ^{3,7,9}			—	—	1	dB
Audio Frequency Response Low ⁶		-3 dB	—	—	30	Hz
Audio Frequency Response High ⁶		-3 dB	15	—	—	kHz
Audio Stereo Separation ^{7,9}			25	—	—	dB
Audio Mono S/N ^{3,4,5,7,10}			55	63	—	dB
Audio Stereo S/N ^{4,5,7,10,11}			—	58	—	dB
Audio THD ^{3,7,9}			—	0.1	0.5	%
De-emphasis Time Constant ⁶		FM_DEEMPHASIS = 2	70	75	80	μs
		FM_DEEMPHASIS = 1	45	50	54	μs
Audio Output Load Resistance ^{6,10}	R _L	Single-ended	10	—	—	kΩ
Audio Output Load Capacitance ^{6,10}	C _L	Single-ended	—	—	50	pF

Notes:

1. Additional testing information is available in "AN388: Si470x/1x/2x/3x/4x Evaluation Test Board Procedure." Volume = maximum for all tests. Tested at RF = 98.1 MHz.
2. To ensure proper operation and receiver performance, follow the guidelines in "AN383: Si47xx Antenna, Schematic, Layout and Design Guidelines." Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. F_{MOD} = 1 kHz, 75 μs de-emphasis, MONO = enabled, and L = R unless noted otherwise.
4. Δf = 22.5 kHz.
5. B_{AF} = 300 Hz to 15 kHz, A-weighted.
6. Guaranteed by characterization.
7. V_{EMF} = 1 mV.
8. |f₂ - f₁| > 2 MHz, f₀ = 2 x f₁ - f₂. AGC is disabled.
9. Δf = 75 kHz.
10. At L_{OUT} and R_{OUT} pins.
11. Analog audio output mode.
12. At temperature (25°C).

Table 7. FM Receiver Characteristics^{1,2} (Continued)

($V_{DD} = 2.7$ to 5.5 V, $V_{IO} = 1.5$ to 3.6 V, $T_A = -20$ to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Seek/Tune Time ⁶		RCLK tolerance = 100 ppm	—	—	80	ms/channel
Powerup Time ⁶		From powerdown	—	—	110	ms
RSSI Offset ¹²		Input levels of 8 and 60 dBμV at RF Input	−3	—	3	dB

Notes:

1. Additional testing information is available in “AN388: Si470x/1x/2x/3x/4x Evaluation Test Board Procedure.” Volume = maximum for all tests. Tested at RF = 98.1 MHz.
2. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Si47xx Antenna, Schematic, Layout and Design Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. $F_{MOD} = 1$ kHz, 75 μs de-emphasis, MONO = enabled, and L = R unless noted otherwise.
4. $\Delta f = 22.5$ kHz.
5. $B_{AF} = 300$ Hz to 15 kHz, A-weighted.
6. Guaranteed by characterization.
7. $V_{EMF} = 1$ mV.
8. $|f_2 - f_1| > 2$ MHz, $f_0 = 2 \times f_1 - f_2$. AGC is disabled.
9. $\Delta f = 75$ kHz.
10. At L_{OUT} and R_{OUT} pins.
11. Analog audio output mode.
12. At temperature (25°C).

Table 8. AM/SW/LW Receiver Characteristics¹(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, TA = -20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency	f _{RF}	Long Wave (LW)	153	—	279	kHz
		Medium Wave (AM)	520	—	1710	kHz
		Short Wave (SW)	2.3	—	21.85	MHz
Sensitivity ^{2,3,4,5, 6}		(S+N)/N = 26 dB	—	25	35	μV EMF
Large Signal Voltage Handling ^{5,7}		THD < 8%	—	300	—	mV _{RMS}
Power Supply Rejection Ratio		ΔV _{DD} = 100 mV _{RMS} , 100 Hz	—	40	—	dB
Audio Output Voltage ^{2,8}			54	60	67	mV _{RMS}
Audio S/N ^{2,3,4,6,8}			50	56	—	dB
Audio THD ^{2,4,8}			—	0.1	0.5	%
Antenna Inductance		Long Wave (LW)	—	2800	—	μH
		Medium Wave (AM)	180	—	450	
Powerup Time		From powerdown	—	—	110	ms

Notes:

1. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Si47xx Antenna, Schematic, Layout and Design Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
2. F_{MOD} = 1 kHz, 30% modulation, A-weighted, 2 kHz channel filter.
3. B_{AF} = 300 Hz to 15 kHz, A-weighted.
4. f_{RF} = 1000 kHz, Δf = 10 kHz.
5. Guaranteed by characterization.
6. Analog audio output mode.
7. See “AN388: Si470X/1X/2X/3X/4X Evaluation Board Test Procedure” for evaluation method.
8. V_{IN} = 5 mV_{rms}.
9. Stray capacitance on antenna and board must be < 10 pF to achieve full tuning range at higher inductance levels.

Table 9. WB Receiver Characteristics¹

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = 25 °C)

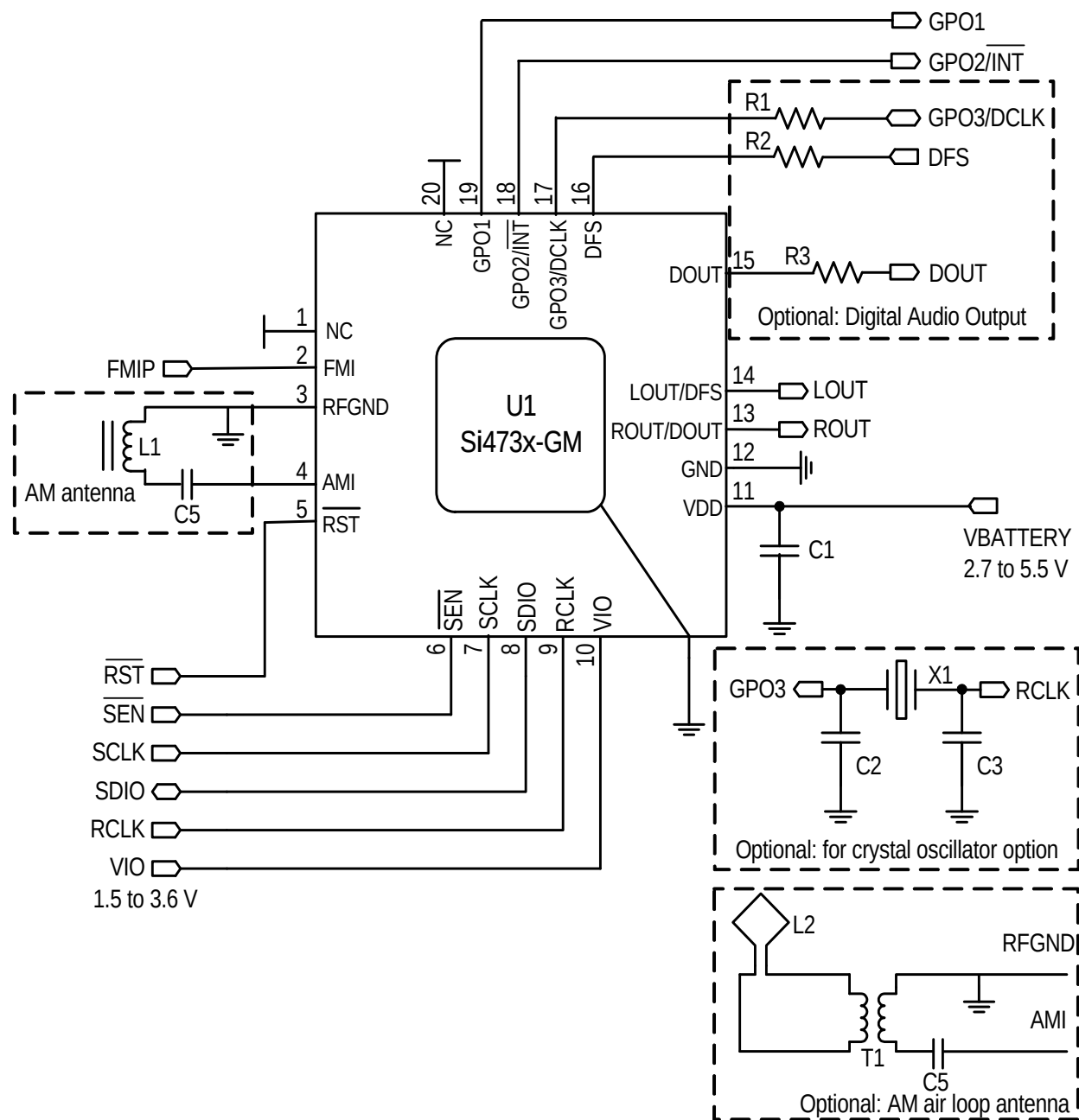
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency	f _R		162.4	—	162.55	MHz
Sensitivity ^{2,3}		SINAD = 12 dB	—	0.9	—	μV EMF
Adjacent Channel Selectivity		±25 kHz	—	52	—	dB
Audio S/N ^{2,3,4,5}		Mono	—	45	—	dB
Audio Frequency Response Low ⁶		–3 dB	—	—	300	Hz
Audio Frequency Response High ⁶		–3 dB	3	—	—	kHz
Notes: 1. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Si47xx Antenna, Schematic, Layout and Design Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers. 2. F_{MOD} = 1 kHz. 3. Δf = 3 kHz. 4. V_{EMF} = 1 mV. 5. A-weighted. 6. Guaranteed by characterization						

Table 10. Reference Clock and Crystal Characteristics

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reference Clock						
RCLK Supported Frequencies ¹			31.130	32.768	40,000	kHz
RCLK Frequency Tolerance ²			–100	—	100	ppm
REFCLK_PRESCALE			1	—	4095	
REFCLK			31.130	32.768	34.406	kHz
Crystal Oscillator						
Crystal Oscillator Frequency			—	32.768	—	kHz
Crystal Frequency Tolerance ²			–50	—	50	ppm
Board Capacitance			—	—	3.5	pF
Notes: 1. The Si473x divides the RCLK input by REFCLK_PRESCALE to obtain REFCLK. There are some RCLK frequencies between 31.130 kHz and 40 MHz that are not supported. See “AN332: Si47xx Programming Guide,” Table 6 for more details. 2. A frequency tolerance of ±50 ppm is required for FM seek/tune using 50 kHz channel spacing, SW seek/tune, and WB tune.						

3. Typical AM/FM Application Schematic



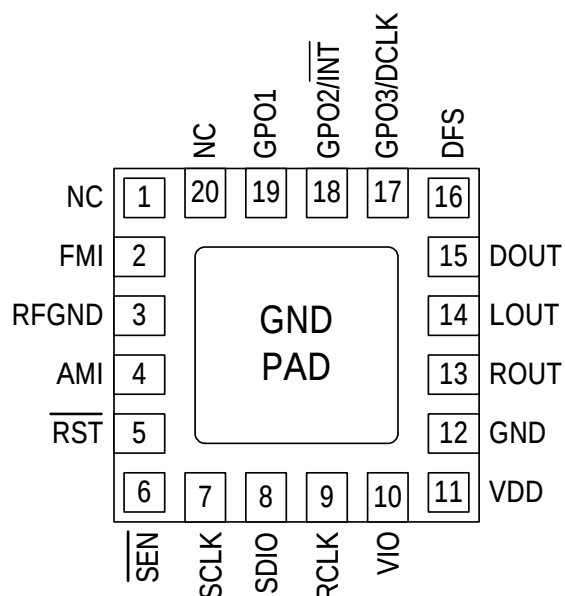
Notes:

1. Place C1 close to V_{DD} pin.
2. All grounds connect directly to GND plane on PCB.
3. Pins 1 and 20 are no connects, leave floating.
4. To ensure proper operation and receiver performance, follow the guidelines in "AN383: Si47xx Antenna, Schematic, Layout and Design Guidelines." Silicon Laboratories will evaluate schematics and layouts for qualified customers.
5. Pin 2 connects to the FM antenna interface and pin 4 connects to the AM antenna interface.
6. RFGND should be locally isolated from GND.
7. Place Si473x as close as possible to antenna jack and keep the FMI and AMI traces as short as possible.

4. Bill of Materials

Component(s)	Value/Description	Supplier
C1	Supply bypass capacitor, 22 nF, $\pm 20\%$, Z5U/X7R	Murata
C5	Coupling capacitor, 0.47 μ F, $\pm 20\%$, Z5U/X7R	Murata
L1	Ferrite loop stick, 180–450 μ H	Jiaxin
U1	Si473x AM/FM Radio Tuner	Silicon Laboratories
Optional Components		
T1	Transformer, 1–5 turns ratio	Jiaxin, UMEC
L2	Air loop antenna, 10–20 μ H	Various
C2, C3	Crystal load capacitors, 22 pF, $\pm 5\%$, COG (Optional: for crystal oscillator option)	Venkel
X1	32.768 kHz crystal (Optional: for crystal oscillator option)	Epson
R1	Resistor, 2 k Ω (Optional: for digital audio)	Venkel
R2	Resistor, 2 k Ω (Optional: for digital audio)	Venkel
R3	Resistor, 600 Ω (Optional: for digital audio)	Venkel

5. Pin Descriptions: Si473x-GM



Pin Number(s)	Name	Description
1, 20	NC	No connect. Leave floating.
2	FMI	FM/WB/SW RF inputs. FMI should be connected to the antenna trace.
3	RFGND	RF ground. Connect to ground plane on PCB.
4	AMI	AM/SW/LW RF input. AMI should be connected to the AM antenna.
5	$\overline{\text{RST}}$	Device reset (active low) input.
6	$\overline{\text{SEN}}$	Serial enable input (active low).
7	SCLK	Serial clock input.
8	SDIO	Serial data input/output.
9	RCLK	External reference oscillator input.
10	V _{IO}	I/O supply voltage.
11	V _{DD}	Supply voltage. May be connected directly to battery.
12, GND PAD	GND	Ground. Connect to ground plane on PCB.
13	ROUT	Right audio line output in analog output mode.
14	LOUT	Left audio line output in analog output mode.
15	DOUT	Digital output data in digital output mode.
16	DFS	Digital frame synchronization input in digital output mode.
17	GPO3/DCLK	General purpose output, crystal oscillator, or digital bit synchronous clock input in digital output mode.
18	GPO2/ $\overline{\text{INT}}$	General purpose output or interrupt pin.
19	GPO1	General purpose output.

6. Ordering Guide

Part Number*	Description	Package Type	Operating Temperature
Si4730-B20-GM	AM/FM Broadcast Radio Receiver	QFN Pb-free	–20 to 85 °C
Si4731-B20-GM	AM/FM Broadcast Radio Receiver with RDS/RBDS	QFN Pb-free	–20 to 85 °C
Si4734-B20-GM	AM/FM/SW/LW Broadcast Radio Receiver	QFN Pb-free	–20 to 85 °C
Si4735-B20-GM	AM/FM/SW/LW Broadcast Radio Receiver with RDS/RBDS	QFN Pb-free	–20 to 85 °C
Si4736-B20-GM	AM/FM/WB Broadcast Radio Receiver	QFN Pb-free	–20 to 85 °C
Si4737-B20-GM	AM/FM/WB Broadcast Radio Receiver with RDS/RBDS	QFN Pb-free	–20 to 85 °C
Si4738-B20-GM	FM/WB Broadcast Radio Receiver	QFN Pb-free	–20 to 85 °C
Si4739-B20-GM	FM/WB Broadcast Radio Receiver with RDS/RBDS	QFN Pb-free	–20 to 85 °C
*Note: Add an “(R)” at the end of the device part number to denote tape and reel option; 2500 quantity per reel.			

7. Package Outline: Si473x QFN

Figure 5 illustrates the package details for the Si473x. Table 11 lists the values for the dimensions shown in the illustration.

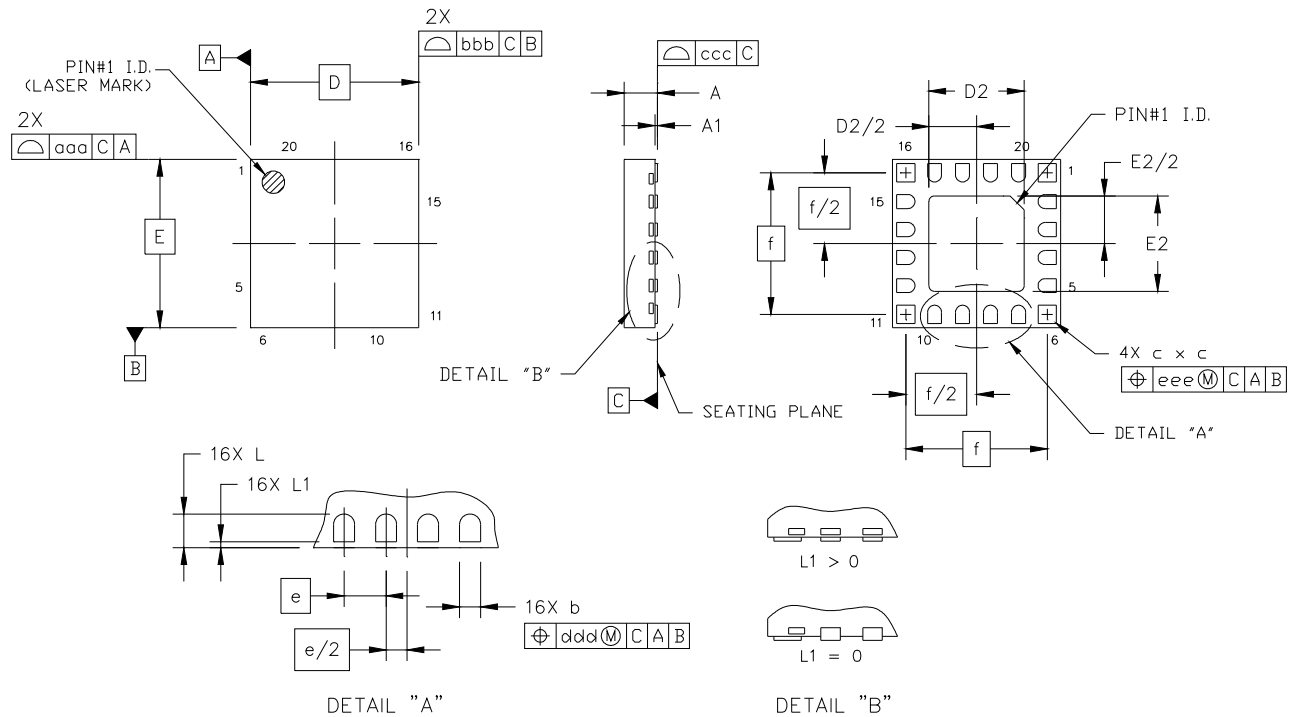


Figure 5. 20-Pin Quad Flat No-Lead (QFN)

Table 11. Package Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
c	0.27	0.32	0.37
D	3.00 BSC		
D2	1.65	1.70	1.75
e	0.50 BSC		
E	3.00 BSC		
E2	1.65	1.70	1.75

Symbol	Millimeters		
	Min	Nom	Max
f	2.53 BSC		
L	0.35	0.40	0.45
L1	0.00	—	0.10
aaa	—	—	0.05
bbb	—	—	0.05
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10

Notes:

1. All dimensions are shown in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.

8. PCB Land Pattern: Si473x QFN

Figure 6 illustrates the PCB land pattern details for the Si473x family. Table 12 lists the values for the dimensions shown in the illustration.

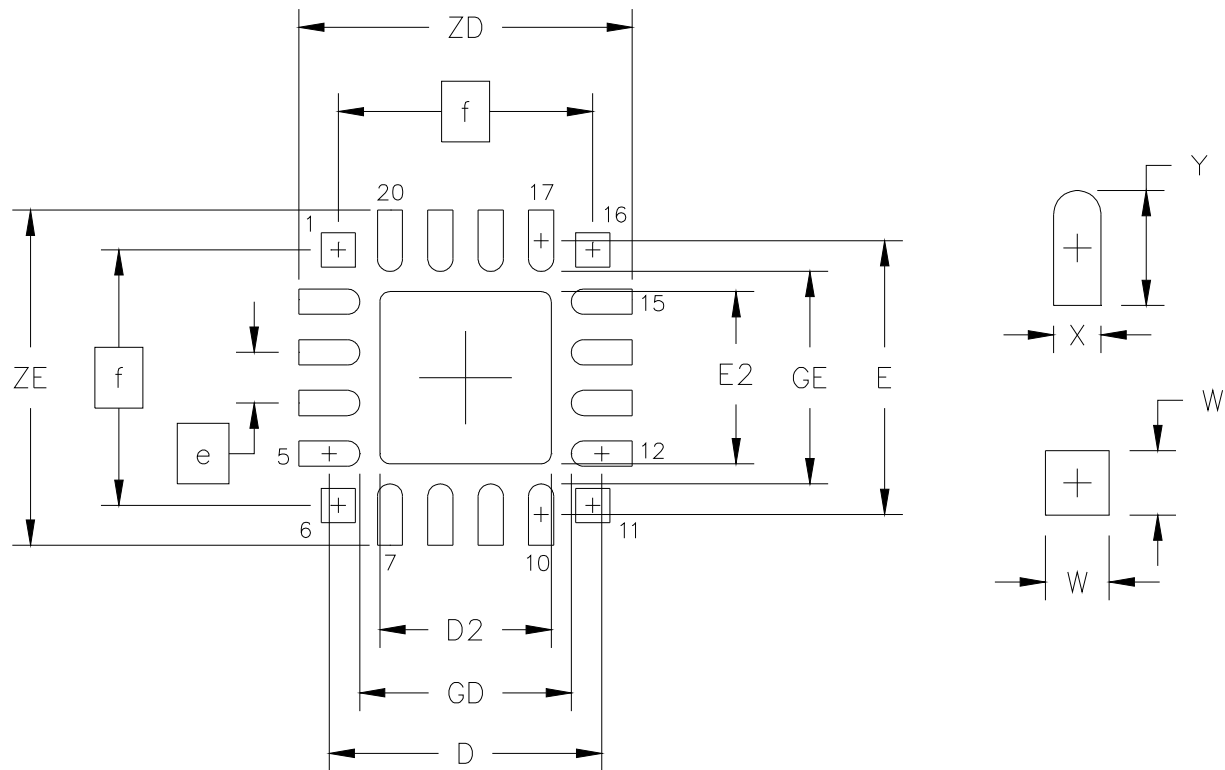


Figure 6. PCB Land Pattern

Table 12. PCB Land Pattern Dimensions

Symbol	Millimeters	
	Min	Max
D	2.71 REF	
D2	1.60	1.80
e	0.50 BSC	
E	2.71 REF	
E2	1.60	1.80
f	2.53 BSC	
GD	2.10	—

Symbol	Millimeters	
	Min	Max
GE	2.10	—
W	—	0.34
X	—	0.28
Y	0.61 REF	
ZE	—	3.31
ZD	—	3.31

Notes: General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Notes: Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μ m minimum, all the way around the pad.

Notes: Stencil Design

1. A stainless steel, laser-cut, and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 1.45 x 1.45 mm square aperture should be used for the center pad. This provides approximately 70% solder paste coverage on the pad, which is optimum to assure correct component stand-off.

Notes: Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

9. Additional Reference Resources

Contact your local sales representatives for more information or to obtain copies of the following references:

- EN55020 Compliance Test Certificate
- AN332: Si47xx Programming Guide
- AN383: Si47xx Antenna, Schematic, Layout, and Design Layout Guidelines
- AN388: Si470x/1x/2x/3x/4x Evaluation Board Test Procedure

NOTES:

CONTACT INFORMATION

Silicon Laboratories Inc.

400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032
Email: FMinfo@silabs.com
Internet: www.silabs.com

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