

DAC-Controlled Boost/Inverter LCD Bias Supply with Internal Switch

ABSOLUTE MAXIMUM RATINGS

Voltage

V _{CC} , ISET, POK, POL, $\overline{\text{SHDN}}$, UP, DN, V _{DD} to GND	-0.3V to +6V
FB, REF, DACOUT to GND	-0.3V to (V _{CC} + 0.3V)
PGND to GND	-0.3V to +0.3V
LX, LCDON to GND	-0.3V to +30V

Current

LX (sinking)	600mA
LCDON (sinking)	10mA

Continuous Power Dissipation (T_A = +70°C)

QSOP (derate 8.30mW/°C above +70°C)667mW

Operating Temperature Ranges

MAX686C/D0°C to +70°C

MAX686EEE-40°C to +85°C

Storage Temperature Range-65°C to +160°C

Lead Temperature (soldering, 10sec)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = V_{DD} = V_{IN} = +5V, C_{REF} = 0.1μF, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (Note 1)	V _{CC} , V _{DD}		2.7		5.5	V
Input Voltage	V _{IN}	Voltage applied to L1	0.8		V _{OUT}	V
Supply Current	I _{CC} + I _{DD}	POL = GND, V _{FB} = 1.3V, I _{DACOUT} = 0mA		65	125	μA
Shutdown Current	I _{SHDN}	$\overline{\text{SHDN}}$ = GND		1.3	4	μA
V _{CC} Undervoltage Lockout	V _{LOCK}	Rising or falling	2.10	2.5	2.65	V
V _{CC} Undervoltage Lockout Hysteresis				100		mV
V _{CC} DAC Reset Threshold	V _{RESET}		0.5	1.5	2.1	V
Line Regulation		Boost configuration, V _{OUT} = 27.5V, I _{LOAD} = 5mA, V _{CC} = V _{DD} = 2.7V to 5.5V		0.1		%/V
Load Regulation		Boost configuration, V _{OUT} = 27.5V, I _{LOAD} = 0mA to 5mA		0.01		%/mA
LX						
LX Voltage Range	V _{LX}				28	V
LX Switch Current Limit	I _{LX}	ISET = V _{CC}	0.42	0.50	0.58	A
		ISET = GND	0.21	0.25	0.29	
LX On-Resistance	R _{LX}	V _{CC} = V _{DD} = 5V, I _{LX} = 100mA		0.6	1.2	Ω
		V _{CC} = V _{DD} = 3.3V, I _{LX} = 100mA		0.8	1.6	
LX Leakage Current	I _{LXLEAK}	V _{LX} = 28V			1.5	μA
Maximum LX On-Time	t _{ON}		8	10	12	μs
Minimum LX Off-Time	t _{OFF}	POL = GND, V _{FB} > 1.2V	0.8	1	1.2	μs
		POL = V _{CC} , V _{FB} < 0.15V	2.8	3.5	4.2	
		POL = GND, V _{FB} < 0.8V	4	5	6	
		POL = V _{CC} , V _{FB} > 0.4V	4	5	6	

DAC-Controlled Boost/Inverter LCD Bias Supply with Internal Switch

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = V_{DD} = V_{IN} = +5V$, $C_{REF} = 0.1\mu F$, $T_A = 0^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE AND FB INPUT						
REF Output Voltage	V_{REF}	$V_{CC} = V_{DD} = 2.7V$ to $5.5V$, no load	1.225	1.250	1.275	V
REF Load Regulation		$I_{REF} = 0\mu A$ to $25\mu A$, $C_{REF} = 0.1\mu F$		1	10	mV
		$I_{REF} = 0\mu A$ to $50\mu A$, $C_{REF} = 0.47\mu F$		1.5		
FB Set Point	V_{FB}	POL = GND	1.225	1.250	1.275	V
		POL = V_{CC}	-15	0	15	mV
FB Input Bias Current	I_{FB}				± 50	nA
POWER OK COMPARATOR, LCDON OUTPUT						
POK Threshold	V_{POK}	V_{POK} rising	1.100	1.125	1.150	V
POK Input Current	I_{POK}				± 50	nA
POK Hysteresis				12		mV
LCDON Sink Current	I_{LCDON}	$V_{LCDON} = 0.4V$, $V_{POK} = 1.25V$	2	6		mA
LCDON Leakage Current		$V_{LCDON} = 28V$, $V_{POK} = GND$		0.02	1	μA
DAC OUTPUT (Notes 2, 3)						
Full-Scale Output Voltage	V_{FS}	$-50\mu A < I_{DACOUT} < 0\mu A$	$V_{REF} - 0.015$	V_{REF}	$V_{REF} + 0.015$	V
Zero-Scale Output Voltage	V_{ZS}	$0\mu A < I_{DACOUT} < 20\mu A$	0		15	mV
Resolution			6			bits
Mid-Scale Accuracy	MSA	Mid-scale = $V_{REF} \times 32/63$	-2		2	%
Differential Nonlinearity	DNL	Guaranteed monotonic	-1		1	LSB
Output Resistance in Shutdown	R_{DACOUT}			1.5		$k\Omega$
LOGIC INPUTS: POL, ISET, UP, DN, SHDN						
Input Low Level	V_{IL}	$2.7V < V_{CC} = V_{DD} < 5.5V$			0.7	V
Input High Level	V_{IH}	$2.7V < V_{CC} = V_{DD} < 5.5V$	2.4			V
Input Bias Current	I_{BIAS}				± 1	μA
Pulse Width High	t_{PWH}	UP, DN, $T_A = +25^\circ C$	1			μs
Pulse Width Low	t_{PWL}	UP, DN, $T_A = +25^\circ C$	1			μs
Pulse Separation	t_{PWS}	UP, DN, $T_A = +25^\circ C$	1			μs

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ELECTRICAL CHARACTERISTICS

($V_{CC} = V_{DD} = V_{IN} = +5V$, $C_{REF} = 0.1\mu F$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (Note 1)	V _{CC} , V _{DD}		2.7		5.5	V
Input Voltage	V _{IN}	Voltage applied to L1	0.8		V _{OUT}	V
Supply Current	I _{CC} + I _{DD}	POL = GND, V _{FB} = 1.3V, I _{DACOUT} = 0mA			125	μA
Shutdown Current	I _{SHDN}	SHDN = GND			4	μA
V _{CC} Undervoltage Lockout	V _{LOCK}	Rising or falling	2.10		2.65	V
LX						
LX Voltage Range	V _{LX}				28	V
LX Switch Current Limit	I _{LX}	ISET = V _{CC}	0.4		0.6	A
		ISET = GND	0.2		0.3	
LX On-Resistance	R _{LX}	V _{CC} = V _{DD} = 5V, I _{LX} = 100mA			1.2	Ω
		V _{CC} = V _{DD} = 3.3V, I _{LX} = 100mA			1.6	
LX Leakage Current	I _{LXLEAK}	V _{LX} = 28V			1.5	μA
Maximum LX On-Time	t _{ON}		7.5		12.5	μs
Minimum LX Off-Time	t _{OFF}	POL = GND, V _{FB} > 1.2V	0.7		1.3	μs
		POL = V _{CC} , V _{FB} < 0.15V	2.8		4.2	
		POL = GND, V _{FB} < 0.8V	3.8		6.2	
		POL = V _{CC} , V _{FB} > 0.4V	3.8		6.2	
REFERENCE AND FB INPUT						
REF Output Voltage	V _{REF}	V _{CC} = V _{DD} = 2.7V to 5.5V, no load	1.22		1.28	V
REF Load Regulation		I _{REF} = 0μA to 25μA, C _{REF} = 0.1μF			10	mV
FB Set Point	V _{FB}	POL = GND	1.22		1.28	V
		POL = V _{CC}	-15		15	mV
FB Input Bias Current	I _{FB}				±50	nA
POWER OK COMPARATOR, LCDON OUTPUT						
POK Threshold	V _{POK}	V _{POK} rising	1.05		1.20	V
POK Input Current	I _{POK}				±50	nA
LCDON Sink Current	I _{LCDON}	V _{LCDON} = 0.4V, V _{POK} = 1.25V	2			mA
DAC OUTPUT (Notes 2, 3)						
Full-Scale Output Voltage	V _{FS}	-50μA < I _{DACOUT} < 0μA	V _{REF} - 0.02		V _{REF} + 0.02	V
Zero-Scale Output Voltage	V _{ZS}	0μA < I _{DACOUT} < 20μA	0		15	mV
Resolution			6			Bits
Mid-Scale Accuracy	MSA	Mid-scale = V _{REF} x 32/63	-3		3	%
LOGIC INPUTS: POL, ISET, UP, DN, SHDN						
Input Low Level	V _{IL}	2.7V < V _{CC} = V _{DD} < 5.5V			0.7	V
Input High Level	V _{IH}	2.7V < V _{CC} = V _{DD} < 5.5V	2.4			V
Input Bias Current	I _{BIAS}				±1	μA

Note 1: The MAX686 requires a supply voltage at $V_{CC} = V_{DD}$ between $+2.7V$ and $+5.5V$; however, the voltage that supplies the inductor can vary from $+0.8V$ to $+27.5V$, depending on circuit operating conditions.

Note 2: The DAC output is set to its midpoint value at power-on.

Note 3: The DAC setting is guaranteed to remain valid as long as V_{CC} is greater than the V_{CC} DAC Reset Threshold.

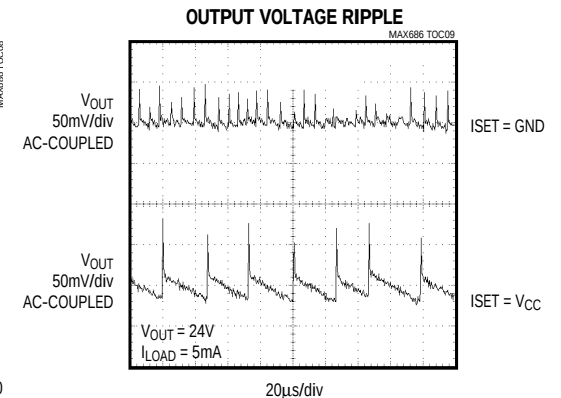
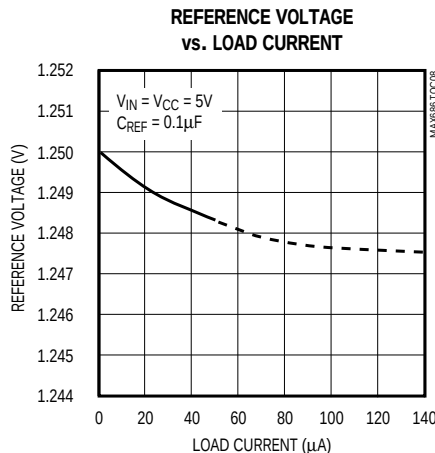
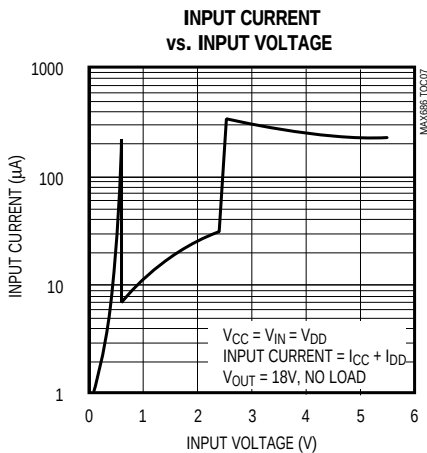
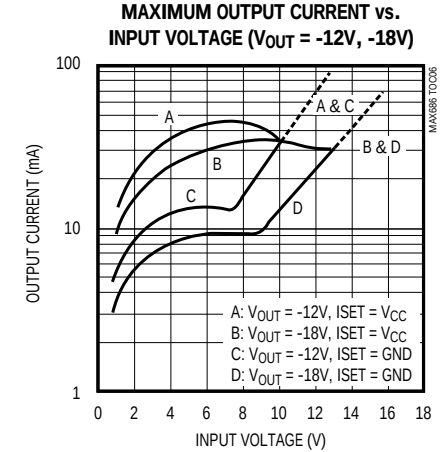
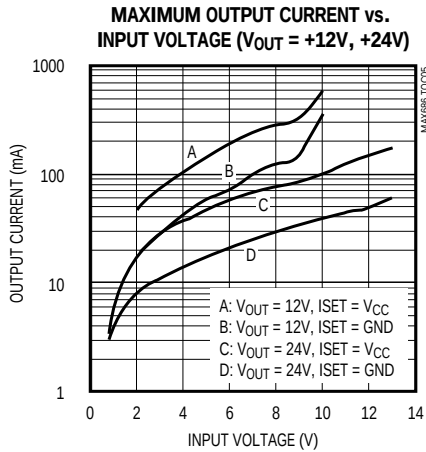
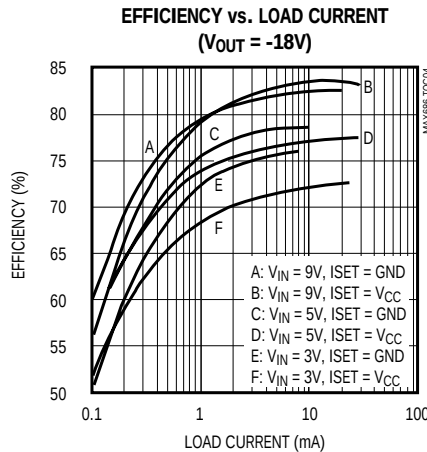
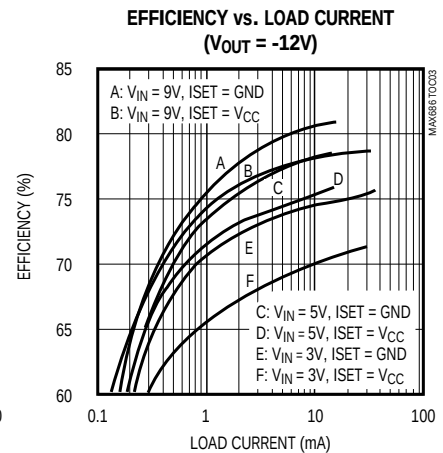
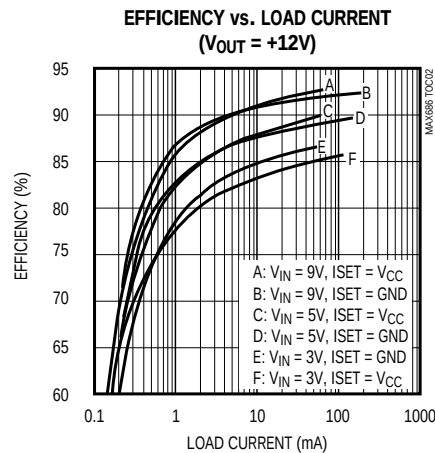
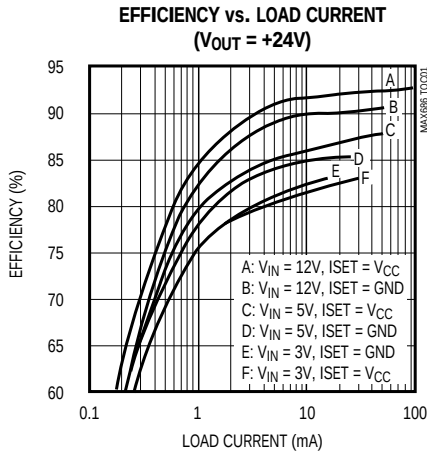
Note 4: Specifications to $-40^\circ C$ are guaranteed by design, not production tested.

DAC-Controlled Boost/Inverter LCD Bias Supply with Internal Switch

Typical Operating Characteristics

(Circuits of Figures 1 and 2, $V_{CC} = V_{DD} = V_{IN} = +5V$, $L1 = 22\mu H$, $\overline{SHDN} = V_{CC}$, $C_{REF} = 0.1\mu F$, $T_A = +25^\circ C$, unless otherwise noted.)

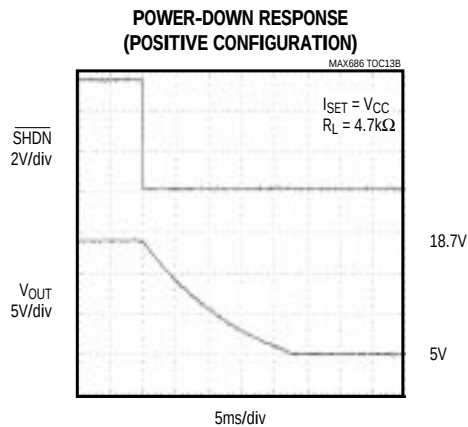
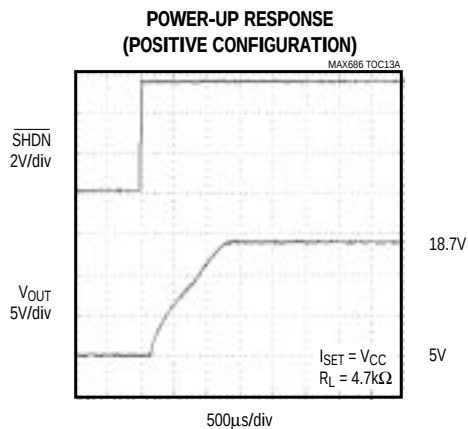
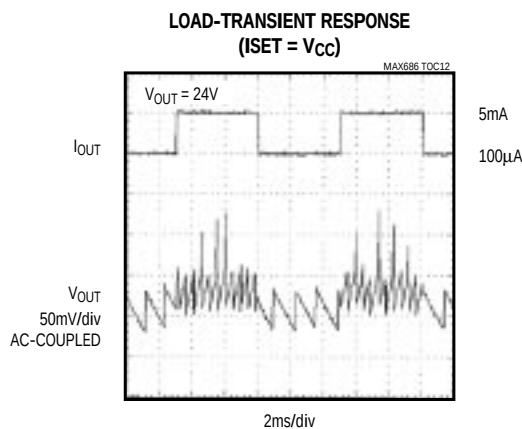
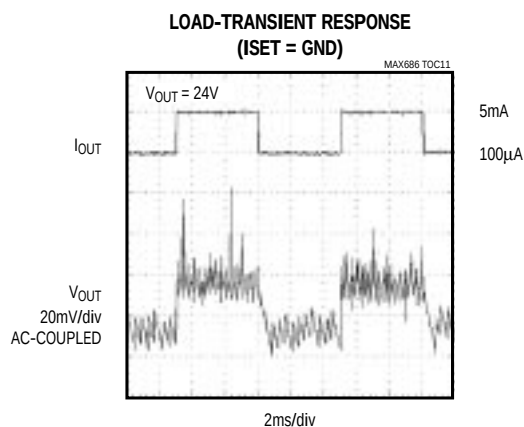
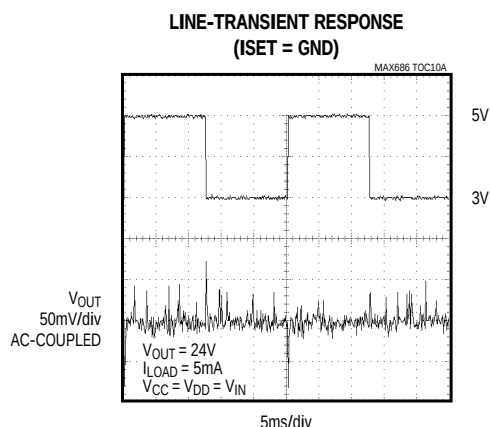
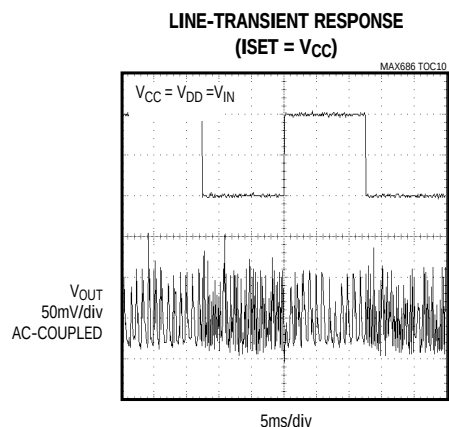
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DAC-Controlled Boost/Inverter LCD Bias Supply with Internal Switch

Typical Operating Characteristics (continued)

(Circuits of Figures 1 and 2, $V_{CC} = V_{DD} = V_{IN} = +5V$, $L_1 = 22\mu H$, $\overline{SHDN} = V_{CC}$, $C_{REF} = 0.1\mu F$, $T_A = +25^\circ C$, unless otherwise noted.)

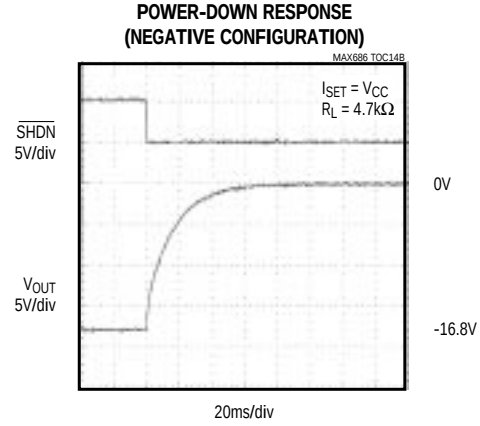
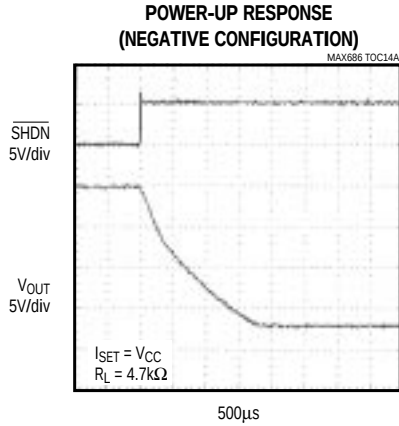


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Typical Operating Characteristics (continued)

(Circuits of Figures 1 and 2, $V_{CC} = V_{DD} = V_{IN} = +5V$, $L1 = 22\mu H$, $\overline{SHDN} = V_{CC}$, $C_{REF} = 0.1\mu F$, $T_A = +25^\circ C$, unless otherwise noted.)



Pin Description

PIN	NAME	FUNCTION
1	PGND	Power Ground. Connect to GND.
2	UP	Increment Output Voltage Input. Increments the DAC on each rising edge such that $ V_{OUT} $ increases.
3	DN	Decrement Output Voltage Input. Decrements the DAC on each rising edge such that $ V_{OUT} $ decreases.
4	POL	Polarity Input. Changes polarity and threshold of FB to allow regulation of either positive or negative output voltages. POL also changes the polarity of the DAC output such that increasing codes always increases the magnitude of the output voltage. Set POL = GND for positive output voltage, or set POL = V_{CC} for negative output voltage.
5	V_{DD}	Gate-Drive Supply for Internal MOSFET. Connect to V_{CC} .
6	ISET	Set LX Current Limit. Sets the peak current limit for the internal switch. Connect to V_{CC} for 500mA current limit. Connect to GND for 250mA current limit.
7	$\overline{SHDN}$	Shutdown Input. A logic low on $\overline{SHDN}$ places the MAX686 in shutdown mode. Connect to V_{CC} for normal operation.
8	DACOUT	DAC Output Voltage
9	REF	Reference Output. Bypass with a $0.1\mu F$ ceramic capacitor to GND.
10	FB	Feedback Input. Connect to an external voltage divider to set the MAX686 output voltage. See the section <i>Setting the Output Voltage with the DAC</i> .
11	POK	Power-OK Sense Input/Power-OK Comparator Input. When the voltage applied to POK is greater than 1.125V, $\overline{LCDON}$ is low. Connect to a resistive voltage divider monitoring V_{IN} or V_{OUT} .
12	V_{CC}	IC Power-Supply Input
13	GND	Ground
14	$\overline{LCDON}$	Power-OK Comparator Open-Drain Output. Connect to external switch to turn LCD power on or off. See the section <i>Controlling the LCD Using POK and $\overline{LCDON}$</i> .
15	N.C.	No Connection. Not internally connected.
16	LX	Drain of Internal 28V, 500mA N-Channel Switch

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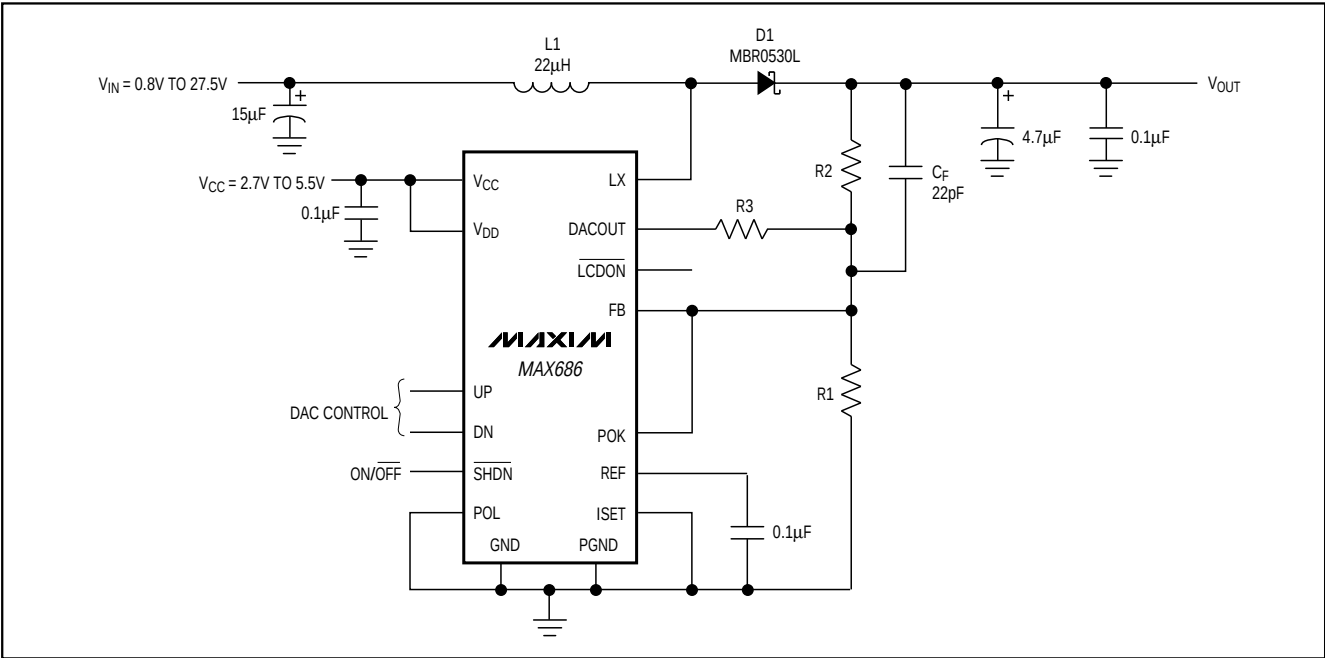


Figure 1. Boost Configuration: Positive Output Voltage

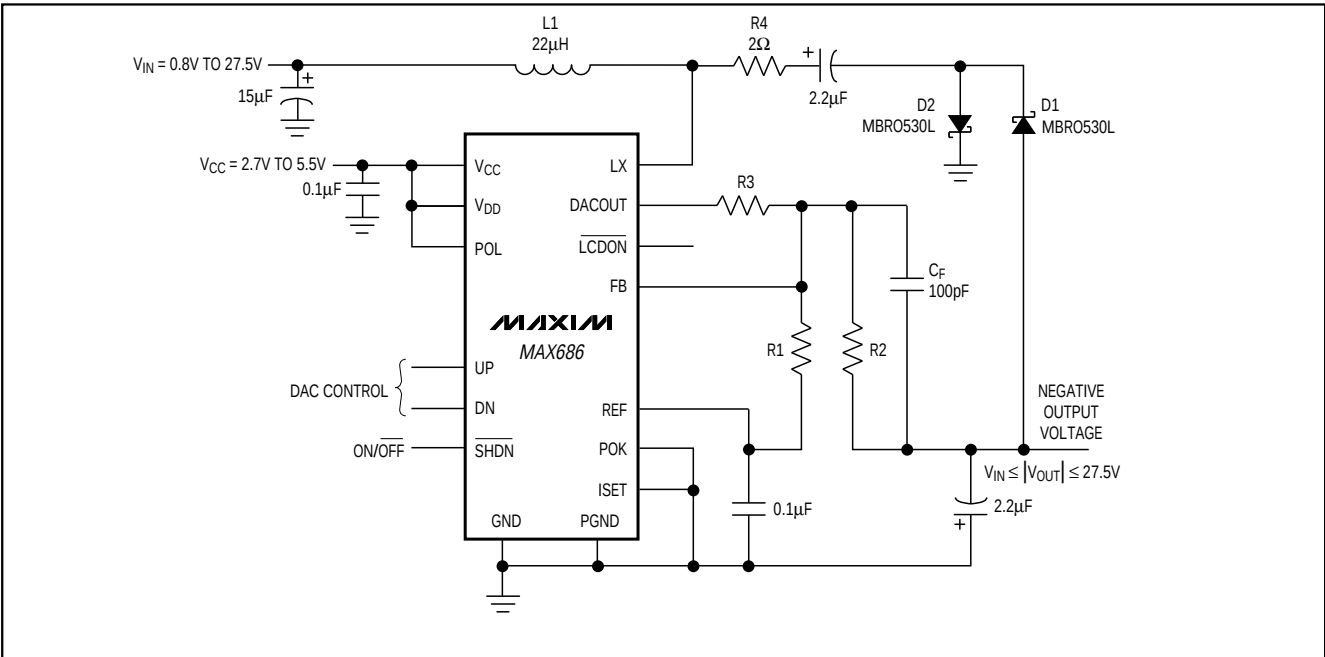


Figure 2. Negative Output Voltage Application Circuit

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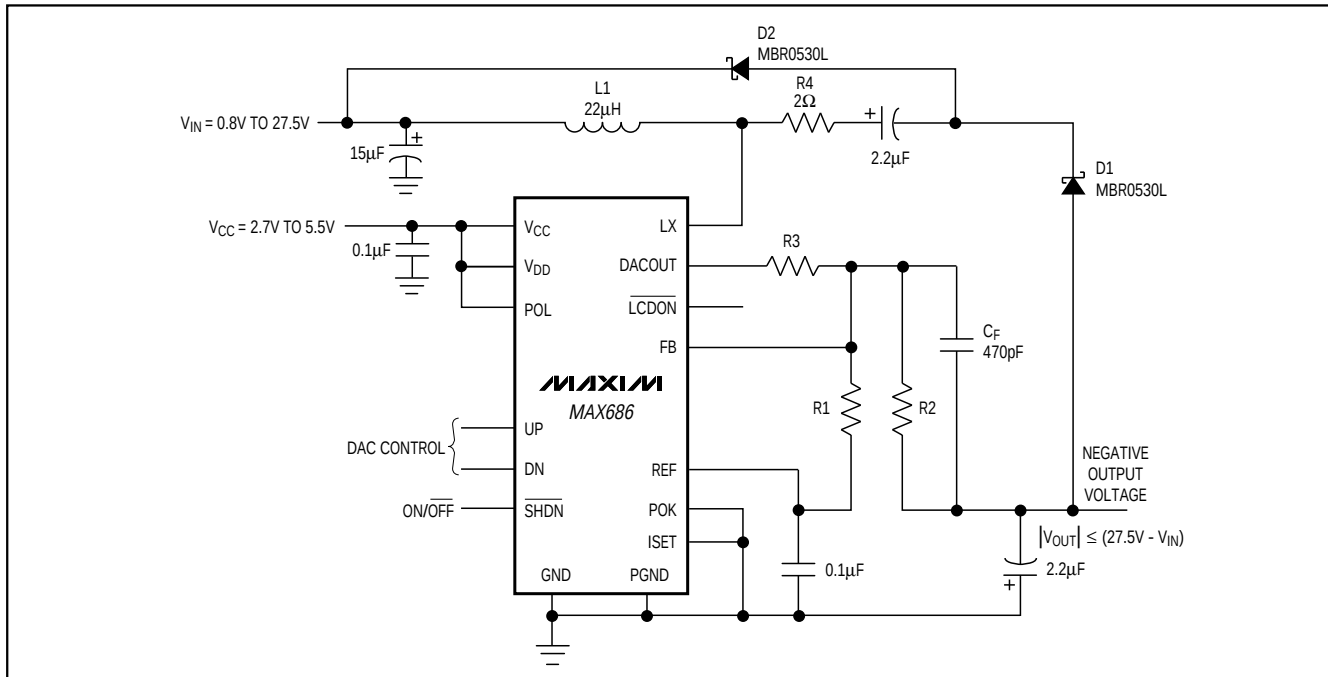


Figure 3. Alternative Negative Output Voltage Application Circuit

Detailed Description

The MAX686 is a step-up converter that contains an internal N-channel MOSFET switch to convert a +0.8V to +27.5V battery voltage to a higher positive or a negative voltage. Figure 1 shows the MAX686 configured to produce a positive output voltage. Figure 2 shows the MAX686 configured with one additional diode and capacitor to produce a negative output voltage. Figure 3 shows an alternative method for developing negative output voltages. Set the output voltage with an external resistor-divider network. Adjust the output voltage with the internal digital-to-analog converter (DAC). The MAX686's current-limited pulse-frequency-modulation (PFM) control scheme has programmable current limiting and provides high efficiency over a wide range of load conditions.

Boost Control Scheme (POL = GND)

A combination of peak current limiting and a pair of one-shots controls the MAX686 switching. During the on-cycle, the internal switch closes, and current through the inductor ramps up until either the fixed 10µs maximum on-time expires (at low input voltages) or the switch peak current limit is reached. The peak current limit is selectable to either 500mA (ISET = VCC) or 250mA (ISET = GND) (see the section *Setting the Peak Inductor Current Limit*).

After the on-cycle terminates, the switch turns off, and the inductor charges the output capacitor through the diode. If the output is out of regulation after the minimum off-time has transpired, another on-cycle begins. If the output is within regulation when the minimum off-time transpires, the off-cycle extends until the output falls out of regulation, at which point an on-cycle starts.

The MAX686 regulates the voltage on FB (V_{FB}) to 1.25V. When the output is well below regulation (V_{FB} is less than 1V and the switch current limit is exceeded), the MAX686 operates in initial power-up mode, and the minimum off-time increases to 5µs to provide soft-start. The switching frequency, which depends on the load, the input voltage, and the output voltage, can be as high as 300kHz.

Inverting Control Scheme (POL = VCC)

In inverting operation, the MAX686 regulates the voltage on FB (V_{FB}) to 0V, and the error amplifier's polarity is reversed. The minimum off-time changes to 3.5µs for negative output voltages. When the output is well below regulation (V_{FB} is 0.25V or more and the switch current limit is exceeded), initial power-up is assumed, and the minimum off-time increases to 5µs to provide soft-start.

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Power-OK Comparator

POK is the input to the power-OK comparator. The comparator drives an internal N-channel MOSFET. The MOSFET's open-drain output, $\overline{\text{LCDON}}$, can drive an external PNP transistor or P-channel MOSFET, switching a positive V_{OUT} to the LCD (Figures 6 and 7). When the voltage at POK exceeds 1.125V (power OK), $\overline{\text{LCDON}}$ goes low, turning on the external PNP transistor. When the voltage at POK drops below 1.125V (power not OK), the external PNP transistor turns off, cutting off power to the LCD display. This feature ensures that the LCD display is not damaged due to improper voltage levels. During shutdown or undervoltage lockout, $\overline{\text{LCDON}}$ is high impedance.

Shutdown Mode

When $\overline{\text{SHDN}}$ is low, the MAX686 enters shutdown mode, in which the control circuit, POK comparator, DAC output buffer, reference, and internal biasing circuitry turn off. The DAC setting is stored as long as V_{CC} remains above the DAC reset threshold. Supply current drops to 1.5 μA . $\overline{\text{SHDN}}$ is a logic-level input; connect it to V_{CC} for normal operation.

The output voltage in shutdown mode depends on the output voltage polarity. In the positive output voltage configuration (Figure 1), the output is directly connected to the input through the diode (D1) and the inductor (L1). When the device is in shutdown mode, the output voltage falls to one diode drop below the input voltage, and any load connected to the output may still conduct current. In the negative output voltage configuration (Figures 2 and 3), there is no DC path between the input and the output, and the output falls to GND in shutdown mode.

Internal DAC

The MAX686 contains an internal 6-bit counter and DAC to control the output voltage digitally (see the section *Setting the Output Voltage with the DAC*). The UP and DN input pins drive an internal up/down counter that directly controls the DAC. To increase the magnitude of V_{OUT} in the boost configuration, apply a rising edge to UP. This decreases the DAC output voltage one step and correspondingly increases V_{OUT} . Conversely, to decrease the magnitude of V_{OUT} , apply a rising edge to DN. This increases the DAC output voltage one step and correspondingly decreases V_{OUT} . The UP and DN control direction reverses for a negative output to maintain the same control direction of the absolute magnitude of the output voltage. Upon power-up, the DAC code internally goes to mid-scale. The DAC's internal counter does not roll over once it reaches full scale or zero. Therefore, additional rising

edges to make the counter roll over are ignored, preventing unexpected undervoltages or overvoltages.

Internal Reference

The MAX626's 1.25V internal reference is accurate to $\pm 2\%$ over temperature. It can source up to 50 μA of current and should be bypassed with at least a 0.1 μF capacitor. See the *Bypass Capacitors* section.

Design Procedure

Setting the Output Voltage with the DAC

For either positive or negative output voltage applications, set the MAX686's output voltage using three external resistors (R1, R2, and R3) as shown in Figures 1, 2, and 3. Since the input bias current at FB has a 50nA maximum value, large resistors can be used in the feedback loop without a significant loss of accuracy. Select R1 to be in the 10k Ω to 220k Ω range and calculate R2 and R3 using the applicable equations from the following subsections.

Setting the Minimum Positive Output Voltage

The minimum output voltage is set with the resistor-divider (R1-R2, Figure 1) from V_{OUT} to FB. The minimum output voltage occurs when $V_{\text{DACOUT}} = V_{\text{FB}} = 1.25\text{V}$. Therefore, R3 has no effect on the minimum output voltage. Choose R1 to be 120k Ω so that the current in the divider is about 10 μA . Then determine R2 as follows:

$$R2 = R1 \times (V_{\text{OUT(MIN)}} - V_{\text{FB}}) / V_{\text{FB}}$$

For example, if $V_{\text{OUT(MIN)}} = 12.5\text{V}$:

$$R2 = 120\text{k}\Omega \times (12.5 - 1.25) / (1.25) = 1.08\text{M}\Omega$$

Mount R1 and R2 close to the FB pin to minimize parasitic capacitance.

Setting the Maximum Positive Output Voltage

The DAC is adjustable from 0V to 1.25V in 64 steps, and $1\text{LSB} = 1.25\text{V} / 63 = 19.8\text{mV}$. Calculate R3 to adjust V_{OUT} with DACOUT (Figure 1).

For $V_{\text{OUT(MAX)}} = 25\text{V}$ and $V_{\text{OUT(MIN)}} = 12.5\text{V}$, determine R3 as follows:

$$\begin{aligned} R3 &= R2 \times (V_{\text{FB}}) / (V_{\text{OUT(MAX)}} - V_{\text{OUT(MIN)}}) \\ &= 1.08\text{M}\Omega \times (1.25) / (25 - 12.5) = 108\text{k}\Omega \end{aligned}$$

The general form for V_{OUT} as a function of the DAC output (V_{DACOUT}) is:

$$V_{\text{OUT}} = V_{\text{OUT(MIN)}} + (V_{\text{FB}} - V_{\text{DACOUT}}) \times R2 / R3$$

At power-up, the DAC resets to mid-scale where $V_{\text{DACOUT}} = 0.635\text{V}$. Therefore, the output voltage after power-up is:

$$\begin{aligned} V_{\text{OUT(MID)}} &= V_{\text{OUT(MIN)}} + (1.25 - 0.635) \times \\ &\quad R2 / R3 = 18.65\text{V} \end{aligned}$$

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Note that for a positive output voltage, V_{OUT} increases as V_{DACOUT} decreases. $V_{OUT(MAX)}$ corresponds to $V_{DACOUT} = 0V$, and $V_{OUT(MIN)}$ corresponds to $V_{DACOUT} = 1.25V$.

Setting the Minimum Negative Output Voltage

For a negative output voltage, the FB threshold voltage (V_{FB}) is $0V$, and $R1$ is placed between FB and REF (Figures 2 and 3). Again, choose $R1$ to be $120k\Omega$ so that the current in the divider is about $10\mu A$. Then determine $R2$ as follows:

$$R2 = R1 \times |V_{OUT} / V_{REF}|$$

For example, if $V_{OUT(MIN)} = -12.5V$:

$$R2 = 120k\Omega \times |(-12.5) / (1.25)| = 1.2M\Omega$$

Setting the Maximum Negative Output Voltage

Assume $V_{OUT(MAX)} = -25V$ and $V_{OUT(MIN)} = -12.5V$, then determine $R3$ and $V_{OUT(MID)}$ as follows:

$$\begin{aligned} R3 &= R2 \times (V_{FB} - V_{DACOUT(MAX)}) / (V_{OUT(MAX)} - V_{OUT(MIN)}) \\ &= 1.2M\Omega \times (0 - 1.25) / (-25 - -12.5) = 120k\Omega \end{aligned}$$

For a negative output voltage,

$$V_{OUT} = V_{OUT(MIN)} + (V_{FB} - V_{DACOUT}) \times R2 / R3.$$

At power-up, the DAC resets to mid-scale where $V_{DACOUT} = 0.635V$. Therefore, the output voltage after reset is:

$$V_{OUT(MID)} = -12.5 + (0 - 0.635) \times (1.2M) / (120k) = -18.85V$$

Note that for a negative output voltage, $|V_{OUT}|$ increases as V_{DACOUT} increases. $|V_{OUT(MAX)}|$ corresponds to $V_{DACOUT} = 1.25V$, and $|V_{OUT(MIN)}|$ corresponds to $V_{DACOUT} = 0V$.

Setting the Output Voltage without the DAC

The MAX686 may be used without the DAC to control the output voltage. For either positive or negative output voltage applications, set the MAX686's output voltage using only two external resistors ($R1$ and $R2$) as shown in Figure 1, 2, or 3. Since the input bias current at FB has a $50nA$ maximum value, large resistors can be used in the feedback loop without a significant loss of accuracy. Select $R1$ to be in the $10k\Omega$ to $220k\Omega$ range and calculate $R2$ using the applicable equations from the following subsections.

Setting the Positive Output Voltage

Use the circuit of Figure 1, connecting POL to GND and omitting $R3$. Connecting POL to GND sets the threshold voltage at FB to V_{REF} . Choose the value of $R1$ in the $10k\Omega$ to $220k\Omega$ range and calculate $R2$ as follows:

$$R2 = R1 \times (V_{OUT} / V_{REF} - 1)$$

where $V_{REF} = 1.25V$.

Setting the Negative Output Voltage

For negative output voltages, configure $R1$ and $R2$ as shown in Figures 2 and 3, connecting POL to V_{CC} and omitting $R3$. Connecting POL to V_{CC} sets the FB threshold voltage to GND for negative output voltages. Choose $R1$ in the $10k\Omega$ to $220k\Omega$ range and calculate $R2$ as follows:

$$R2 = R1 \times |V_{OUT}| / V_{REF}$$

where $V_{REF} = 1.25V$.

Figures 2 and 3 demonstrate two possible methods of generating a negative voltage with the MAX686. In Figure 3, D2 connects to the input supply (V_{IN}). This connection features the best output ripple performance, but $|V_{OUT}|$ must be limited to values less than $-27.5V - V_{IN}$. If the application requires a larger negative voltage, use the method of Figure 2, connecting D2 to GND. This method allows a maximum output voltage of $-27.5V$, but $|V_{OUT}|$ must be greater than V_{IN} .

Setting the Peak Inductor Current Limit

External current-limit selection provides added control over the MAX686's output performance. A higher current limit increases the amount of energy stored in the inductor during each cycle, which provides higher output current capability. For higher output current applications, choose the $500mA$ current-limit option by connecting ISET to V_{CC} . When the load requires lower output current, the $250mA$ current limit provides several advantages. First, a smaller inductor saves board area and cost. Second, smaller energy transfers per cycle reduce output ripple for a given capacitor. Connecting ISET to GND selects the $250mA$ current-limit option. Connecting ISET to V_{CC} selects the $500mA$ current-limit option. Refer to the *Typical Operating Characteristics* for efficiency and load current graphs at each ISET current setting.

Selecting Inductors

The MAX686's high switching frequency allows for the use of a small inductor. The $22\mu H$ inductor shown in Figures 1, 2, and 3 is recommended for most applications, although values between $10\mu H$ and $47\mu H$ are acceptable. Use inductors with a ferrite core or equivalent; powder iron cores are not recommended for use with high switching frequencies. The inductor's incremental saturation rating must exceed the selected current limit. For highest efficiency, use an inductor with a low DC resistance (under $200m\Omega$). See Table 1 for a list of inductor suppliers.

DAC-Controlled Boost/Inverter LCD Bias Supply with Internal Switch

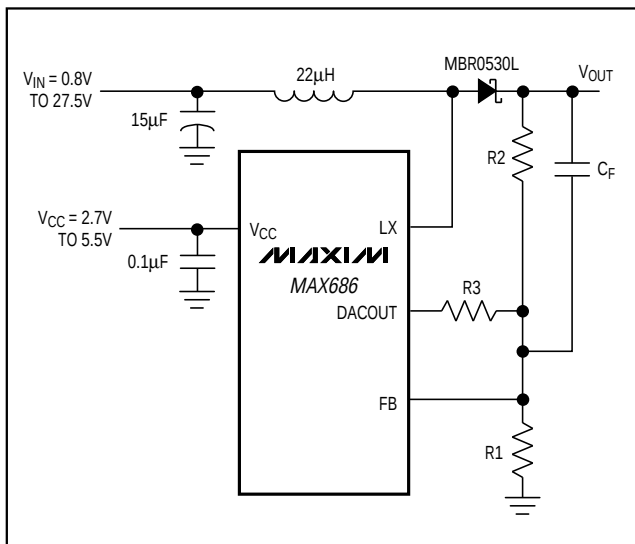


Figure 4. Feed-Forward Capacitor

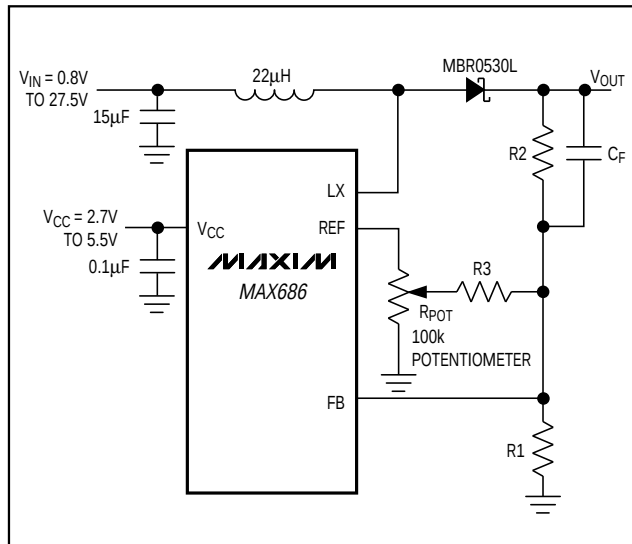


Figure 5. Using a Potentiometer to Adjust Output Voltage

Table 1. Component Suppliers

SUPPLIER	PHONE	FAX
CAPACITORS		
AVX: TPS series	(803) 946-0690	(803) 626-3123
Matsuo: 267 series	(714) 969-2491	(714) 960-6492
Sprague 595D series	(603) 224-1961	(603) 224-1430
DIODES		
Motorola: MBR0530L	(602) 303-5454	(602) 994-6430
Nihon: EC11 FS1 series	(805) 867-2555	(805) 867-2698
INDUCTORS		
Coilcraft: DO1608 and DT1608 series	(847) 639-6400	(847) 639-1469
Murata-Erie: LQH4 series	(814) 237-1431	(814) 238-0490
Sumida: CD43, CD54, and CD74 series	(847) 956-0666	(847) 956-0702
TDK: NLC565050 series	(847) 390-4373	(847) 390-4428

Selecting Diodes

The MAX686's high switching frequency demands a high-speed rectifier. Schottky diodes, such as the 1N5818 or MBR0530L, are recommended. Make sure that the diode's peak current rating exceeds the peak current set by ISET and that its breakdown voltage exceeds the output voltage. Schottky diodes are preferred due to their low forward voltage. However, ultra-high-speed silicon rectifiers are also acceptable. Table 1 lists Schottky diode suppliers.

Selecting Capacitors

Output Filter Capacitors

The primary selection criterion for the output filter capacitor is low equivalent series resistance (ESR). The product of the peak inductor current and the output filter capacitor's ESR determines the amplitude of the high-frequency ripple seen on the output voltage. These requirements can be balanced by appropriately selecting the current limit, as discussed in the *Setting the Peak Inductor Current Limit* section. Table 1 lists some low-ESR capacitor suppliers.

Bypass Capacitors

Although the output current of many MAX686 applications may be relatively small, the input supply must be able to source current transients equal to the ISET current limit. The input bypass capacitor reduces the peak currents drawn from the voltage source and reduces noise caused by the MAX686's switching action. The input source impedance determines the size of the capacitor required at the input (V_{IN}). As with the output filter capacitor, low ESR is the primary consideration. A 15µF, low-ESR capacitor is adequate for most applications, although smaller bypass capacitors may also be acceptable in light-load applications. Bypass the IC separately with a 0.1µF ceramic capacitor placed as close as possible to the Vcc and GND pins.

Bypass REF to GND with a 0.1µF ceramic capacitor for REF currents up to 25µA. REF can source up to 50µA of current for external loads. For $25\mu A \leq I_{REF} \leq 50\mu A$, bypass REF with a 0.47µF capacitor.

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Parallel a feed-forward capacitor (C_F) across R2 to compensate the feedback loop and ensure stability (Figure 4). Use values up to 100pF for most applications. Choose the lowest capacitor value that ensures stability; high capacitance values may degrade line regulation.

DAC-Controlled Boost/Inverter LCD Bias Supply with Internal Switch

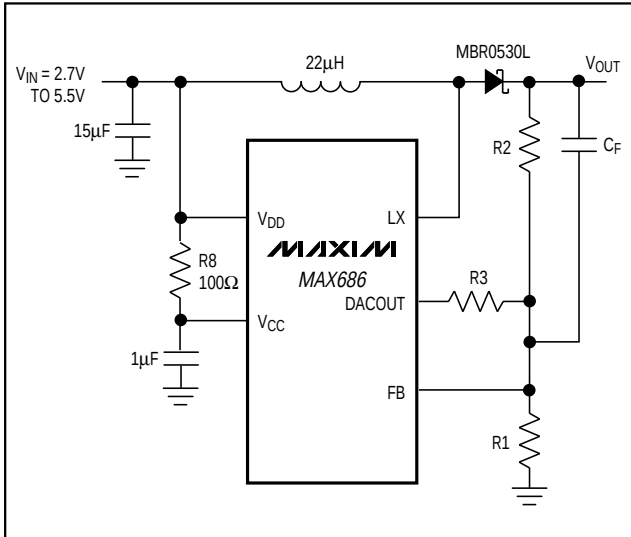


Figure 8. Using a Common Supply-Voltage Source

R6 turns it off when $\overline{\text{LCDON}}$ goes high. R6 and R7 can be the same value. Choose R7 such that the minimum base current is greater than 1/50 of the collector current. For example, assume $V_{\text{OUT(MIN)}} = 12.5\text{V}$ and $I_{\text{LCD}} = 10\text{mA}$ and then determine R7 as follows:

$$R7 \leq 50 \times (12.5 - 0.7) / 10\text{mA} = 59\text{k}\Omega$$

Remember that the LCD voltage, V_{OUTSW} , is the regulated output voltage minus the drop across the PNP switch (300mV typ).

Connecting V_{IN} to V_{CC}

The MAX686 (V_{CC} , V_{DD}) and the inductor (V_{IN}) can be powered from the same source as long as the +5.5V V_{CC} maximum limit is not violated. To ensure stability, connect V_{IN} and V_{DD} directly to the source, connect

V_{CC} to the source through a 100Ω resistor (R8), and bypass V_{CC} with a 1µF ceramic capacitor as shown in Figure 8. Since the supply current is very small, the voltage drop across R8 is insignificant and does not degrade performance. The RC isolates V_{CC} from the switching noise created by the inductor and internal power switch.

Although, in many cases, the MAX686 and the inductor are powered from the same source, it is often advantageous in battery-powered applications to power the MAX686 IC (V_{CC} , V_{DD}) from an available regulated supply and to power the inductor (V_{IN}) directly from a battery. The MAX686 requires a +2.7V to +5.5V supply at V_{CC} , but the inductor can be powered from voltages as low as 0.8V, significantly increasing usable battery life.

Layout Considerations

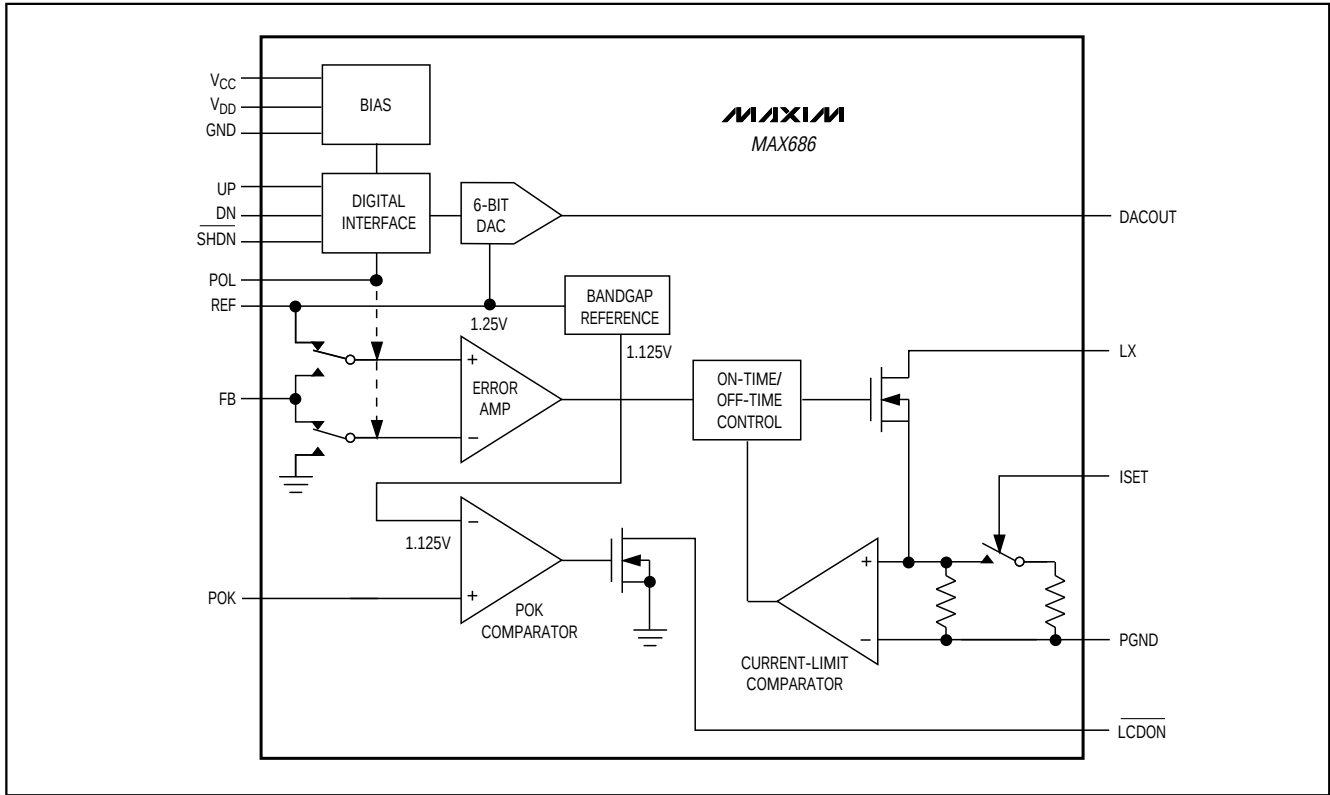
Proper PC board layout is essential due to high current levels and fast switching waveforms that radiate noise. It is recommended that initial prototyping be performed using the MAX686 evaluation kit or equivalent PC board-based design. Breadboards or proto-boards should never be used when prototyping switching regulators.

Connect the GND pin, the input bypass-capacitor ground lead, and the output filter-capacitor ground lead to a single point (star ground configuration) to minimize ground noise and improve regulation. Also, minimize lead lengths to reduce stray capacitance, trace resistance, and radiated noise, with preference given to the feedback circuit, the ground circuit, and LX. Place R1 and R2 as close to the feedback pin as possible. Place the bypass capacitors as close to the pins as possible.

Refer to the MAX686 evaluation kit data sheet for an example of proper board layout.

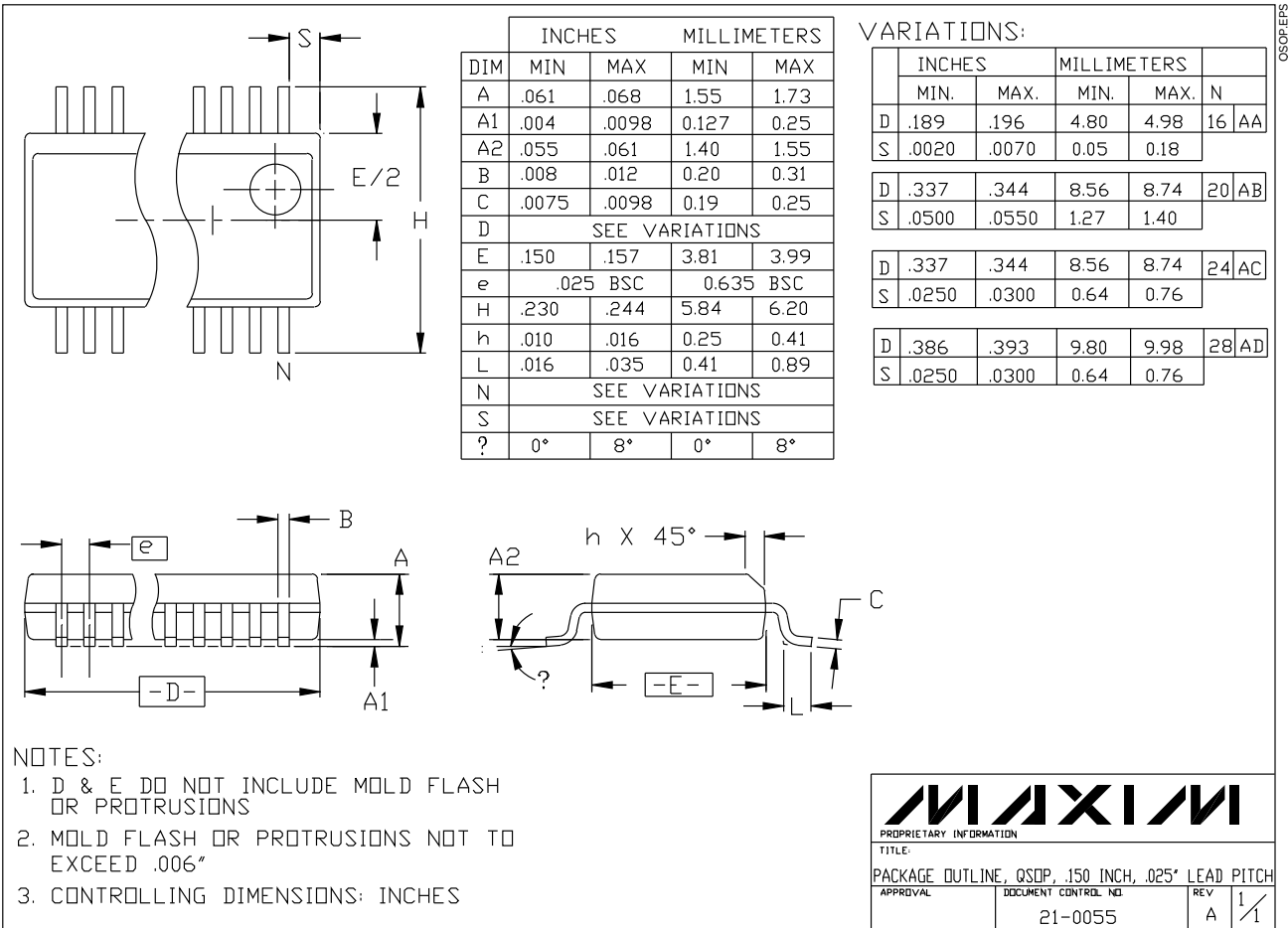
DAC-Controlled Boost/Inverter LCD Bias Supply with Internal Switch

Functional Diagram



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DAC-Controlled Boost/Inverter LCD Bias Supply with Internal Switch



Chip Information

TRANSISTOR COUNT: 1325

SUBSTRATE CONNECTED TO GND