

Fast, Low-Voltage, Dual 4Ω SPDT CMOS Analog Switches

ABSOLUTE MAXIMUM RATINGS

(Voltages Referenced to GND)

V+, IN_	-0.3V to +6V
COM_, NC_, NO_ (Note 1)	-0.3V to (V+ + 0.3V)
Continuous Current into Any Terminal	±30mA
Peak Current into COM_, NC_, NO_ (pulsed at 1ms, 10% duty cycle)	±100mA

Continuous Power Dissipation (T_A = +70°C)

10-Pin μMAX (derate 4.7mW/°C above +70°C)	330mW
10-Pin Thin QFN (derate 24.4mW/°C above +70°C)	1951mW
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Note 1: Signals on NO_, NC_, or COM_ exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +4.5V to +5.5V, V_{IH} = +2.4V, V_{IL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 9)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
ANALOG SWITCH							
Analog Signal Range	V _{COM_} , V _{NO_} , V _{NC_}		0		V+	V	
On-Resistance	R _{ON}	V+ = 4.5V, I _{COM_} = 10mA, V _{NO_} or V _{NC_} = 0 to V+	T _A = +25°C	2.5	4	Ω	
			T _A = T _{MIN} to T _{MAX}		4.5		
On-Resistance Match Between Channels (Notes 3, 4)	ΔR _{ON}	V+ = 4.5V, I _{COM_} = 10mA, V _{NO_} or V _{NC_} = 0 to V+	T _A = +25°C	0.1	0.2	Ω	
			T _A = T _{MIN} to T _{MAX}		0.4		
On-Resistance Flatness (Note 5)	R _{FLAT(ON)}	V+ = 4.5V, I _{COM_} = 10mA, V _{NO_} or V _{NC_} = 0 to V+	T _A = +25°C	0.5	1	Ω	
			T _A = T _{MIN} to T _{MAX}		1.2		
NO_, NC_ Off-Leakage Current (Note 6)	I _{NC_(OFF)} , I _{NO_(OFF)}	V+ = 5.5V; V _{COM_} = 1V, 4.5V; V _{NO_} or V _{NC_} = 4.5V, 1V	T _A = +25°C	-0.1	±0.01	0.1	nA
			T _A = T _{MIN} to T _{MAX}	-0.3		0.3	
COM_ Off-Leakage Current (Note 6)	I _{COM_(OFF)}	V+ = 5.5V; V _{COM_} = 1V, 4.5V; V _{NO_} or V _{NC_} = 4.5V, 1V	T _A = +25°C	-0.1	±0.01	0.1	nA
			T _A = T _{MIN} to T _{MAX}	-0.3		0.3	
COM_ On-Leakage Current (Note 6)	I _{COM_(ON)}	V+ = 5.5V; V _{COM_} = 4.5V, 1V; V _{NO_} or V _{NC_} = 4.5V, 1V or floating	T _A = +25°C	-0.1	±0.01	0.1	nA
			T _A = T _{MIN} to T _{MAX}	-0.3		0.3	
DIGITAL I/O (IN1, IN2)							
Input Logic High	V _{IH}		2.4			V	
Input Logic Low	V _{IL}				0.8	V	
Input Leakage Current	I _{IH} , I _{IL}	V _{IN_} = 0 or +5.5V	-100	5	100	nA	

Fast, Low-Voltage, Dual 4Ω SPDT CMOS Analog Switches

MAX4635/MAX4636

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = +4.5V to +5.5V, V_{IH} = +2.4V, V_{IL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 9)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC						
Turn-On Time (Note 6)	t _{ON}	V _{NO_} , V _{VNC_} = 3V; R _L = 300Ω, C _L = 35pF, Figure 1a	T _A = +25°C	12	14	ns
			T _A = T _{MIN} to T _{MAX}		16	
Turn-Off Time (Note 6)	t _{OFF}	V _{NO_} , V _{VNC_} = 3V; R _L = 300Ω, C _L = 35pF, Figure 1a	T _A = +25°C	5	6	ns
			T _A = T _{MIN} to T _{MAX}		8	
Break-Before-Make Time (Note 6)	t _{BBM}	V _{NO_} , V _{VNC_} = 3V; R _L = 300Ω, C _L = 35pF, Figure 1b	T _A = +25°C	7		ns
			T _A = T _{MIN} to T _{MAX}	1		
Charge Injection	Q	V _{GEN} = 2V, R _{GEN} = 0, C _L = 1.0nF, Figure 2		2		pC
NO_, NC_ Off-Capacitance	C _{NO_(OFF)} , C _{VNC_(OFF)}	V _{NO_} , V _{VNC_} = GND, f = 1MHz, Figure 3		9		pF
COM_ On-Capacitance	C _{COM_(ON)}	V _{COM_} = GND, f = 1MHz, Figure 3		32		pF
Off-Isolation (Note 7)	V _{ISO}	C _L = 5pF, R _L = 50Ω, f = 10MHz, Figure 4		-52		dB
		C _L = 5pF, R _L = 50Ω, f = 1MHz, Figure 4		-65		
Crosstalk (Note 8)	V _{CT}	C _L = 5pF, R _L = 50Ω, f = 10MHz, Figure 4		-66		dB
		C _L = 5pF, R _L = 50Ω, f = 1MHz, Figure 4		-67		
Total Harmonic Distortion	THD	R _L = 600Ω, V _{NO_} = 5V _{p-p} , f = 20Hz to 20kHz		0.1		%
SUPPLY						
Positive Supply Current	I+	V+ = 5.5V, V _{IN_} = 0 or V+		0.001	1.0	μA

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +2.7V to +3.6V, V_{IH} = +2.0V, V_{IL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 9)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
ANALOG SWITCH							
Analog Signal Range	V _{COM_} , V _{NO_} , V _{VNC_}		0		V+	V	
On-Resistance	R _{ON}	V+ = 2.7V, I _{COM_} = 10mA, V _{NO_} or V _{VNC_} = 0 to V+	T _A = +25°C	5	5.5	Ω	
			T _A = T _{MIN} to T _{MAX}		8		
On-Resistance Match Between Channels (Notes 3, 4)	ΔR _{ON}	V+ = 2.7V, I _{COM_} = 10mA, V _{NO_} or V _{VNC_} = 0 to V+	T _A = +25°C	0.1	0.2	Ω	
			T _A = T _{MIN} to T _{MAX}		0.4		
On-Resistance Flatness (Note 5)	R _{FLAT(ON)}	V+ = 2.7V, I _{COM_} = 10mA, V _{NO_} or V _{VNC_} = 0 to V+	T _A = +25°C	1.5	2	Ω	
			T _A = T _{MIN} to T _{MAX}		2.5		
NO_, NC_ Off-Leakage Current (Note 6)	I _{NO_(OFF)} , I _{VNC_(OFF)}	V+ = 3.3V; V _{COM_} = 1V, 3V; V _{NO_} or V _{VNC_} = 3V, 1V	T _A = +25°C	-0.1	±0.01	0.1	nA
			T _A = T _{MIN} to T _{MAX}	-0.3		0.3	
COM_ Off-Leakage Current (Note 6)	I _{COM_(OFF)}	V+ = 3.3V; V _{COM_} = 1V, 3V; V _{NO_} or V _{VNC_} = 3V, 1V	T _A = +25°C	-0.1	±0.01	0.1	nA
			T _A = T _{MIN} to T _{MAX}	-0.3		0.3	

Fast, Low-Voltage, Dual 4Ω SPDT CMOS Analog Switches

ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V+ = +2.7V to +3.6V, V_{IH} = +2.0V, V_{IL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 9)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
COM_ On-Leakage Current (Note 6)	I _{COM(ON)}	V+ = 3.3V; V _{COM_} = 1V, 3V; V _{NO_} or V _{N_} = 1V, 3V, or floating	T _A = +25°C	-0.1	±0.01	0.1	nA
			T _A = T _{MIN} to T _{MAX}	-0.3		0.3	
DIGITAL I/O (IN1, IN2)							
Input Logic High	V _{IH}		2.0			V	
Input Logic Low	V _{IL}				0.4	V	
Input Leakage Current	I _{IH} , I _{IL}	V _{IN_} = 0 or +5.5V	-100	5	100	nA	
DYNAMIC							
Turn-On Time (Note 6)	t _{ON}	V _{NO_} , V _{N_} = 2V; C _L = 35pF, R _L = 300Ω, Figure 1a	T _A = +25°C	14	18	ns	
			T _A = T _{MIN} to T _{MAX}		20		
Turn-Off Time (Note 6)	t _{OFF}	V _{NO_} , V _{N_} = 2V; C _L = 35pF, R _L = 300Ω, Figure 1a	T _A = +25°C	6	8	ns	
			T _A = T _{MIN} to T _{MAX}		10		
Break-Before-Make Time (Note 6)		V _{NO_} , V _{N_} = 2V; C _L = 35pF, R _L = 300Ω, Figure 1b	T _A = +25°C	7		ns	
			T _A = T _{MIN} to T _{MAX}	1			
Charge Injection	Q	V _{GEN} = 1.5V, R _{GEN} = 0, C _L = 1.0nF, Figure 2		11		pC	
NO_, NC_ Off-Capacitance	C _{NO_(OFF)} , C _{N_(OFF)}	V _{NO_} , V _{N_} = GND, f = 1MHz, Figure 3		9		pF	
COM On-Capacitance	C _{COM(ON)}	V _{COM} = GND, f = 1MHz, Figure 3		32		pF	
Off-Isolation (Note 7)	V _{ISO}	C _L = 5pF, R _L = 50Ω, f = 10MHz, Figure 4		-52		dB	
		C _L = 5pF, R _L = 50Ω, f = 1MHz, Figure 4		-65			
Crosstalk (Note 8)	V _{CT}	C _L = 5pF, R _L = 50Ω, f = 10MHz, Figure 4		-66		dB	
		C _L = 5pF, R _L = 50Ω, f = 1MHz, Figure 4		-67			
SUPPLY							
Positive Supply Current	I+	V+ = 3.6V, V _{IN} = 0 or +3.6V		0.001	1	μA	

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 3: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

Note 4: ΔR_{ON} matching specifications for QFN-packaged parts are guaranteed by design.

Note 5: Flatness is defined as the difference between the maximum and minimum values of on-resistance as measured over the specified analog signal ranges.

Note 6: Guaranteed by design.

Note 7: Off-Isolation = $20 \log_{10} (V_{COM} / V_{NO})$, V_{COM} = output, V_{NO} = input to off switch.

Note 8: Between any two switches.

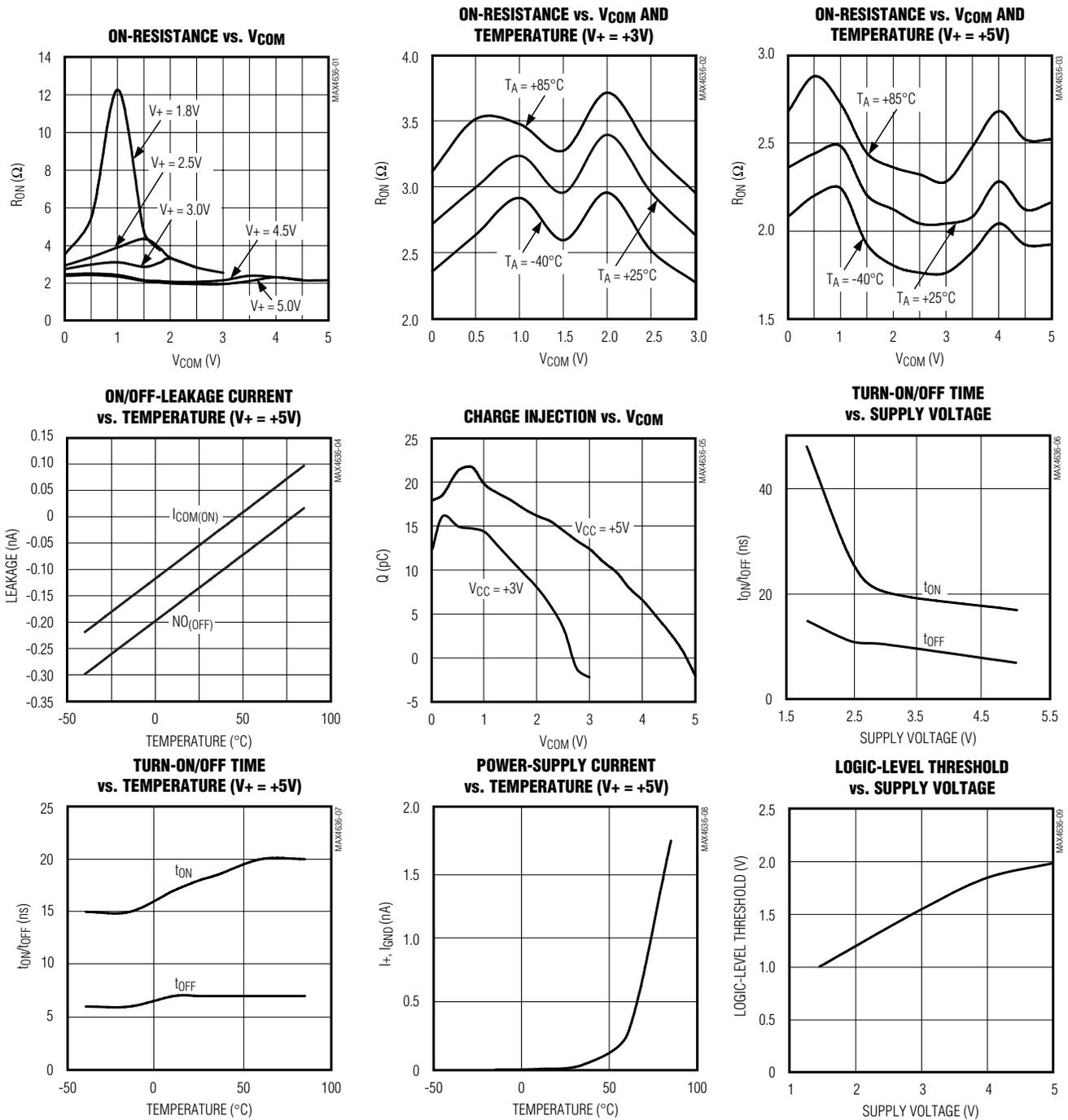
Note 9: QFN packaged parts are tested at +25°C and guaranteed by design and correlation over the entire temperature range.

Fast, Low-Voltage, Dual 4Ω SPDT CMOS Analog Switches

Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

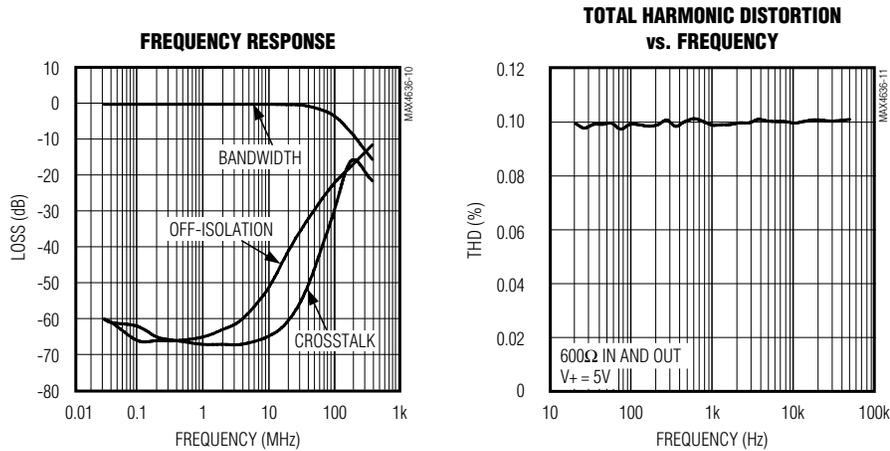
MAX4635/MAX4636



Fast, Low-Voltage, Dual 4Ω SPDT CMOS Analog Switches

Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)



Pin Description

PIN		NAME	FUNCTION
MAX4635	MAX4636		
1	1	IN1	Logic Control for Switch 1
2	9	NO1	Normally Open Terminal of Switch 1
3	3	GND	Ground
4	7	NO2	Normally Open Terminal of Switch 2
5	5	IN2	Logic Control Input for Switch 2
6	6	COM2	Common Terminal of Switch 2
7	4	NC2	Normally Closed Terminal of Switch 2
8	8	V+	Input Supply Voltage, +1.8V to +5.5V
9	2	NC1	Normally Closed Terminal of Switch 1
10	10	COM1	Common Terminal of Switch 1

Fast, Low-Voltage, Dual 4Ω SPDT CMOS Analog Switches

MAX4635/MAX4636

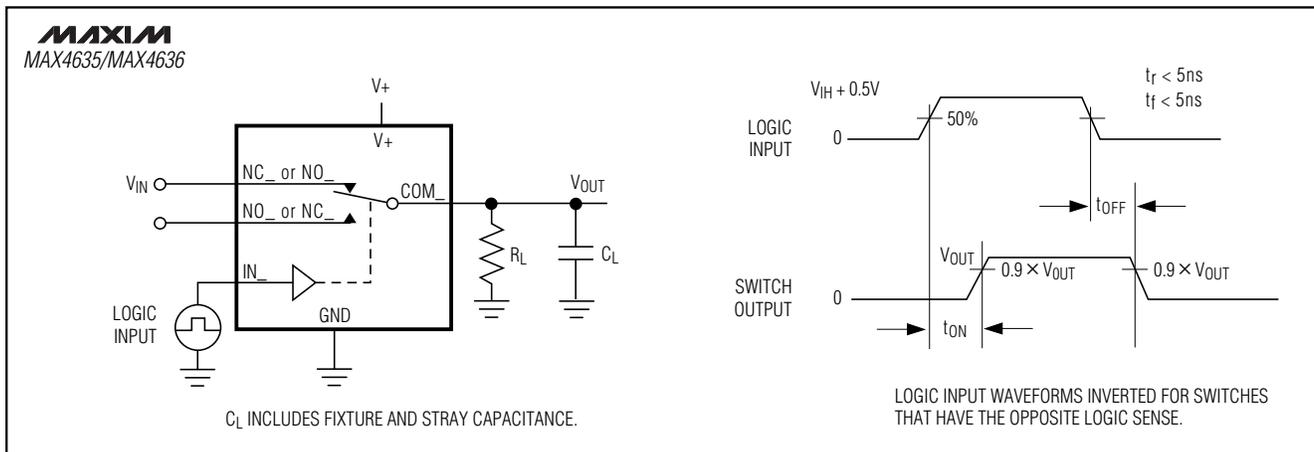


Figure 1a. Switching Time

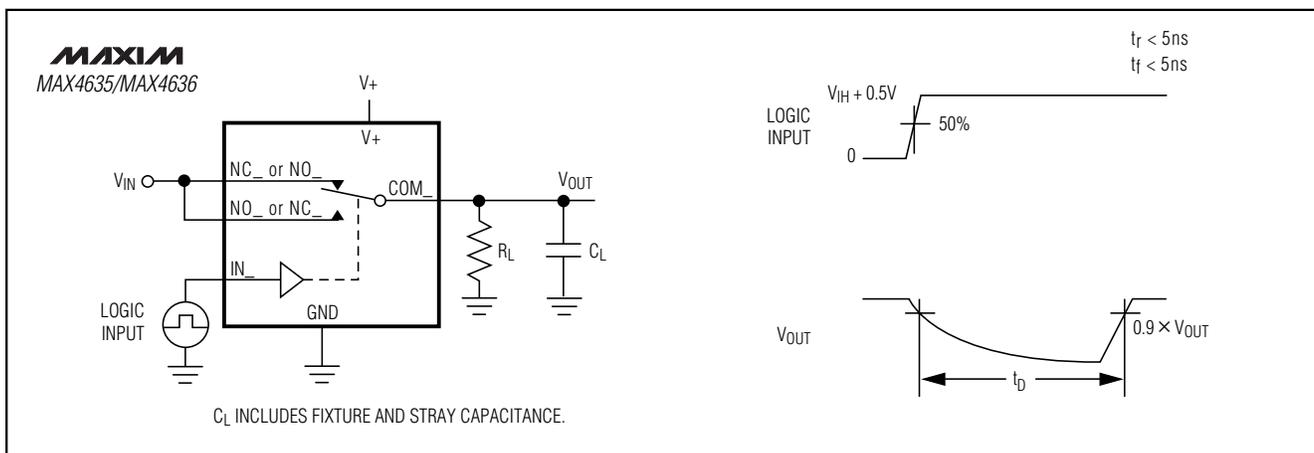


Figure 1b. Break-Before-Make Interval

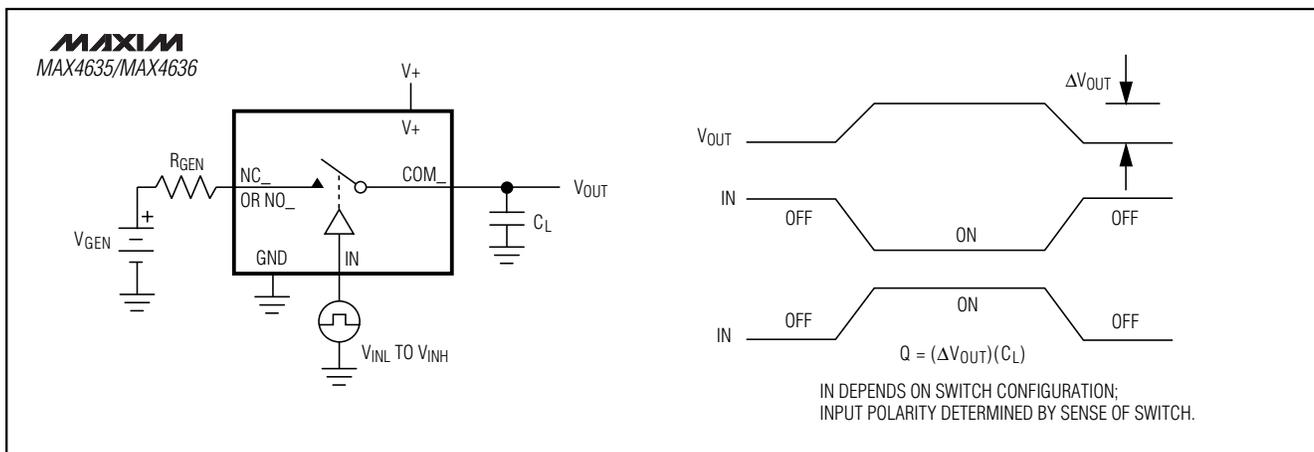


Figure 2. Charge Injection

Fast, Low-Voltage, Dual 4Ω SPDT CMOS Analog Switches

Detailed Description

The MAX4635/MAX4636 are low-on-resistance (R_{ON}), low-voltage, dual SPDT analog switches that operate from a +1.8V to +5.5V supply. The MAX4635/MAX4636 feature very fast switching speed ($t_{ON} = 14\text{ns}$ max, $t_{OFF} = 6\text{ns}$ max) and guaranteed break-before-make switching. The low maximum R_{ON} allows high continuous currents to be switched in a variety of applications.

Applications Information

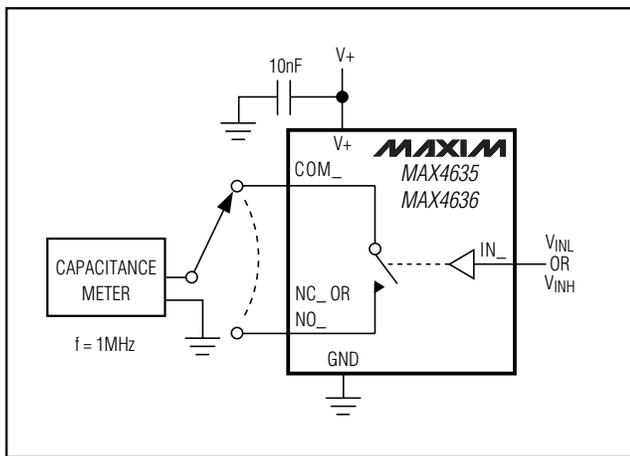


Figure 3. Channel Off/On-Capacitance

Logic Inputs

The MAX4635/MAX4636 logic inputs (IN1, IN2) can be driven up to +5.5V, regardless of the voltage on V+. This allows interfacing to 5V logic signals while operating with a +3.3V supply voltage without external level translation.

Analog Signal Levels

Analog signals ranging over the entire supply voltage ($V+$ to GND) can be passed with very little change in on-resistance (see *Typical Operating Characteristics*). The switches are bidirectional, so the NO_, NC_, and COM_ pins may be used as either inputs or outputs.

Power-Supply Sequencing and Overvoltage Protection

Caution: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the device. Proper power-supply sequencing is recommended for all CMOS devices. Always apply $V+$ before applying analog signals, especially if the analog signal is not current limited. If this sequencing is not possible, and if the analog inputs are not current limited to less than 30mA, add a small-signal diode (D1) as shown in Figure 5. If the analog signal can dip below GND, add D2. Adding protection diodes reduces the analog range to a diode drop (about 0.7V) below $V+$ (for D1), and a diode drop above ground (for D2).

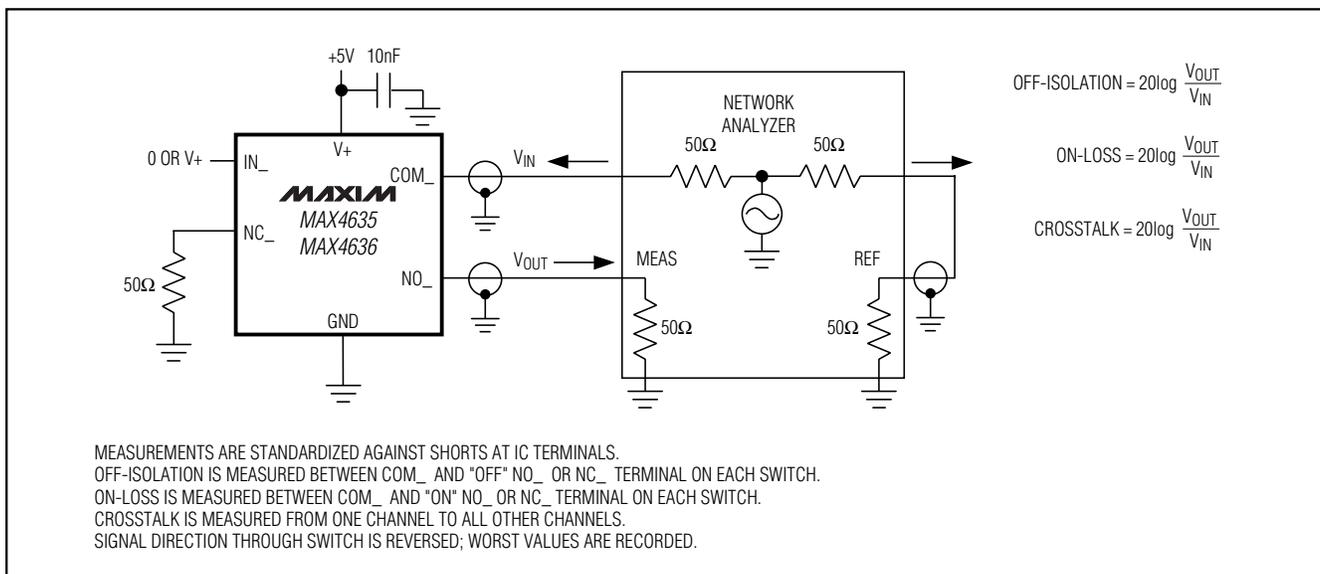


Figure 4. On-Loss, Off-Isolation, and Crosstalk

Fast, Low-Voltage, Dual 4Ω SPDT CMOS Analog Switches

Chip Information

TRANSISTOR COUNT: 239

PROCESS: CMOS

MAX4635/MAX4636

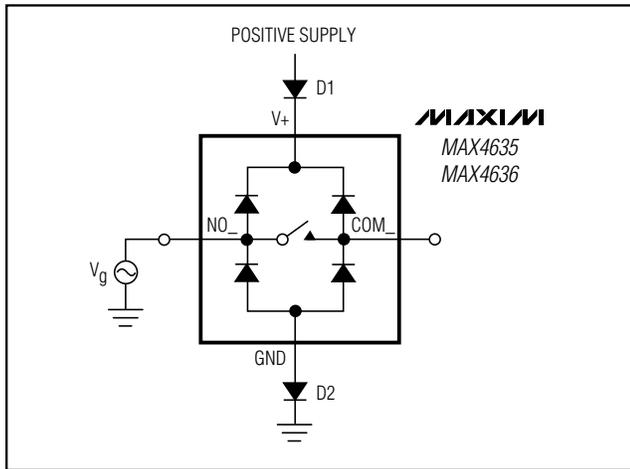


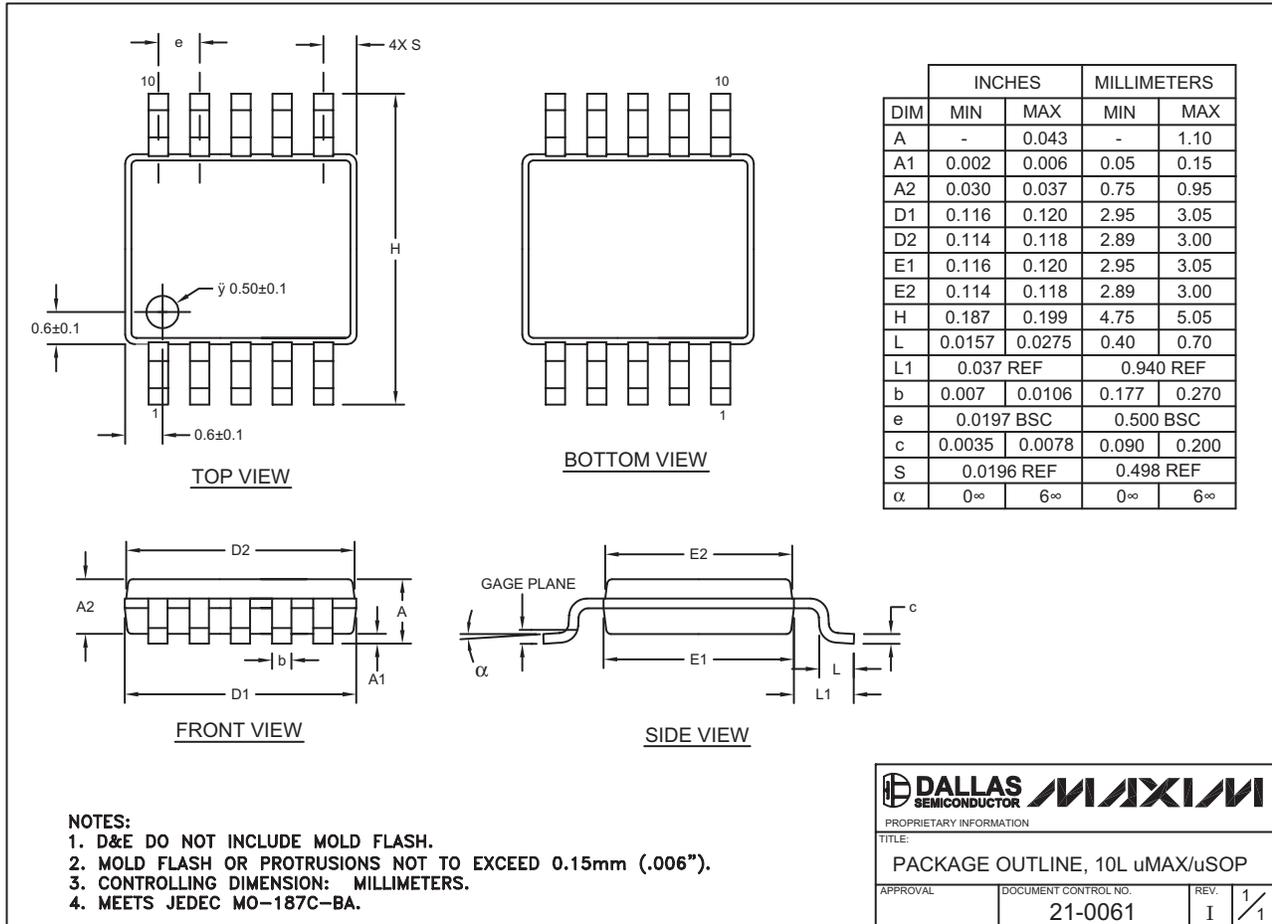
Figure 5. Overvoltage Protection Using Two External Blocking Diodes

On-resistance increases slightly at low supply voltages. Maximum supply voltage ($V+$) must not exceed +6V. Adding protection diode D2 causes the logic threshold to be shifted relative to GND. Protection diodes D1 and D2 also protect against some overvoltage situations. With Figure 5's circuit, if the supply voltage is below the absolute maximum rating, and if a fault voltage up to the absolute maximum rating is applied to an analog signal pin, no damage results.

Fast, Low-Voltage, Dual 4Ω SPDT CMOS Analog Switches

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



10LUMAXEPS

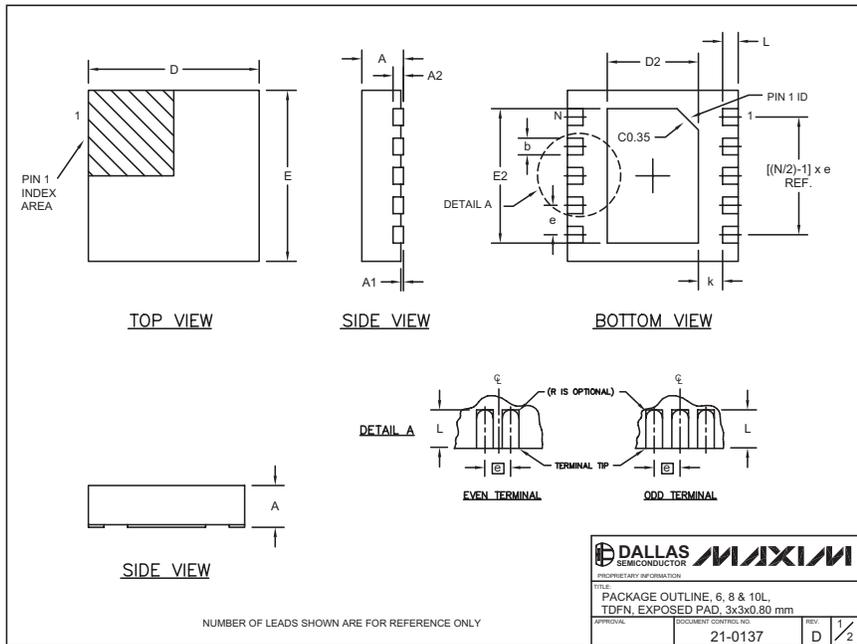
Note: The MAX4636 does not have an exposed pad.

Fast, Low-Voltage, Dual 4Ω SPDT CMOS Analog Switches

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

MAX4635/MAX4636



COMMON DIMENSIONS							
SYMBOL	MIN.	MAX.					
A	0.70	0.80					
D	2.90	3.10					
E	2.90	3.10					
A1	0.00	0.05					
L	0.20	0.40					
k	0.25 MIN.						
A2	0.20 REF.						

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-1	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-1	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF

NOTES:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2".
6. "N" IS THE TOTAL NUMBER OF LEADS.

DALLAS SEMICONDUCTOR		MAXIM	
<small>PROPRIETARY INFORMATION</small>			
<small>TITLE: PACKAGE OUTLINE, 6, 8 & 10L, TDFN, EXPOSED PAD, 3x3x0.80 mm</small>			
<small>APPROVAL</small>	<small>DOCUMENT CONTROL NO.</small>	<small>REV.</small>	<small>2/2</small>
	21-0137	D	2/2

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600 _____ 11