

Conclusion

The MAX17502 successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX17502 high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated MOSFETs operates over a 4.5V to 60V input voltage range. This device is offered in a fixed 3.3V, 5V, or adjustable output voltage (0.9V to 92%VIN) while delivering up to 1A of current. The output voltage is accurate to within $\pm 1.7\%$ over -40°C to $+125^{\circ}\text{C}$. The MAX17502 is available in compact TDFN and TSSOP packages. Simulation models are available.

The device features peak-current-mode control with pulse-width modulation (PWM) and operates with fixed switching frequency at any load. The low-resistance, on-chip MOSFETs ensure high efficiency at full load and simplify the layout.

A programmable soft-start feature allows users to reduce input inrush current. The device also incorporates an output enable/undervoltage lockout pin (EN/UVLO) that allows the user to turn on the part at the desired input-voltage level. An open-drain active-low RESET pin provides a delayed power-good signal to the system upon achieving successful regulation of the output voltage.

II. Manufacturing Information

A. Description/Function:	60V, 1A, Ultra-Small, High-Efficiency, Synchronous Step-Down DC-DC Converter
B. Process:	S18
C. Number of Device Transistors:	14609
D. Fabrication Location:	Japan, USA
E. Assembly Location:	Taiwan, Thailand
F. Date of Initial Production:	March 22, 2012

III. Packaging Information

A. Package Type:	10-pin TDFN
B. Lead Frame:	Copper
C. Lead Finish:	NiPdAu
D. Die Attach:	Non-conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4357
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	87.5°C/W
K. Single Layer Theta Jc:	18.2°C/W
L. Multi Layer Theta Ja:	67.3°C/W
M. Multi Layer Theta Jc:	18.2°C/W

IV. Die Information

A. Dimensions:	40.9449X103.937 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Eric Wright (Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 78 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 14.1 \times 10^{-9}$$

$$\lambda = 14.1 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25C and 0.93 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The PI01-0 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM: +/- 2500V per JEDEC JESD22-A114

ESD-CDM: +/- 750V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX17502

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135C	DC Parameters & functionality	78	0	
	Biased				
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.