# Specifications

## **Absolute Maximum Ratings** at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>CC</sub> max	V <sub>CC</sub>	5.5	V
Maximum pin voltage1	V1 max	SW	43	V
Maximum pin voltage2	V2 max	Other pin	5.5	V
Allowable power dissipation	Pd max	Ta = 25°C *1	1.30	W
Operating temperature	Topr		-30 to +85	°C
Storage temperature	Tstg		–55 to +125	°C

\*1 Mounted on a specified board: 70mm×70mm×1.2mm (4 layer glass epoxy)

Caution 1) Absolute maximum ratings represent the values which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

### **Recommendation Operating Condition** at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range1	V <sub>CC</sub> op	V <sub>CC</sub>	2.7 to 5.5	V
PWM frequency	Fpwm	PWM MODE	300 to 100k	Hz

### Electrical Characteristics Analog block at Ta = 25°C, V<sub>CC</sub> = 3.6V, unless otherwise specified

Description	0 mbal	0		Ratings		Unit	
Parameter	Symbol	Conditions	min	typ	max	Unit	
Standby current dissipation	ICC1	SHUTDOWN		0	5	μA	
DC/DC current dissipation 1	ICC2	V <sub>OUT</sub> = 30V, I <sub>LED</sub> = 20mA		1		mA	
FB voltage	Vfb	LEDO1,2=20mA		0.25		V	
Output current 1	lo1	LEDO 1 LEDO 2	9.5	10	10.5	μA	
Output current 2	lo2	LEDO 1 LEDO 2	19	20	21	μA	
Output current matching 1	lom1	LEDO1 LEDO 2 LEDISET=10mA	-2	0.3	2	%	
Output current matching 2	lom2	LEDO1 LEDO 2 LEDISET=20mA	-2	0.3	2	%	
LEDO1,2 leak current	llk	LEDO1 LEDO2			1	μA	
OVP voltage 1	Vovp	OVP	37	38	39	V	
SWOUT ON resistance	Ron	IL = 100mA		250		mΩ	
NMOS switch current limit	ILIM			1		А	
OSC frequency	Fosc			600		kHz	
High level input voltage	V <sub>IN</sub> H	SWIRE PWM	1.5		V <sub>CC</sub>	V	
Low level input voltage	VINL	SWIRE PWM	0		0.4	V	
Under voltage lockout	Vuvlo	V <sub>IN</sub> falling		2.2		V	
SWIRE output voltage for Acknowledge	Vack	Rpullup = 15kΩ			0.4	V	

### **Recommended SWIRE Timing** at Ta = $25^{\circ}$ C, V<sub>CC</sub> = 3.6V, unless otherwise specified

Devenuetor	Ourseland	mbol Conditions		Unit		
Parameter	Symbol	Symbol Conditions		typ	max	Unit
SWIRE setup time	Ton		20			μs
from shutdown						
SWIRE mode selectable time	Tsel		1		2.2	ms
SWIRE delay time to start	Tw0		100			μs
digital mode detection						
SWIRE low time to switch to	Tw1		260			μs
digital mode						
SWIRE low time to shutdown	Toff		8.9			ms

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Describer	0 set et			Ratings		11.1
Parameter	Symbol	Conditions	min	typ	max	Unit
SWIRE start time for digital mode programming	Tstart		2			μS
SWIRE end time for digital mode programming	Tend		2		360	μS
SWIRE High time of bit 0	Th0	Bit detection = 0	2		180	μS
SWIRE Low time of bit 0	TIO	Bit detection = 0	$Th0 \times 2$		360	μS
SWIRE High time of bit 1	Th1	Bit detection = 1	$TI1 \times 2$		360	μS
SWIRE Low time of bit1	TI1	Bit detection = 1	2		180	μS
DCDC startup delay	Tdel			2		ms
Delay time of Acknowledge	Tackd				2	μS
Duration of Acknowledge	Tack				512	μS

## **Block Diagram**



L1: VL3012T-220M49 (TDK) VLS3012T-100M72 (TDK)

D1: MBR0540T1 (ON semi)

C2: GRM21BR71H105K (Murata)

Fig.2 Block Diagram

## LV52206XA

Pin Functio	n	
PIN #	Pin Name	Description
A1	LEDO1	Constant current output _pin1.
A2	FCAP	Filtering capacitor terminal for PWM mode.
A3	VCC	Supply voltage
B1	LEDO2	Constant current output _pin2.
B2	PWM / SWIRE	1-wire control and PWM dimming input (active High).
B3	OVP	Output voltage sense connection for over voltage sensing.
C1	GND	Ground.
C2	GND	Ground.
C3	SW	Switch pin. Drain of the internal power FET.



### **Dimming Mode Selection**

Dimming Mode is selected by a specific pattern of the SWIRE within Tsel (1ms) from the startup of the device every time. In order to startup the device, the SWIRE must keep high for longer than Ton.

#### PWM Mode

The dimming mode is set to PWM mode when it is not recognized as a digital mode within Tsel. To enter Digital Mode, the SWIRE is required keeping in low state for Tw1 (See Fig.4). If the PWM frequency is used faster than 6.6kHz, the dimming mode is set to PWM mode only. But slower than 6.6kHz, it is necessary to avoid entering the digital mode condition, such as SWIRE keeps high for longer than Tsel. PWM is enabled after Tdel from Tsel.





### **Digital Mode**

To enter Digital Mode, SWIRE should be taken high for more than Tw0 ( $100\mu$ s) from the first rising edge and keep low state for Tw1( $260\mu$ s) before Tsel(1ms).



Fig4. SWIRE Timing Diagram in Digital mode

It is required sending the device address byte and the data byte to select  $V_{FB}$ . The bit detection is determined by the ratio of Th and Tl (See Fig6). The start condition for the bit transmission required SWIRE high for at least Tstart. The end condition is required SWIRE low for at least Tend. When data is not being transferred, SWIRE is set in the "H" state. These registers are initialized with POR (Power On Reset).

In the LV52206XA, the device address(DA7 to DA0) is specified as "01110011". AKct is setting for the acknowledge response. If the device address and the data byte are transferred on AKct=1, the ACK signal is sent from the receive side to the send side. The acknowledge signal is issued when SWIRE on the send side is released and SWIRE on the receive side is set to low state.

	Register	BIT	Description
	DA7	7	0
	DA6	6	1
	DA5	5	1
Device	DA4	4	1
Address	DA3	3	0
	DA2	2	0
ĺ	DA1	1	1
	DA0	0	1

Table1. Device Address Description

	Register	BIT	Description
	AKct 7		0 = Acknowledge disabled
	ARCI	'	1 = Acknowledge enabled
	A1	6	Address bit1
	A0	5	Address bit0
Data	Data D4		Data bit 4
	D3	3	Data bit 3
	D2	2	Data bit 2
	D1	1	Data bit 1
	D0	0	Data bit 0

Table2. Data Description



Fig5. Example of writing data





## Table3

## LED Current setting Address=00

	A1	A0	D4	D3	D2	D1	D0	LED Current(mA)	
0	0	0	0	0	0	0	0	0	
1	0	0	0	0	0	0	1	0.5	
2	0	0	0	0	0	1	0	1	
3	0	0	0	0	0	1	1	1.5	
4	0	0	0	0	1	0	0	2	
5	0	0	0	0	1	0	1	2.5	
6	0	0	0	0	1	1	0	3	
7	0	0	0	0	1	1	1	3.5	
8	0	0	0	1	0	0	0	4	
9	0	0	0	1	0	0	1	5	
10	0	0	0	1	0	1	0	6	
11	0	0	0	1	0	1	1	7	
12	0	0	0	1	1	0	0	8	
13	0	0	0	1	1	0	1	9	
14	0	0	0	1	1	1	0	10	
15	0	0	0	1	1	1	1	11	
16	0	0	1	0	0	0	0	12	
17	0	0	1	0	0	0	1	13	
18	0	0	1	0	0	1	0	14	
19	0	0	1	0	0	1	1	15	
20	0	0	1	0	1	0	0	16	
21	0	0	1	0	1	0	1	17	
22	0	0	1	0	1	1	0	18	
23	0	0	1	0	1	1	1	19	
24	0	0	1	1	0	0	0	20	*Default
25	0	0	1	1	0	0	1	21	
26	0	0	1	1	0	1	0	22	
27	0	0	1	1	0	1	1	23	
28	0	0	1	1	1	0	0	24	
29	0	0	1	1	1	0	1	25	
30	0	0	1	1	1	1	0	26	
31	0	0	1	1	1	1	1	27	

### Table4

OVP setting Address=01

A1	A0	D4	D3	D2	D1	D0	OVP(V)	
0	1	0	0	0	0	0	38	*Default
0	1	0	0	0	0	1	41	

## Table5

LEDOUT setting Adress=10

A1	A0	D4	D3	D2	D1	D0	LEDO1	LEDO2	
1	0	0	0	0	0	0	ON	ON	*Default
1	0	0	0	0	0	1	ON	OFF	
1	0	0	0	0	1	0	OFF	ON	

### Start up and Shutdown

The device becomes enabled when SWIRE is initially taken high. The dimming mode is determined within Tsel and the boost converter start up after Tdel. To place the device into shutdown mode, the SWIRE must be held low for Toff.

### PWM MODE



### Digital MODE



Fig7.Start up and shutdown diagram

## **Open LED Protection**

If OVP terminal voltage exceeds a threshold Vovp (38V typ) and LEDO terminal voltage less than 0.05V for 8 cycles, boost converter enters shutdown mode. In order to restart the IC, It is necessary to start it again from a shut down condition.

### **Over Current Protection**

Current limit value for built-in power MOS is around 1A. The power MOS is turned off for each switching cycle when peak current through it exceeds the limit value.

### Under Voltage Lock Out (UVLO)

UVLO operation works when VIN terminal voltage is below 2.2V.

#### **Thermal Shutdown**

When chip temperature is too high, boost converter is stopped.

### **Application Circuit Diagram**



L1:VLS3012E-220M(TDK), VLF504015MT-220M (TDK) D1:MBR0540T1 (ON semi), NSR05F40 (ONsemi) C2:GRM21BR71H105K(Murata), C1608X5R1H105K (TDK)

Fig8. Various application circuit diagram

## LV52206XA

## **Typical Characteristics** ( $V_{IN} = 3.6V$ , $L = 22\mu$ H, T = 25°C, unless otherwise specified)

Efficiency vs Output Current

MODE=Digital



<u>LEDO Current vs. DATA</u> Mode=Digital, LEDO1.LEDO2=0.5V





Icc vs VIN MODE=PWM, Duty=100% 10LED, 2 1.6 (Techarian 1.2 Icc(ma) 0.8 0.4 0 4 VIN(V) 2

3

Frequency vs VIN

6

5



### PACKAGE DIMENSIONS

WLP9(1.19X1.19) unit : mm



## **ORDERING INFORMATION**

Device	Package	Shipping (Qty / Packing)
LV52206XA-MH	WLP9 (1.19x1.19) (Pb-Free)	5000 / Tape & Reel

0,08±0,05

\_\_\_\_0.08 S

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