Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max	V_{CC}	5.5	V
Maximum pin voltage1	V1 max	SW	43	V
Maximum pin voltage2	V2 max	Other pin	5.5	V
Allowable power dissipation	Pd max	Ta = 25°C *1	1.30	W
Operating temperature	Topr		–30 to +85	°C
Storage temperature	Tstg		–55 to +125	°C

*1 Mounted on a specified board: 70mm×70mm×1.2mm (4 layer glass epoxy)

Caution 1) Absolute maximum ratings represent the values which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommendation Operating Condition at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range1	V_{CC} op	V_{CC}	2.7 to 5.5	V
PWM frequency	Fpwm	PWM MODE	300 to 100k	Hz

Electrical Characteristics Analog block at Ta = 25°C, V_{CC} = 3.6V, unless otherwise specified

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Standby current dissipation	$I_{CC}1$	SHUTDOWN		0	5	μA
DC/DC current dissipation 1	$I_{CC}2$	V_{OUT} = 30V, I_{LED} = 20mA		1		mA
FB voltage	Vfb	LEDO1,2=20mA		0.25		V
Output current 1	Io1	LEDO 1 LEDO 2	9.5	10	10.5	μA
Output current 2	Io2	LEDO 1 LEDO 2	19	20	21	μA
Output current matching 1	Iom1	LEDO1 LEDO 2 LEDISET=10mA	–2	0.3	2	%
Output current matching 2	Iom2	LEDO1 LEDO 2 LEDISET=20mA	–2	0.3	2	%
LEDO1,2 leak current	Ilk	LEDO1 LEDO2			1	μA
OVP voltage 1	Vovp	OVP	37	38	39	V
SWOUT ON resistance	Ron	IL = 100mA		250		mΩ
NMOS switch current limit	ILIM			1		A
OSC frequency	Fosc			600		kHz
High level input voltage	$V_{IN}H$	SWIRE PWM	1.5		V_{CC}	V
Low level input voltage	$V_{IN}L$	SWIRE PWM	0		0.4	V
Under voltage lockout	Vuvlo	V_{IN} falling		2.2		V
SWIRE output voltage for Acknowledge	Vack	Rpullup = 15kΩ			0.4	V

Recommended SWIRE Timing at Ta = 25°C, V_{CC} = 3.6V, unless otherwise specified

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
SWIRE setup time from shutdown	Ton		20			μs
SWIRE mode selectable time	Tsel		1		2.2	ms
SWIRE delay time to start digital mode detection	Tw0		100			μs
SWIRE low time to switch to digital mode	Tw1		260			μs
SWIRE low time to shutdown	Toff		8.9			ms

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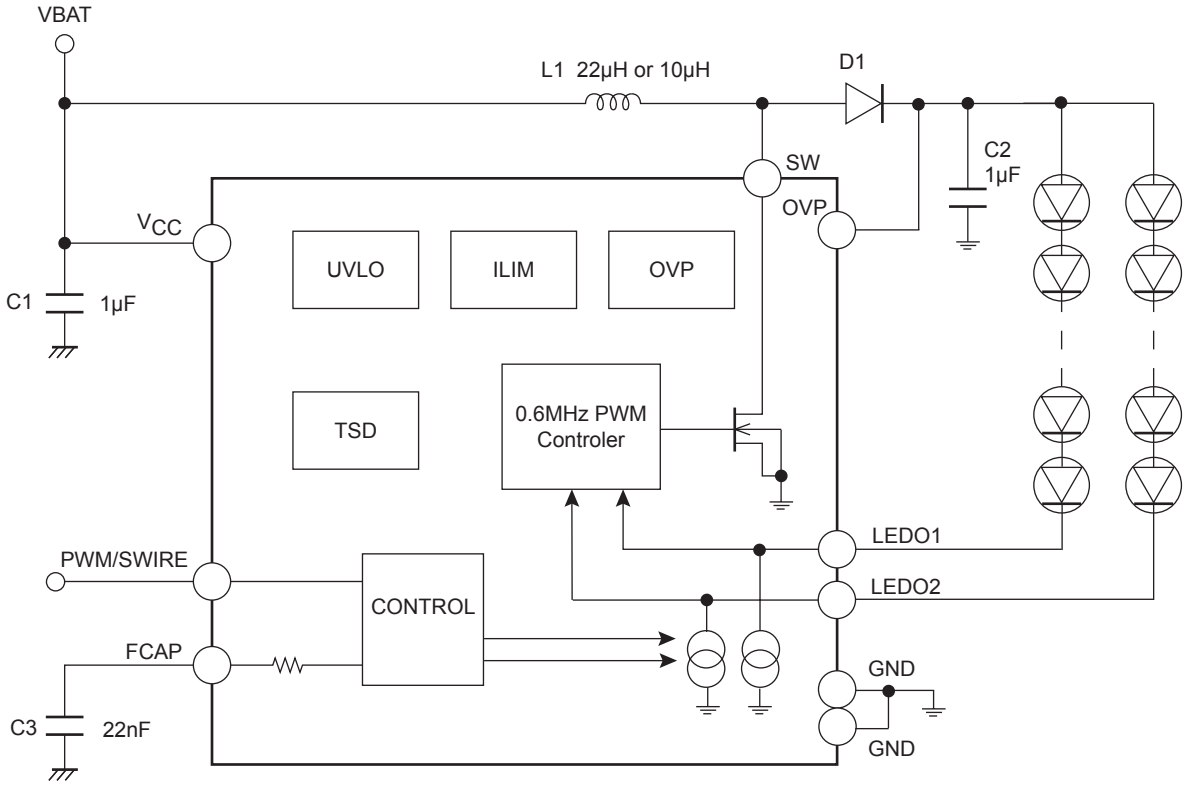
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
SWIRE start time for digital mode programming	Tstart		2			µs
SWIRE end time for digital mode programming	Tend		2		360	µs
SWIRE High time of bit 0	Th0	Bit detection = 0	2		180	µs
SWIRE Low time of bit 0	Tl0	Bit detection = 0	Th0 × 2		360	µs
SWIRE High time of bit 1	Th1	Bit detection = 1	Tl1 × 2		360	µs
SWIRE Low time of bit1	Tl1	Bit detection = 1	2		180	µs
DCDC startup delay	Tdel			2		ms
Delay time of Acknowledge	Tackd				2	µs
Duration of Acknowledge	Tack				512	µs

Block Diagram

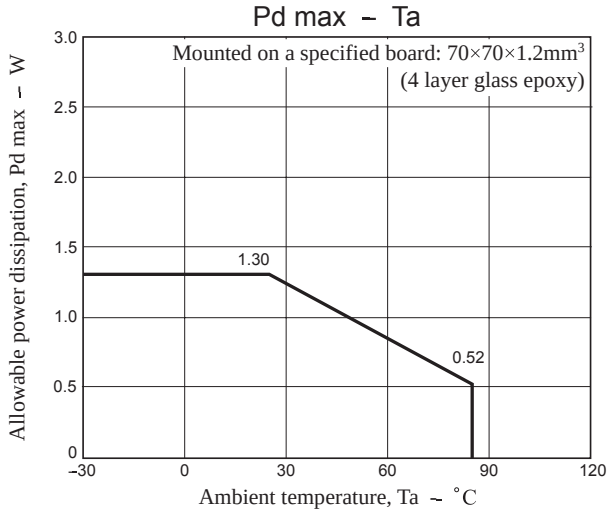


L1: VL3012T-220M49 (TDK) VLS3012T-100M72 (TDK)
D1: MBR0540T1 (ON semi)
C2: GRM21BR71H105K (Murata)

Fig.2 Block Diagram

Pin Function

PIN #	Pin Name	Description
A1	LEDO1	Constant current output _pin1.
A2	FCAP	Filtering capacitor terminal for PWM mode.
A3	VCC	Supply voltage
B1	LEDO2	Constant current output _pin2.
B2	PWM / SWIRE	1-wire control and PWM dimming input (active High).
B3	OVP	Output voltage sense connection for over voltage sensing.
C1	GND	Ground.
C2	GND	Ground.
C3	SW	Switch pin. Drain of the internal power FET.



Dimming Mode Selection

Dimming Mode is selected by a specific pattern of the SWIRE within Tsel (1ms) from the startup of the device every time. In order to startup the device, the SWIRE must keep high for longer than Ton.

PWM Mode

The dimming mode is set to PWM mode when it is not recognized as a digital mode within Tsel. To enter Digital Mode, the SWIRE is required keeping in low state for Tw1 (See Fig.4). If the PWM frequency is used faster than 6.6kHz, the dimming mode is set to PWM mode only. But slower than 6.6kHz, it is necessary to avoid entering the digital mode condition, such as SWIRE keeps high for longer than Tsel. PWM is enabled after Tdel from Tsel.

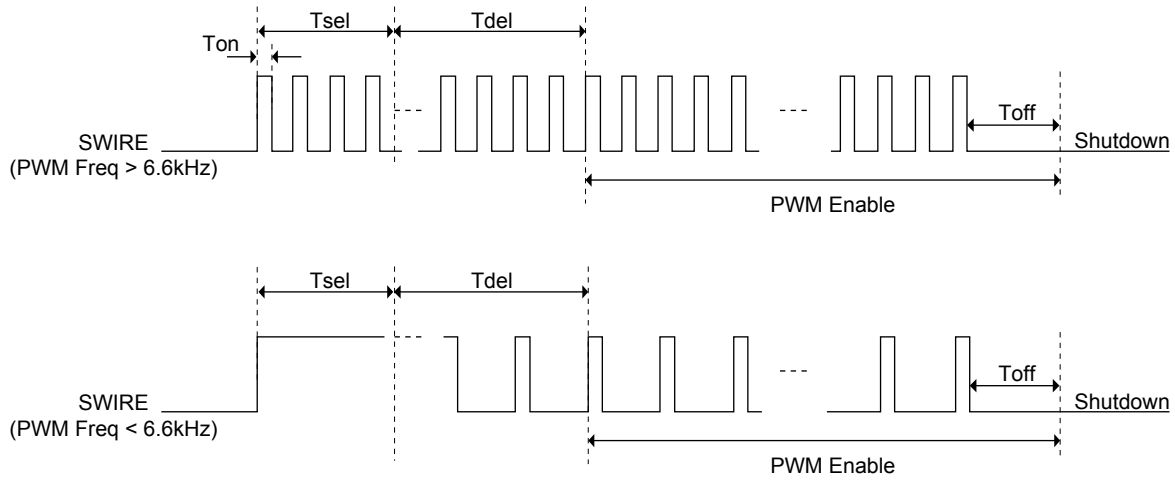


Fig3. SWIRE Timing Diagram in PWM mode

Digital Mode

To enter Digital Mode, SWIRE should be taken high for more than Tw0 (100μs) from the first rising edge and keep low state for Tw1(260μs) before Tsel(1ms).

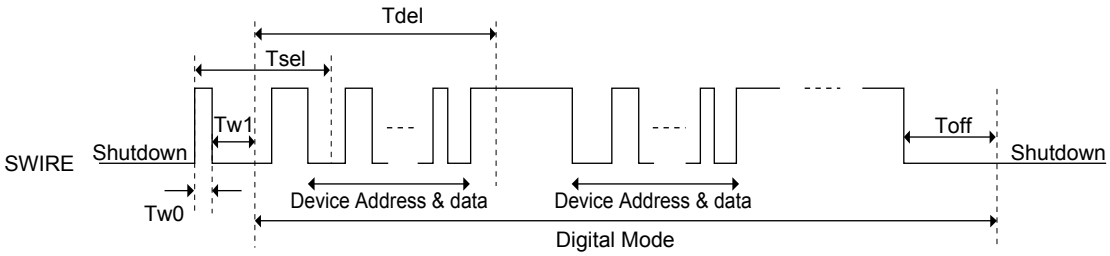


Fig4. SWIRE Timing Diagram in Digital mode

It is required sending the device address byte and the data byte to select V_{FB}. The bit detection is determined by the ratio of Th and Tl (See Fig6). The start condition for the bit transmission required SWIRE high for at least Tstart. The end condition is required SWIRE low for at least Tend. When data is not being transferred, SWIRE is set in the "H" state. These registers are initialized with POR (Power On Reset).
In the LV52206XA, the device address(DA7 to DA0) is specified as "01110011". AKct is setting for the acknowledge response. If the device address and the data byte are transferred on AKct=1, the ACK signal is sent from the receive side to the send side. The acknowledge signal is issued when SWIRE on the send side is released and SWIRE on the receive side is set to low state.

	Register	BIT	Description
Device Address	DA7	7	0
	DA6	6	1
	DA5	5	1
	DA4	4	1
	DA3	3	0
	DA2	2	0
	DA1	1	1
	DA0	0	1

Table1. Device Address Description

	Register	BIT	Description
Data	AKct	7	0 = Acknowledge disabled 1 = Acknowledge enabled
	A1	6	Address bit1
	A0	5	Address bit0
	D4	4	Data bit 4
	D3	3	Data bit 3
	D2	2	Data bit 2
	D1	1	Data bit 1
	D0	0	Data bit 0

Table2. Data Description

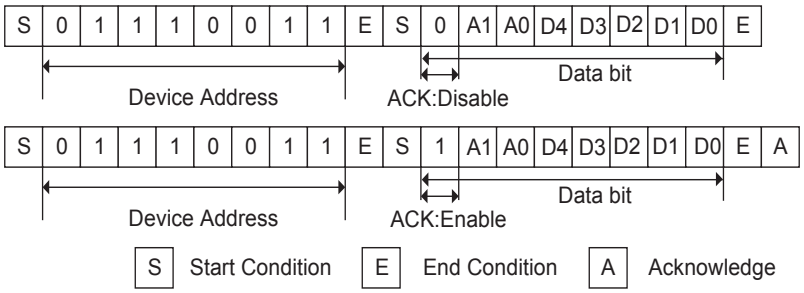


Fig5. Example of writing data

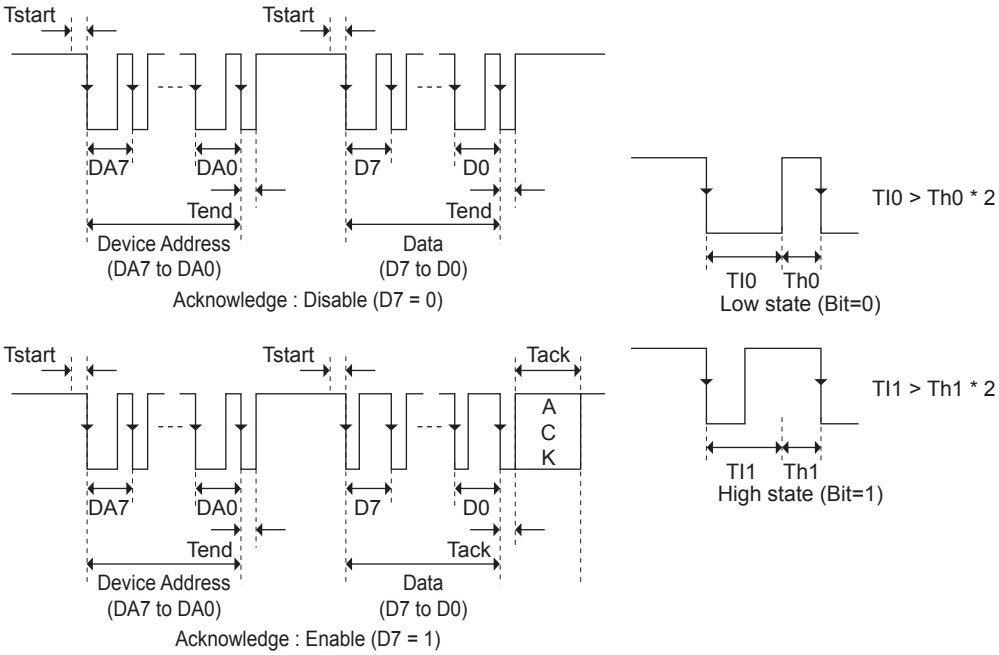


Fig6.Bit detection Diagram

Table3

LED Current setting Address=00

	A1	A0	D4	D3	D2	D1	D0	LED Current(mA)	
0	0	0	0	0	0	0	0	0	
1	0	0	0	0	0	0	1	0.5	
2	0	0	0	0	0	1	0	1	
3	0	0	0	0	0	1	1	1.5	
4	0	0	0	0	1	0	0	2	
5	0	0	0	0	1	0	1	2.5	
6	0	0	0	0	1	1	0	3	
7	0	0	0	0	1	1	1	3.5	
8	0	0	0	1	0	0	0	4	
9	0	0	0	1	0	0	1	5	
10	0	0	0	1	0	1	0	6	
11	0	0	0	1	0	1	1	7	
12	0	0	0	1	1	0	0	8	
13	0	0	0	1	1	0	1	9	
14	0	0	0	1	1	1	0	10	
15	0	0	0	1	1	1	1	11	
16	0	0	1	0	0	0	0	12	
17	0	0	1	0	0	0	1	13	
18	0	0	1	0	0	1	0	14	
19	0	0	1	0	0	1	1	15	
20	0	0	1	0	1	0	0	16	
21	0	0	1	0	1	0	1	17	
22	0	0	1	0	1	1	0	18	
23	0	0	1	0	1	1	1	19	
24	0	0	1	1	0	0	0	20	*Default
25	0	0	1	1	0	0	1	21	
26	0	0	1	1	0	1	0	22	
27	0	0	1	1	0	1	1	23	
28	0	0	1	1	1	0	0	24	
29	0	0	1	1	1	0	1	25	
30	0	0	1	1	1	1	0	26	
31	0	0	1	1	1	1	1	27	

Table4

OVP setting Address=01

A1	A0	D4	D3	D2	D1	D0	OVP(V)	
0	1	0	0	0	0	0	38	*Default
0	1	0	0	0	0	1	41	

Table5

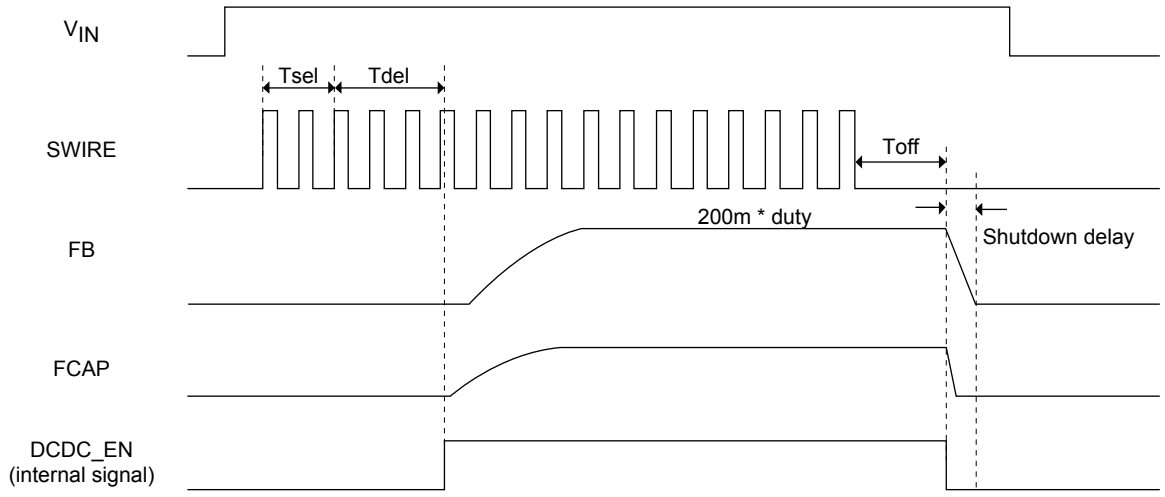
LEDOUT setting Adress=10

A1	A0	D4	D3	D2	D1	D0	LEDO1	LEDO2	
1	0	0	0	0	0	0	ON	ON	*Default
1	0	0	0	0	0	1	ON	OFF	
1	0	0	0	0	1	0	OFF	ON	

Start up and Shutdown

The device becomes enabled when SWIRE is initially taken high. The dimming mode is determined within Tsel and the boost converter start up after Tdel. To place the device into shutdown mode, the SWIRE must be held low for Toff.

PWM MODE



Digital MODE

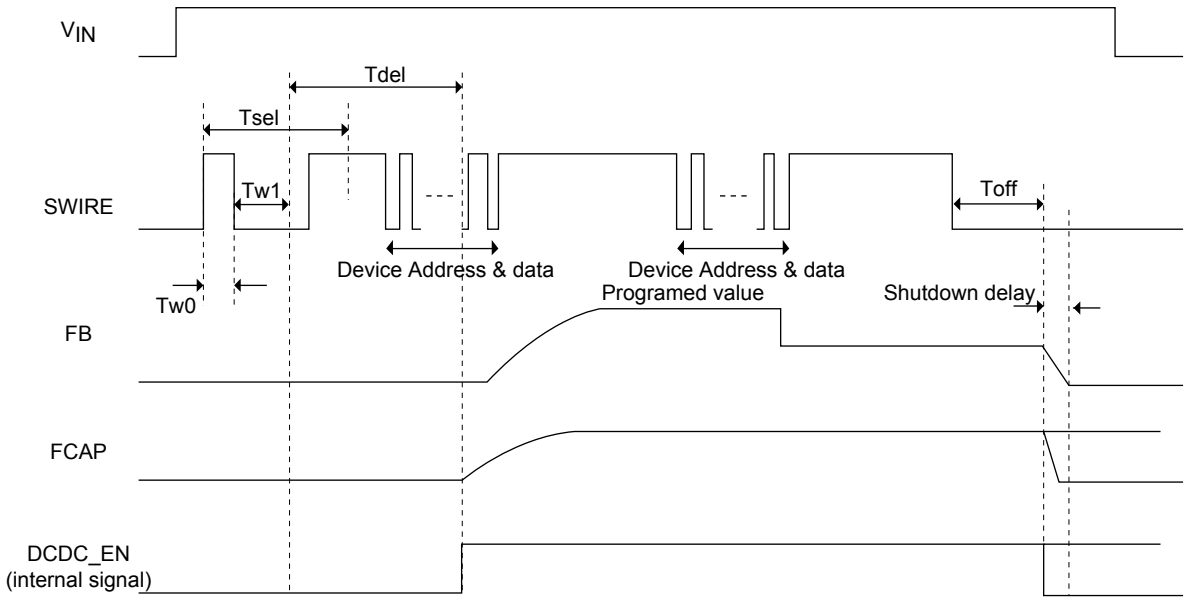


Fig7.Start up and shutdown diagram

Open LED Protection

If OVP terminal voltage exceeds a threshold Vovp (38V typ) and LEDO terminal voltage less than 0.05V for 8 cycles, boost converter enters shutdown mode. In order to restart the IC, It is necessary to start it again from a shut down condition.

Over Current Protection

Current limit value for built-in power MOS is around 1A. The power MOS is turned off for each switching cycle when peak current through it exceeds the limit value.

Under Voltage Lock Out (UVLO)

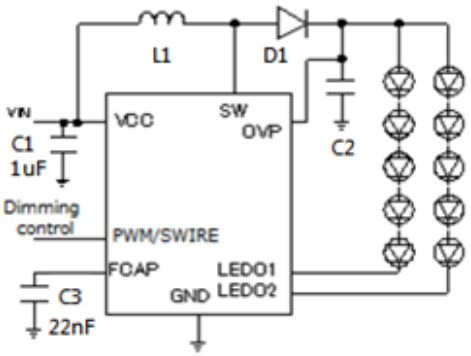
UVLO operation works when V_{IN} terminal voltage is below 2.2V.

Thermal Shutdown

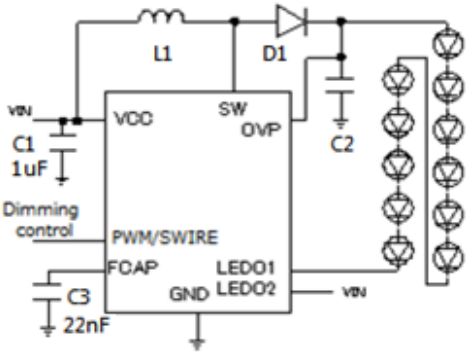
When chip temperature is too high, boost converter is stopped.

Application Circuit Diagram

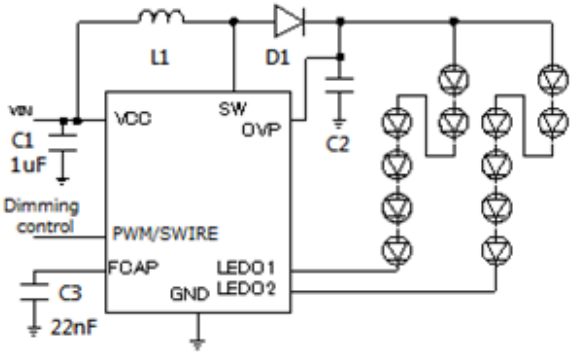
10 LED Application
5x2



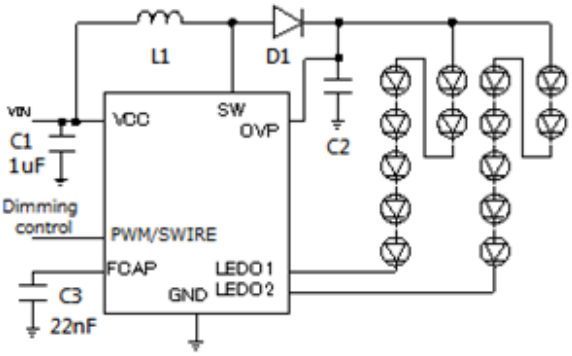
11 LED Application
11x1



12 LED Application
6x2



14 LED Application
7x2



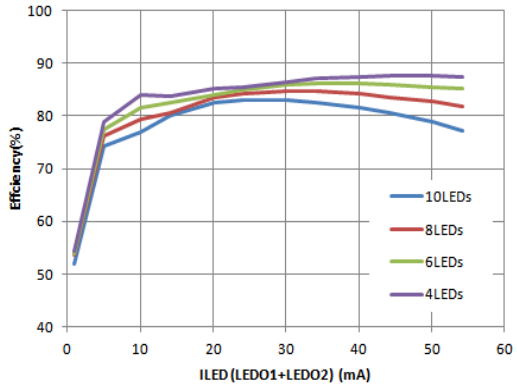
L1:VLS3012E-220M(TDK), VLF504015MT-220M (TDK)
D1:MBR0540T1 (ON semi), NSR05F40 (ONsemi)
C2:GRM21BR71H105K(Murata), C1608X5R1H105K (TDK)

Fig8. Various application circuit diagram

Typical Characteristics (V_{IN} = 3.6V, L = 22μH, T = 25°C, unless otherwise specified)

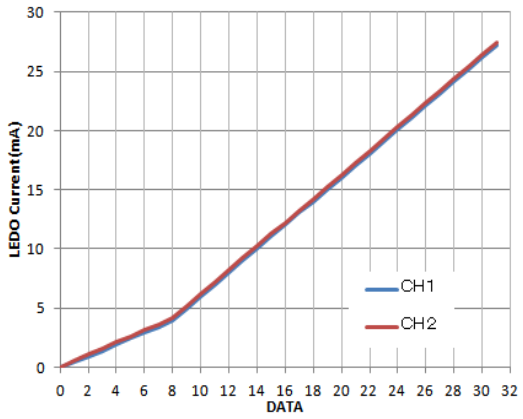
Efficiency vs Output Current

MODE=Digital



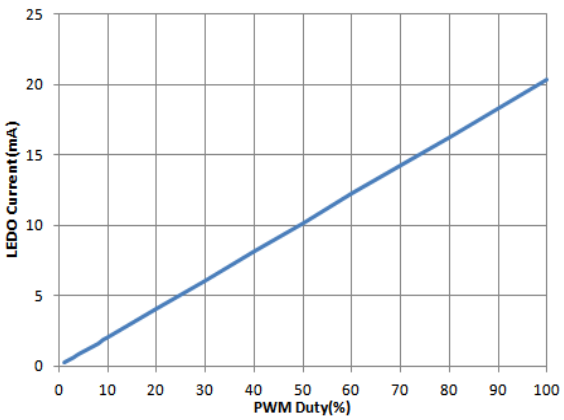
LEDO Current vs. DATA

Mode=Digital, LEDO1.LEDO2=0.5V



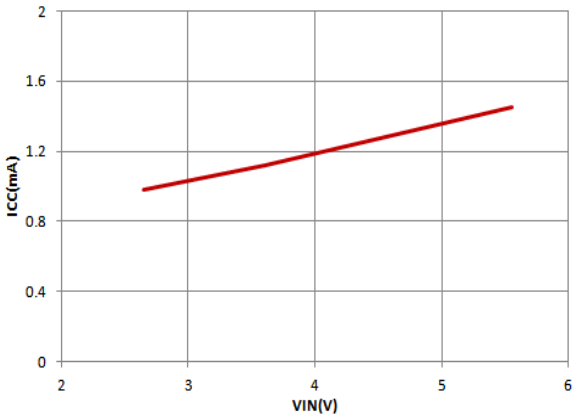
LEDO Current vs. PWM Duty

Mode=PWM, 10kHz, LEDO1.LEDO2=0.5V

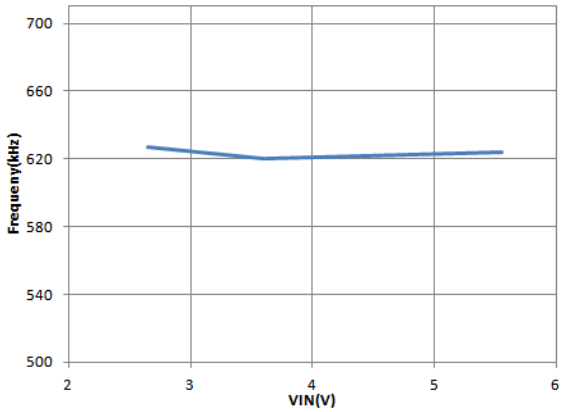


Icc vs VIN

MODE=PWM, Duty=100% 10LED,

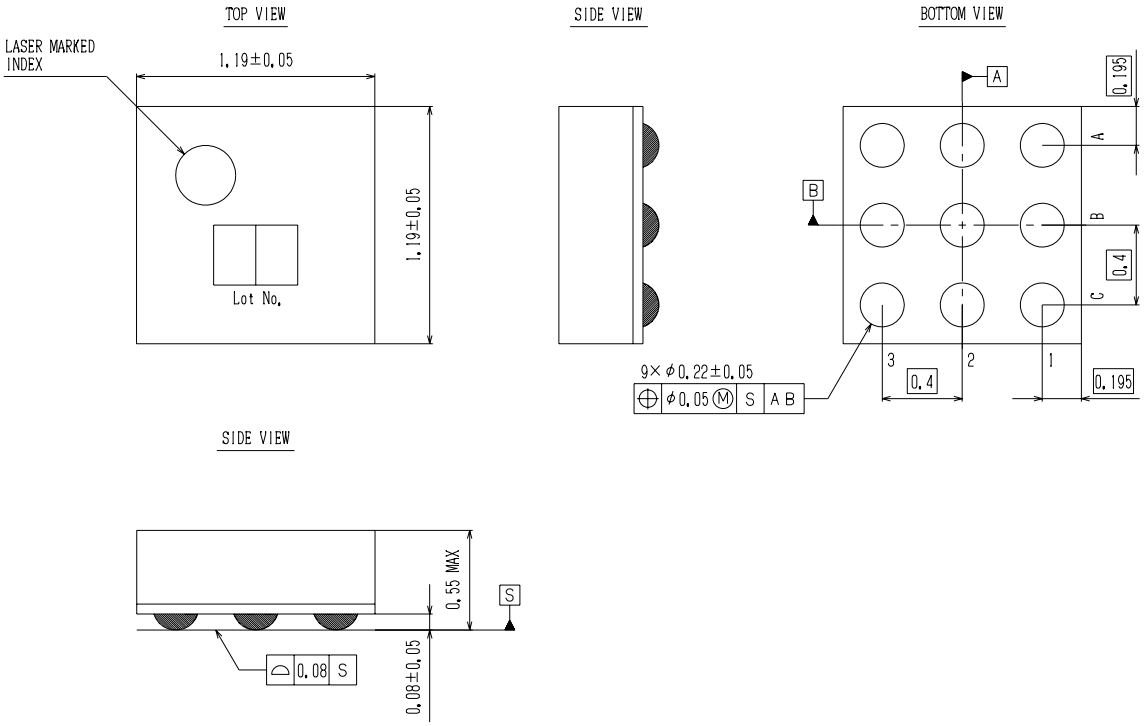


Frequency vs VIN



PACKAGE DIMENSIONS

WLP9(1.19X1.19)
unit : mm



ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LV52206XA-MH	WLP9 (1.19x1.19) (Pb-Free)	5000 / Tape & Reel