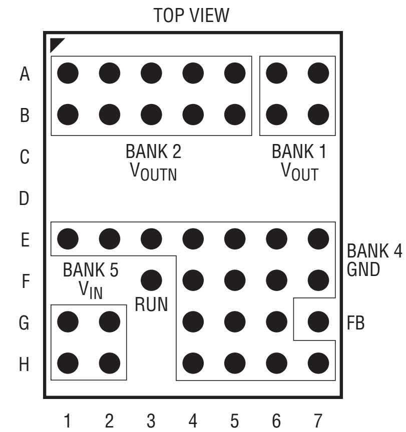
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, RUN, BIAS 42V
V_{OUT} Relative to V_{OUTN} 25V
V_{IN} + V_{OUT} (Note 2)..48V
GND to V_{OUT}^{-} Isolation (Note 3) 2kVAC
Maximum Internal Temperature (Note 4) .... 125°C
Peak Solder Reflow Body Temperature .... 245°C
Storage Temperature.............................. –55°C to 125°C

PIN CONFIGURATION



BGA PACKAGE
38-LEAD (11.25mm × 9mm × 4.92mm)
T_{JMAX} = 125°C, θ_{JA} = 20.8°C/W, $\theta_{JCbottom}$ = 5.1°C/W, θ_{JCtop} = 18.4°C/W, θ_{JB} = 5.3°C/W
WEIGHT = 1.1g, θ VALUES DETERMINED PER JEDEC 51-9, 51-12

ORDER INFORMATION http://www.linear.com/product/LTM8067#orderinfo

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 4)
		DEVICE	CODE			
LTM8067EY#PBF	SAC305 (RoHS)	LTM8067Y	e1	BGA	3	–40°C to 125°C
LTM8067IY#PBF	SAC305 (RoHS)	LTM8067Y	e1	BGA	3	–40°C to 125°C
LTM8067IY	SnPb (63/37)	LTM8067Y	e0	BGA	3	–40°C to 125°C

Consult Marketing for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

- Terminal Finish Part Marking:
  www.linear.com/leadfree
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures:
  www.linear.com/umodule/pcbassembly
- LGA and BGA Package and Tray Drawings:
  www.linear.com/packaging

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating temperature range, otherwise specifications are at T_A = 25°C, RUN = 2V (Note 4).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input DC Voltage	RUN = 2V	●			2.8	V
V_{OUT} DC Voltage	R_{ADJ} = 15.4k R_{ADJ} = 8.25k R_{ADJ} = 1.78k	●	 4.75 	2.5 5 24	 5.25 	V V V
V_{IN} Quiescent Current	V_{RUN} = 0V Not Switching			 7	3 	µA mA
V_{OUT} Line Regulation	3V ≤ V_{IN} ≤ 40V, I_{OUT} = 0.1A, RUN = 2V			1		%
V_{OUT} Load Regulation	0.05A ≤ I_{OUT} ≤ 0.3A, RUN = 2V			1		%
V_{OUT} Ripple (RMS)	I_{OUT} = 0.1A, 1MHz BW			30		mV
Isolation Voltage	(Note 3)			2		kV
Input Short-Circuit Current	V_{OUT} Shorted			80		mA
RUN Pin Input Threshold	RUN Pin Falling		1.18	1.214	1.25	V
RUN Pin Current	V_{RUN} = 1V V_{RUN} = 1.3V			2.5 	 0.1	µA µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: V_{IN} + V_{OUT} is defined as the sum of (V_{IN} – GND) + (V_{OUT} – V_{OUTN}).

Note 3: The LTM8067 isolation test voltage of either 2kVAC or its equivalent of 2.83kVDC is applied for one second.

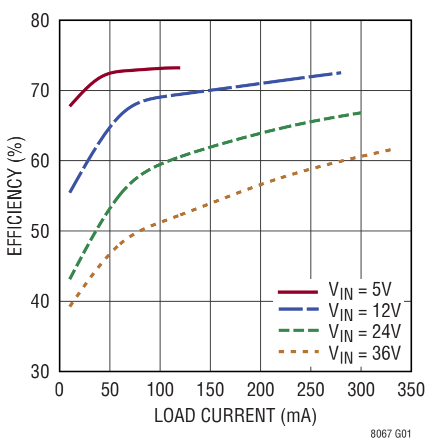
Note 4: The LTM8067E is guaranteed to meet performance specifications from 0°C to 125°C. Specifications over the –40°C to 125°C internal temperature range are assured by design, characterization and correlation with statistical process controls. LTM8067I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Test flowcharts are posted for viewing at:

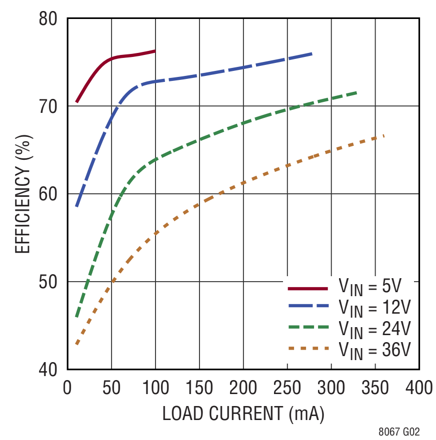
www.linear.com/quality

TYPICAL PERFORMANCE CHARACTERISTICS Unless otherwise noted, operating conditions are as in Table 1 (T_A = 25°C).

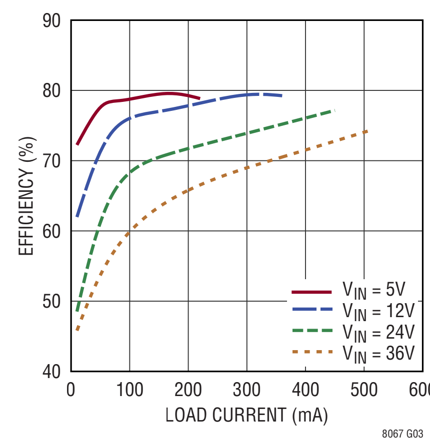
Efficiency vs Load Current, V_{OUT} = 2.5V



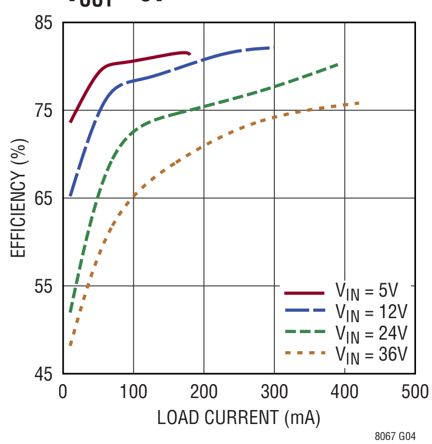
Efficiency vs Load Current, V_{OUT} = 3.3V



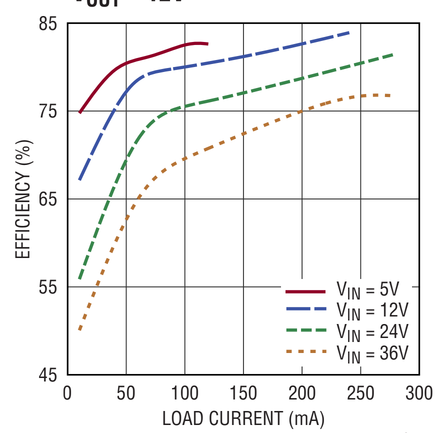
Efficiency vs Load Current, V_{OUT} = 5V



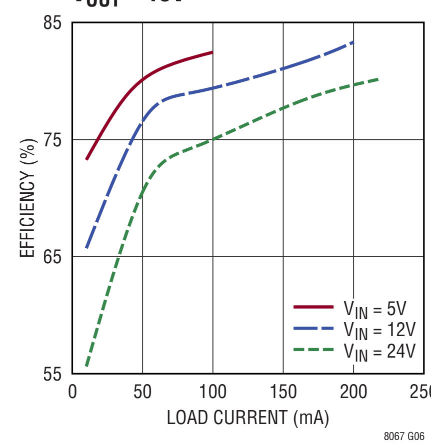
Efficiency vs Load Current, V_{OUT} = 8V



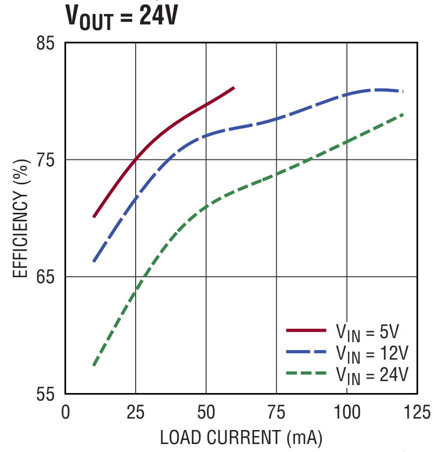
Efficiency vs Load Current, V_{OUT} = 12V



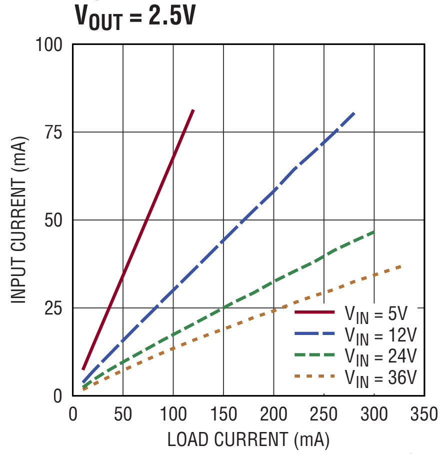
Efficiency vs Load Current, V_{OUT} = 15V



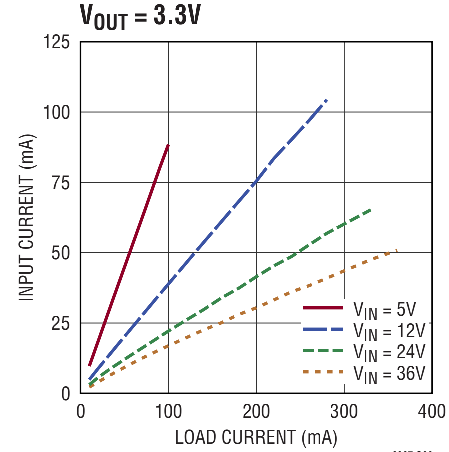
Efficiency vs Load Current, V_{OUT} = 24V



Input Current vs Load Current V_{OUT} = 2.5V



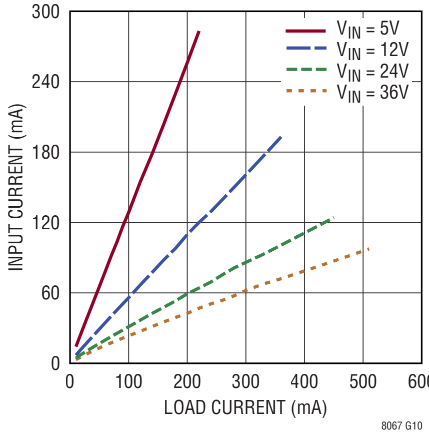
Input Current vs Load Current V_{OUT} = 3.3V



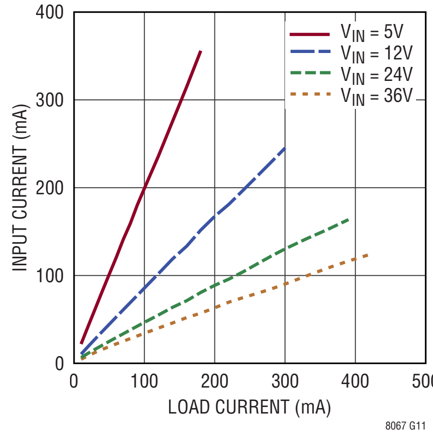
TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, operating conditions are as in Table 1 (T_A = 25°C).

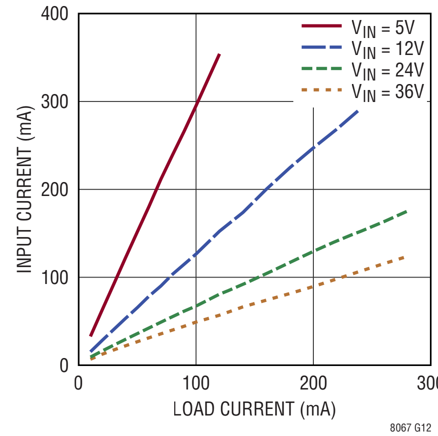
Input Current vs Load Current V_{OUT} = 5V



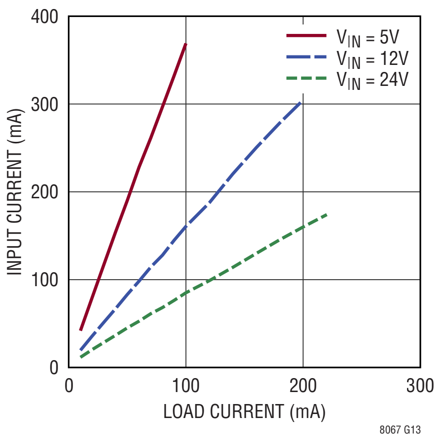
Input Current vs Load Current V_{OUT} = 8V



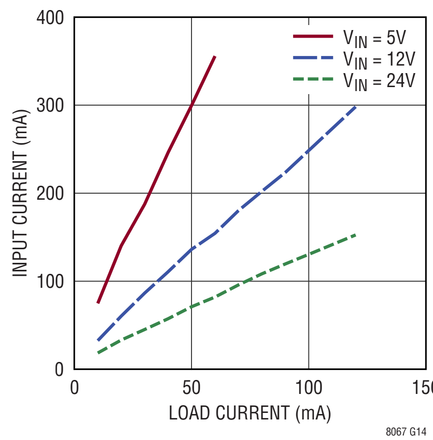
Input Current vs Load Current V_{OUT} = 12V



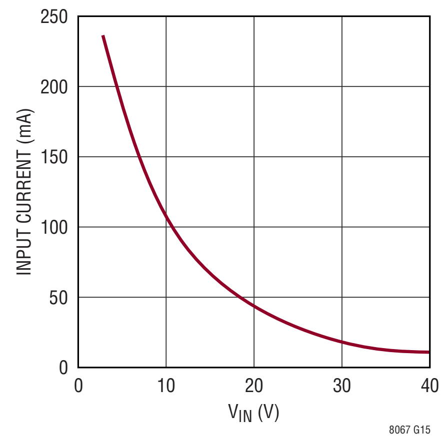
Input Current vs Load Current V_{OUT} = 15V



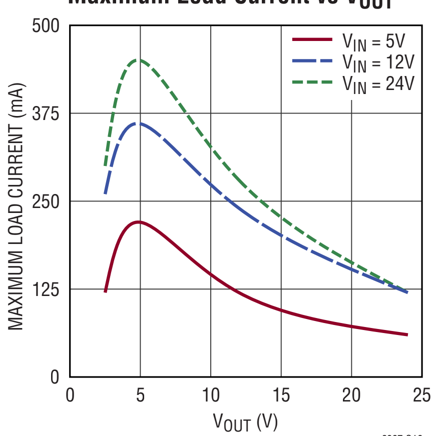
Input Current vs Load Current V_{OUT} = 24V



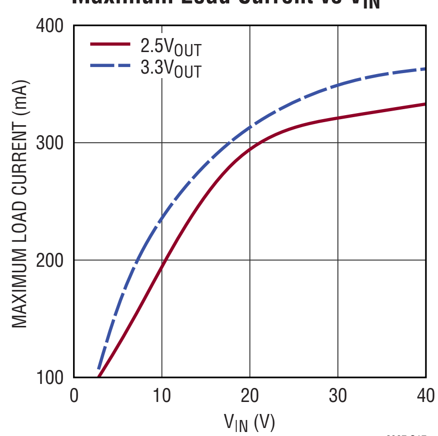
Input Current vs V_{IN}, V_{OUT} Shorted



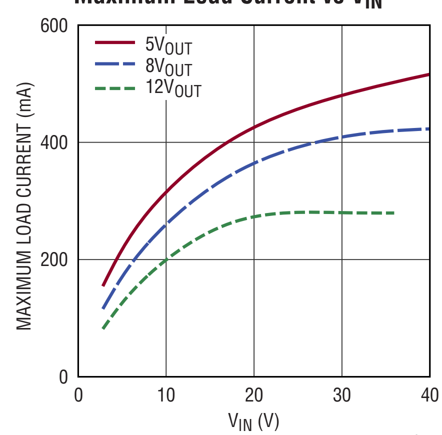
Maximum Load Current vs V_{OUT}



Maximum Load Current vs V_{IN}

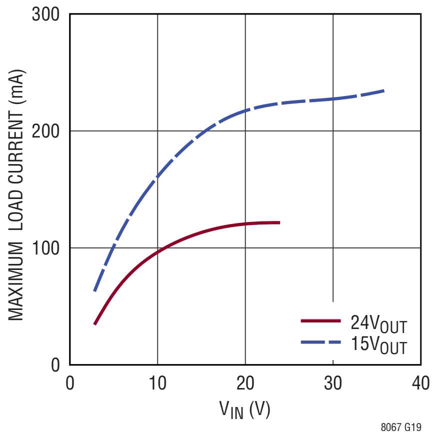


Maximum Load Current vs V_{IN}

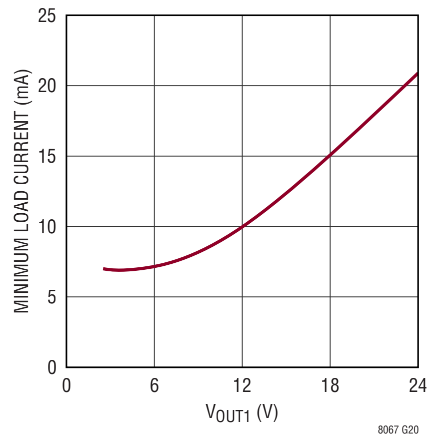


TYPICAL PERFORMANCE CHARACTERISTICS Unless otherwise noted, operating conditions are as in Table 1 (T_A = 25°C).

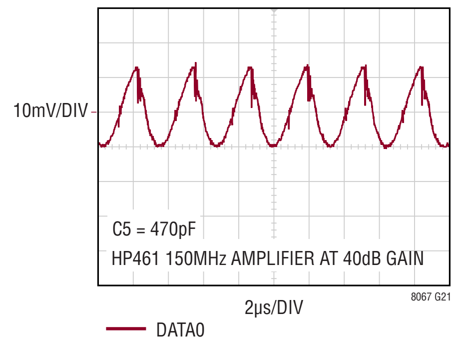
Maximum Load Current vs V_{IN}



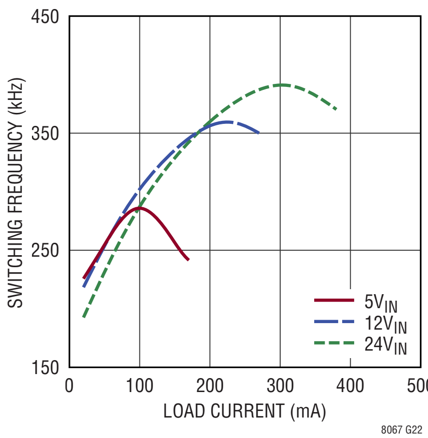
Minimum Load Current vs V_{OUT} Over Full Output Voltage Range



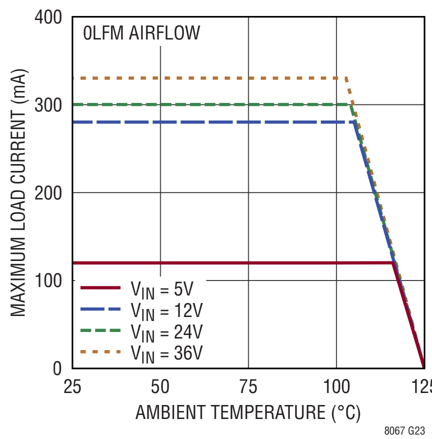
Output Noise and Ripple DC2357A, 200mA Load Current



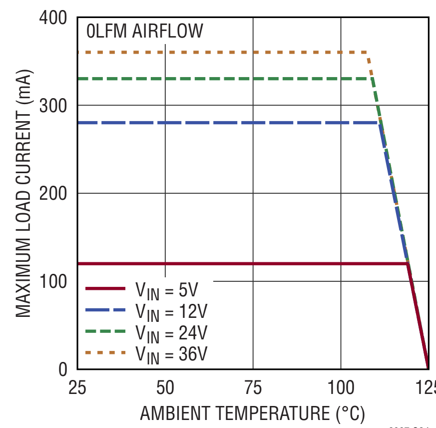
Frequency vs VOUT Load Current Stock DC2357A Demo Board



Derating, 2.5V_{OUT}

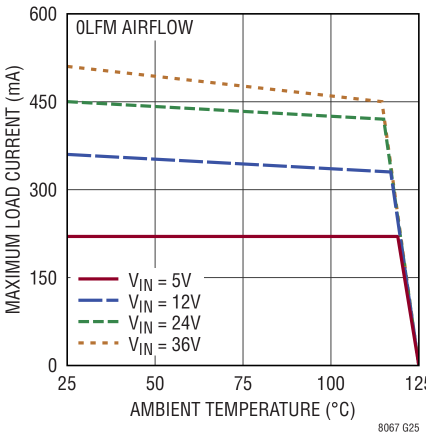


Derating, 3.3V_{OUT}

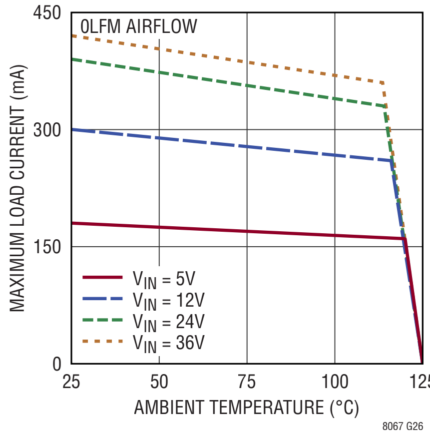


TYPICAL PERFORMANCE CHARACTERISTICS Unless otherwise noted, operating conditions are as in Table 1 (T_A = 25°C).

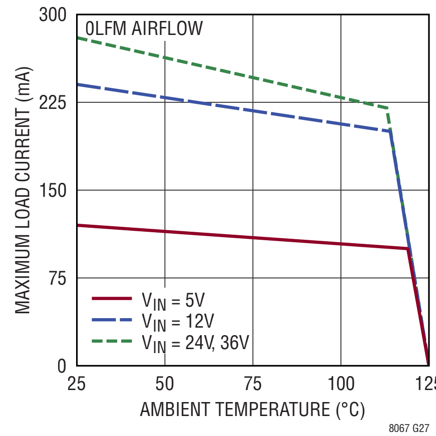
Derating, 5V$_{OUT}$



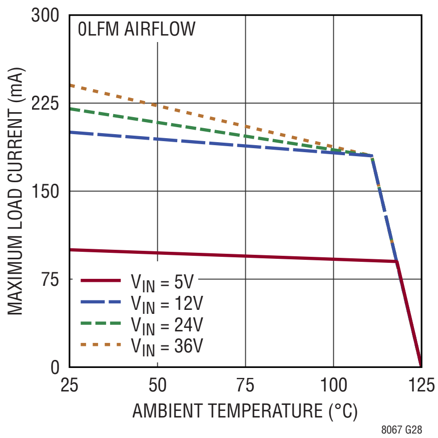
Derating, 8V$_{OUT}$



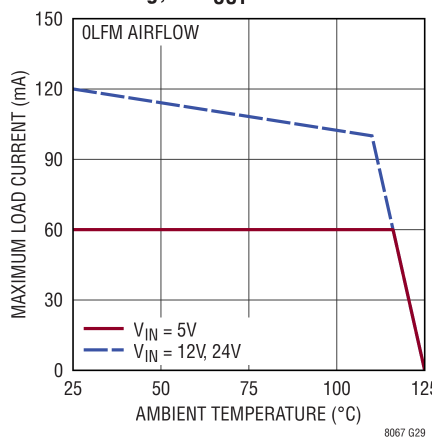
Derating, 12V$_{OUT}$



Derating, 15V$_{OUT}$



Derating, 24V$_{OUT}$



PIN FUNCTIONS

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

V_{OUT} (Bank 1): V_{OUT} and V_{OUTN} comprise the isolated output of the LTM8067 flyback stage. Apply an external capacitor between V_{OUT} and V_{OUTN}. Do not allow V_{OUTN} to exceed V_{OUT}.

V_{OUTN} (Bank 2): V_{OUTN} is the return for V_{OUT}. V_{OUT} and V_{OUTN} comprise the isolated output of the LTM8067. In most applications, the bulk of the heat flow out of the LTM8067 is through the GND and V_{OUTN} pads, so the printed circuit design has a large impact on the thermal performance of the part. See the PCB Layout and Thermal Considerations sections for more details. Apply an external capacitor between V_{OUT} and V_{OUTN}.

GND (Bank 4): This is the primary side local ground of the LTM8067 primary. In most applications, the bulk of the heat flow out of the LTM8067 is through the GND and V_{OUTN} pads, so the printed circuit design has a large impact on the thermal performance of the part. See the PCB Layout and Thermal Considerations sections for more details.

V_{IN} (Bank 5): V_{IN} supplies current to the LTM8067's internal regulator and to the integrated power switch. These pins must be locally bypassed with an external, low ESR capacitor.

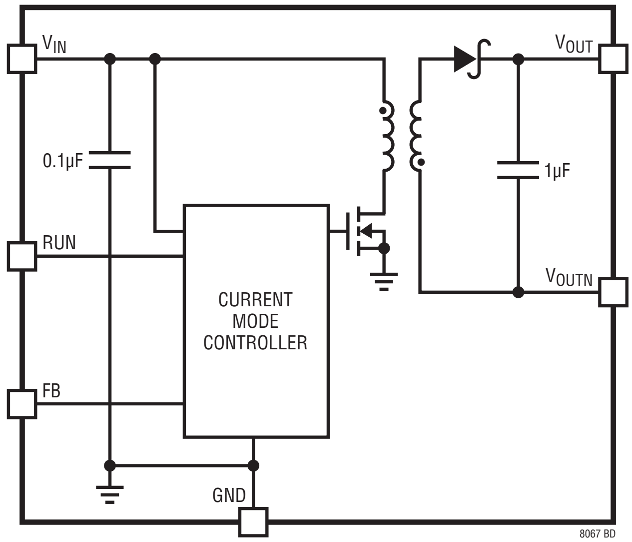
RUN (Pin F3): A resistive divider connected to V_{IN} and this pin programs the minimum voltage at which the LTM8067 will operate. Below 1.214V, the LTM8067 does not deliver power to the secondary. When RUN is less than 1.214V, the pin draws 2.5µA, allowing for a programmable hysteresis. Do not allow a negative voltage (relative to GND) on this pin. Tie this pin to V_{IN} if it is not used.

FB (Pins G7): Apply a resistor from this pin to GND to set the output voltage V_{OUTN} relative to V_{OUTN}, using the recommended value given in Table 1. If Table 1 does not list the desired V_{OUT} value, the equation:

$$R_{FB} = 37.415\left(V_{OUT}^{-0.955}\right)k\Omega$$

may be used to approximate the value. To the seasoned designer, this exponential equation may seem unusual. The equation is exponential due to nonlinear current sources that are used to temperature compensate the regulation. Do not drive this pin with an external power source.

BLOCK DIAGRAM



OPERATION

The LTM8067 is a stand-alone isolated flyback switching DC/DC power supply that can deliver up to 450mA of output current at $5V_{OUT}$, $24V_{IN}$. This module provides a regulated output voltage programmable via one external resistor from 2.5V to 24V. The input voltage range of the LTM8067 is 2.8V to 40V. Given that the LTM8067 is a flyback converter, the output current depends upon the input and output voltages, so make sure that the input voltage is high enough to support the desired output voltage and load current. The Typical Performance Characteristics section gives several graphs of the maximum load versus V_{IN} for several output voltages.

A simplified block diagram is given. The LTM8067 contains a current mode controller, power switching element, power transformer, power Schottky diode and a modest amount of input and output capacitance.

The LTM8067 has a galvanic primary to secondary isolation rating of 2kVAC. For details please refer to the Isolation, Working Voltage and Safely Compliance section. The LTM8067 is a UL 60950 recognized component.

The RUN pin is used to turn on or off the LTM8067, disconnecting the output and reducing the input current to 1µA or less.

The LTM8067 is a variable frequency device. For a given input and output voltage, the frequency decreases as the load increases. For light loads, the current through the internal transformer may be discontinuous.

APPLICATIONS INFORMATION

For most applications, the design process is straight forward, summarized as follows:

1. Look at Table 1 and find the row that has the desired input range and output voltage.
2. Apply the recommended C_{IN}, C_{OUT} and R_{FB}.

While these component combinations have been tested for proper operation, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions. Bear in mind that the maximum output current may be limited by junction temperature, the relationship between the input and output voltage magnitude and polarity and other factors. Please refer to the graphs in the Typical Performance Characteristics section for guidance.

Capacitor Selection Considerations

The C_{IN} and C_{OUT} capacitor values in Table 1 are the minimum recommended values for the associated operating conditions. Applying capacitor values below those indicated in Table 1 is not recommended, and may result in undesirable operation. Using larger values is generally acceptable, and can yield improved dynamic response, if it is necessary. Again, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions.

Ceramic capacitors are small, robust and have very low ESR. However, not all ceramic capacitors are suitable. X5R and X7R types are stable over temperature and applied voltage and give dependable service. Other types, including Y5V and Z5U have very large temperature and voltage coefficients of capacitance. In an application circuit they may have only a small fraction of their nominal capacitance resulting in much higher output voltage ripple than expected.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM8067. A ceramic input capacitor combined with trace or cable inductance forms a high-Q (underdamped) tank circuit. If the LTM8067 circuit is plugged into a live supply, the input voltage can ring to much higher than its nominal value, possibly exceeding the device's rating. This situation is easily avoided; see the Hot-Plugging Safely section.

Table 1. Recommended Component Values for Specific V_{OUT} Values

V_{IN}	V_{OUT}	C_{IN}	C_{OUT}	R_{FB}
2.8V to 40V	2.5V	2.2µF, 50V, 1206	100µF, 6.3V, 1210	15.4k
2.8V to 40V	3.3V	2.2µF, 50V, 1206	47µF, 6.3V, 1210	11.8k
2.8V to 40V	5V	2.2µF, 50V, 1206	22µF, 16V, 1210	8.25k
2.8V to 37V	8V	2.2µF, 50V, 1206	22µF, 16V, 1210	5.23k
2.8V to 33V	12V	4.7µF, 50V, 1206	10µF, 50V, 1210	3.48k
2.8V to 30V	15V	4.7µF, 50V, 1206	4.7µF, 25V, 1210	2.8k
2.8V to 27V	18V	4.7µF, 50V, 1206	4.7µF, 25V, 1210	2.37k
2.8V to 21V	24V	4.7µF, 50V, 1206	4.7µF, 25V, 1210	1.78k

Note: An input bulk capacitor is required.

APPLICATIONS INFORMATION

Isolation, Working Voltage and Safety Compliance

The LTM8067 isolation is 100% hi-pot tested by tying all of the primary pins together, all of the secondary pins together and subjecting the two resultant circuits to a high voltage differential for one second. This establishes the isolation voltage rating of the LTM8067 component.

The isolation rating of the LTM8067 is not the same as the working or operational voltage that the application will experience. This is subject to the application's power source, operating conditions, the industry where the end product is used and other factors that dictate design requirements such as the gap between copper planes, traces and component pins on the printed circuit board, as well as the type of connector that may be used. To maximize the allowable working voltage, the LTM8067 has two columns of solder balls removed to facilitate the printed circuit board design. The ball to ball pitch is 1.27mm, and the typical ball diameter is 0.75mm. Accounting for the missing columns and the ball diameter, the printed circuit board may be designed for a metal-to-metal separation of up to 3.06mm. This may have to be reduced somewhat to allow for tolerances in solder mask or other printed circuit board design rules. For those situations where information about the spacing of LTM8067 internal circuitry is required, the minimum metal to metal separation of the primary and secondary is 1mm.

To reiterate, the manufacturer's isolation voltage rating and the required working or operational voltage are often different numbers. In the case of the LTM8067, the isolation voltage rating is established by 100% hi-pot testing. The working or operational voltage is a function of the end product and its system level specifications. The actual required operational voltage is often smaller than the manufacturer's isolation rating.

The LTM8067 is a UL recognized component under UL 60950, file number 464570. The UL 60950 insulation category of the LTM8067 transformer is Functional. Considering UL 60950 Table 2N and the gap distances stated above, 3.06mm external and 1mm internal, the LTM8067 may be operated with up to 250V working voltage in a pollution degree 2 environment. The actual working voltage, insulation category, pollution degree and other critical parameters for the specific end application depend upon the actual environmental, application and safety compliance requirements. It is therefore up to the user to perform a safety and compliance review to ensure that the LTM8067 is suitable for the intended application.

Safety Rated Capacitors

Some applications require safety rated capacitors, which are high voltage capacitors that are specifically designed and rated for AC operation and high voltage surges. These capacitors are often certified to safety standards such as UL 60950, IEC 60950 and others. In the case of the LTM8067, a common application of a safety rated capacitor would be to connect it from GND to V_{OUTN}. To provide maximum flexibility, the LTM8067 does not include any components between GND and V_{OUTN}. Any safety capacitors must be added externally.

The specific capacitor and circuit configuration for any application depends upon the safety requirements of the system into which the LTM8067 is being designed. Table 2 provides a list of possible capacitors and their manufacturers. The application of a capacitor from GND to V_{OUTN} may also reduce the high frequency output noise on the output.

Table 2. Safety Rated Capacitors

MANUFACTURER	PART NUMBER	DESCRIPTION
Murata Electronics	GA343DR7GD472KW01L	4700pF, 250V AC, X7R, 4.5mm × 3.2mm Capacitor
Johanson Dielectrics	302R29W471KV3E-****-SC	470pF, 250V AC, X7R, 4.5mm × 2mm Capacitor
Syfer Technology	1808JA250102JCTSP	100pF, 250V AC, C0G, 1808 Capacitor

APPLICATIONS INFORMATION

PCB Layout

Most of the headaches associated with PCB layout have been alleviated or even eliminated by the high level of integration of the LTM8067. The LTM8067 is nevertheless a switching power supply, and care must be taken to minimize electrical noise to ensure proper operation. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See Figure 1 for a suggested layout. Ensure that the grounding and heat sinking are acceptable.

A few rules to keep in mind are:

1. Place the R_{FB} resistor as close as possible to its respective pin.
2. Place the C_{IN} capacitor as close as possible to the V_{IN} and GND connections of the LTM8067.
3. Place the C_{OUT} capacitor as close as possible to V_{OUT} and V_{OUTN}
4. Place the C_{IN} and C_{OUT} capacitors such that their ground current flow directly adjacent to or underneath the LTM8067.
5. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM8067.
6. Use vias to connect the GND copper area to the board's internal ground planes. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board. Pay attention to the location and density of the thermal vias in Figure 1. The LTM8067 can benefit from the heat sinking afforded by vias that connect to internal GND planes at these locations, due to their proximity to internal power handling components. The optimum number of thermal vias depends upon the printed circuit board design. For example, a board might use very small via holes. It should employ more thermal vias than a board that uses larger holes.

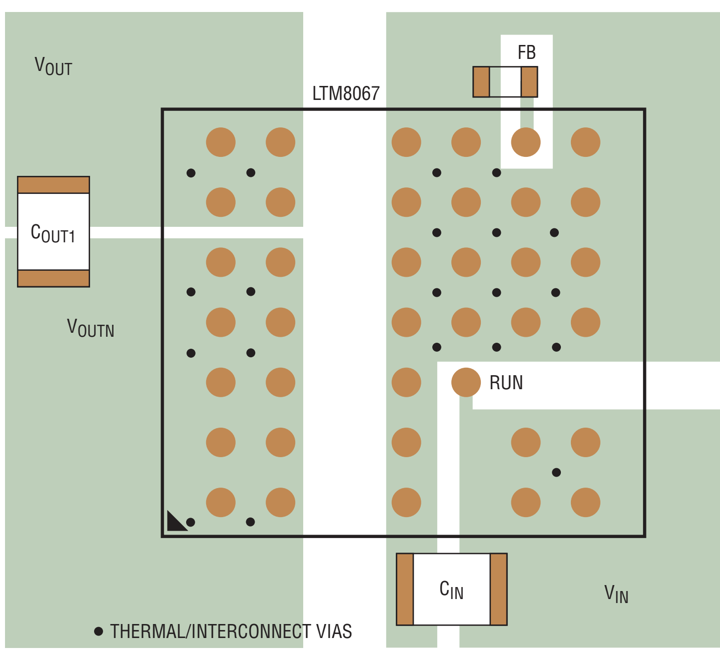


Figure 1. Layout Showing Suggested External Components, Planes and Thermal Vias

APPLICATIONS INFORMATION

Minimum Load

Due to the nature of the flyback regulator in general, and the LTM8067 control scheme specifically, the LTM8067 requires a minimum load for proper operation. Otherwise, the output may go out of regulation if the load is too light. The most common way to address this is to place a resistor across the output. The Minimum Load Current vs V_{OUT} Over Full Output Voltage Range graph in the Typical Performance Characteristics section may be used as a guide in selecting the resistor. Note that this graph describes room temperature operation. If the end application operates at a colder temperature, the minimum load requirement may be higher and the minimum load condition must be characterized for the lowest operating temperature.

If it is impractical to place a resistive load permanently across the output, a resistor and Zener diode may be used instead, as shown in Figure 2. While the minimum load resistor mentioned in the prior paragraph will always draw current while the LTM8067 output is powered, the series resistor-Zener diode combination will only draw current if the output is too high. When using this circuit, take care to ensure that the characteristics of the Zener diode are appropriate for the intended application's temperature range.

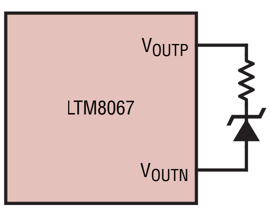


Figure 2: Use a Resistor and Zener Diode to Meet the Minimum Load Requirement

Hot-Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of the LTM8067. However, these capacitors can cause problems if the LTM8067 is plugged into a live supply (see Linear Technology Application Note 88 for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the V_{IN} pin of the LTM8067 can ring to more than twice the nominal input voltage, possibly exceeding the LTM8067's rating and damaging the part. If the input supply is poorly controlled or the user will be plugging the LTM8067 into an energized supply, the input network should be designed to prevent this overshoot. This can be accomplished by installing a small resistor in series to V_{IN}, but the most popular method of controlling input voltage overshoot is adding an electrolytic bulk capacitor to the V_{IN} net. This capacitor's relatively high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low frequency ripple filtering and can slightly improve the efficiency of the circuit, though it can be a large component in the circuit.

Thermal Considerations

The LTM8067 output current may need to be derated if it is required to operate in a high ambient temperature. The amount of current derating is dependent upon the input voltage, output power and ambient temperature. The temperature rise curves given in the Typical Performance Characteristics section can be used as a guide. These curves were generated by the LTM8067 mounted to a 58cm^2 4-layer FR4 printed circuit board. Boards of other sizes and layer count can exhibit different thermal behavior, so it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental operating conditions.

For increased accuracy and fidelity to the actual application, many designers use FEA to predict thermal performance. To that end, the Pin Configuration section of the data sheet typically gives four thermal coefficients:

θ_{JA}: Thermal resistance from junction to ambient

$\theta_{JCbottom}$: Thermal resistance from junction to the bottom of the product case

θ_{JCtop}: Thermal resistance from junction to top of the product case

$\theta_{JCboard}$: Thermal resistance from junction to the printed circuit board.

While the meaning of each of these coefficients may seem to be intuitive, JEDEC has defined each to avoid

APPLICATIONS INFORMATION

confusion and inconsistency. These definitions are given in JESD 51-12, and are quoted or paraphrased as follows:

θ_{JA} is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as still air although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.

$\theta_{JCbottom}$ is the junction-to-board thermal resistance with all of the component power dissipation flowing through the bottom of the package. In the typical µModule converter, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.

θ_{JCtop} is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule converter are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

$\theta_{JCboard}$ is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule converter and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two-sided, two-layer board. This board is described in JESD 51-9.

Given these definitions, it should now be apparent that none of these thermal coefficients reflects an actual physical operating condition of a µModule converter. Thus, none of them can be individually used to accurately predict the thermal performance of the product. Likewise, it would be inappropriate to attempt to use any one coefficient to correlate to the junction temperature vs load graphs given in the product's data sheet. The only appropriate way to use the coefficients is when running a detailed thermal analysis, such as FEA, which considers all of the thermal resistances simultaneously.

A graphical representation of these thermal resistances is given in Figure 3.

The blue resistances are contained within the µModule converter, and the green are outside.

The die temperature of the LTM8067 must be lower than the maximum rating of 125°C, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM8067. The bulk of the heat flow out of the LTM8067 is through the bottom of the module and the BGA pads into the printed circuit board. Consequently a poor printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. Please refer to the PCB Layout section for printed circuit board design suggestions.

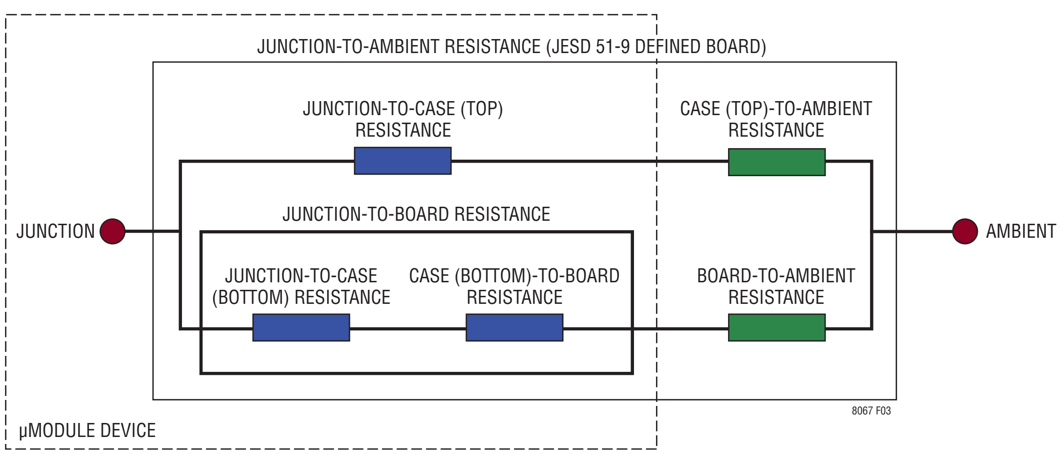
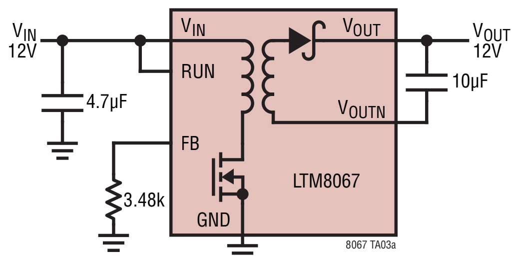


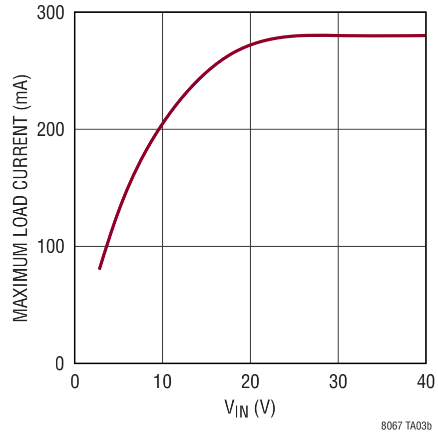
Figure 3. Approximate Thermal Model of LTM8067

APPLICATIONS INFORMATION

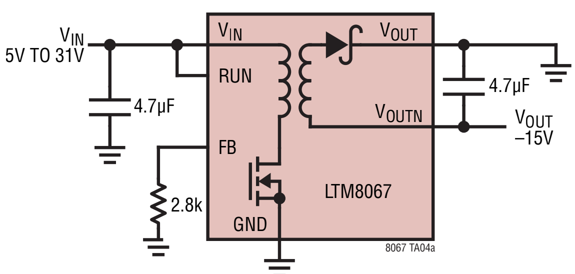
12V Flyback Converter



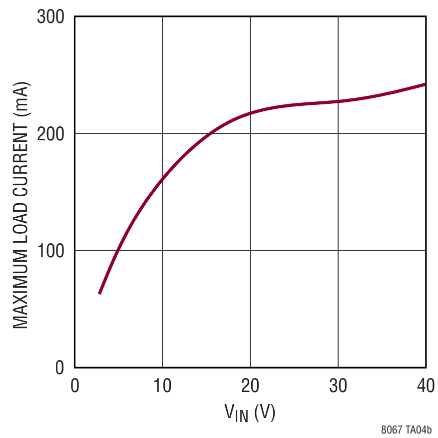
Maximum Load Current vs V_{IN}



–15V Inverting Regulator



Maximum Load Current vs V_{IN}

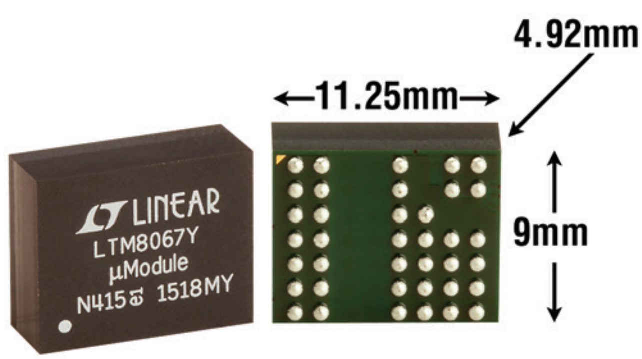


PACKAGE DESCRIPTION

Pin Assignment Table
(Arranged by Pin Number)

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
A1	V_{OUTN}	B1	V_{OUTN}	C1	-	D1	-	E1	GND	F1	-	G1	V_{IN}	H1	V_{IN}
A2	V_{OUTN}	B2	V_{OUTN}	C2	-	D2	-	E2	GND	F2	-	G2	V_{IN}	H2	V_{IN}
A3	V_{OUTN}	B3	V_{OUTN}	C3	-	D3	-	E3	GND	F3	RUN	G3	-	H3	-
A4	V_{OUTN}	B4	V_{OUTN}	C4	-	D4	-	E4	GND	F4	GND	G4	GND	H4	GND
A5	V_{OUTN}	B5	V_{OUTN}	C5	-	D5	-	E5	GND	F5	GND	G5	GND	H5	GND
A6	V_{OUT}	B6	V_{OUT}	C6	-	D6	-	E6	GND	F6	GND	G6	GND	H6	GND
A7	V_{OUT}	B7	V_{OUT}	C7	-	D7	-	E7	GND	F7	GND	G7	FB	H7	GND

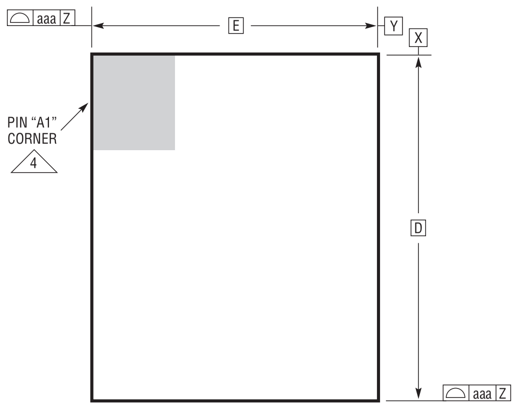
PACKAGE PHOTO



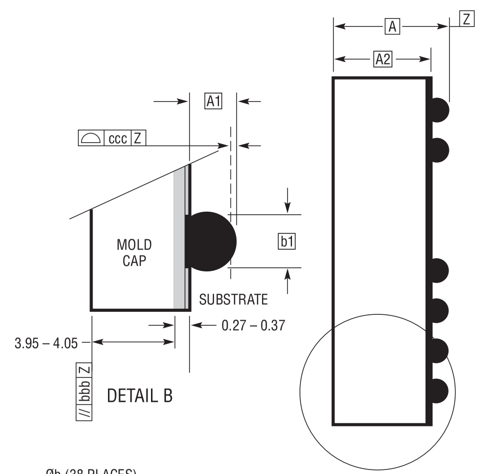
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTM8067#packaging for the most recent package drawings.

BGA Package
38-Lead (11.25mm × 9.00mm × 4.92mm)
(Reference LTC DWG # 05-08-1925 Rev A)

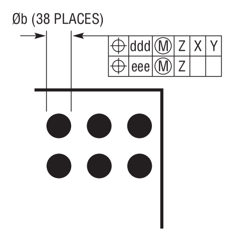


PACKAGE TOP VIEW

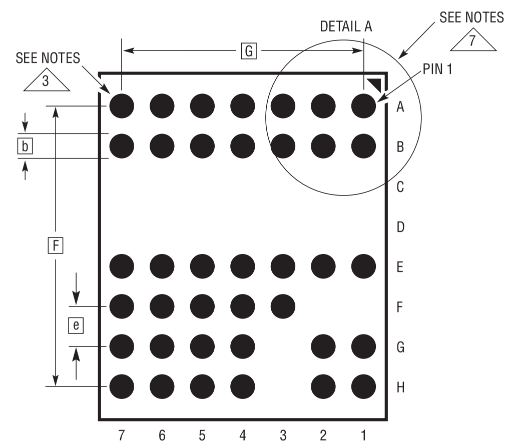


DETAIL B

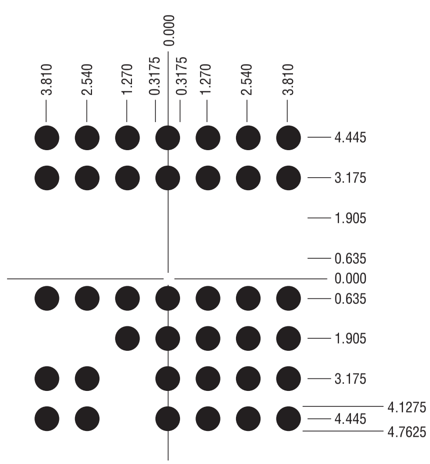
DETAIL B
PACKAGE SIDE VIEW



DETAIL A



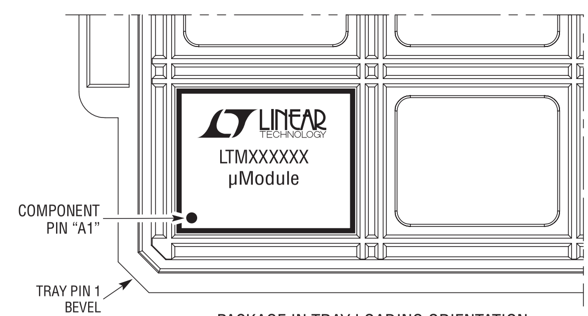
PACKAGE BOTTOM VIEW



SUGGESTED PCB LAYOUT
TOP VIEW

DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	4.72	4.92	5.12	
A1	0.50	0.60	0.70	
A2	4.22	4.32	4.42	
b	0.60	0.75	0.90	
b1	0.60	0.63	0.66	
D		11.25		
E		9.0		
e		1.27		
F		8.89		
G		7.62		
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
TOTAL NUMBER OF BALLS: 38				

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JESD MS-028 AND JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. SOLDER BALL COMPOSITION IS 96.5% Sn/3.0% Ag/0.5% Cu
7. ⚠ PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY



PACKAGE IN TRAY LOADING ORIENTATION

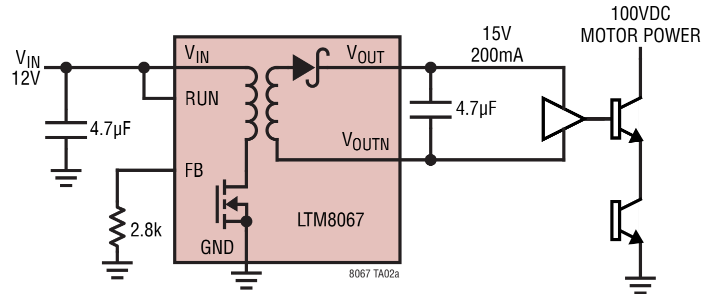
BGA 38 1212 REV A

REVISION HISTORY

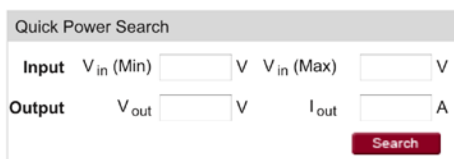
REV	DATE	DESCRIPTION	PAGE NUMBER
A	05/16	Corrected symbol of internal switch in block diagram from NPN transistor to N-channel MOSFET	9
B	11/16	Corrected V_{OUT} on Maximum Load Current vs V_{IN} from $12V_{OUT}$ to $24V_{OUT}$ and from $15V_{OUT}$ to $12V_{OUT}$	6
		Corrected minimum metal to metal space from 0.75mm to 1mm	12
		Updated the Related Parts Table	20
C	07/17	Added Minimum Load section	14

TYPICAL APPLICATION

15V Floating 1GBT Gate Drive



DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. 	
TechClip Videos	Quick videos detailing how to bench test electrical and thermal performance of µModule products.	
Digital Power System Management	Linear Technology's family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM8068	2kVAC Isolated µModule Converter with LDO Post Regulator	$2.8V \le V_{IN} \le 40V$, $1.2V \le V_{OUT} \le 18V$; $20µV_{RMS}$ Output Ripple. UL60950 Recognized.
LTM8047	725VDC, 1.5W Isolated µModule Converter	$3.1V \le V_{IN} \le 32V$, $2.5V \le V_{OUT} \le 12V$
LTM8048	725VDC, 1.5W Isolated µModule Converter with LDO Post Regulator	$3.1V \le V_{IN} \le 32V$, $1.2V \le V_{OUT} \le 12V$; $20µV_{RMS}$ Output Ripple
LTM8045	Inverting or SEPIC µModule DC/DC Convertor	$2.8V \le V_{IN} \le 18V$, $2.5V \le V_{OUT} \le 15V$ or $-2.5V \le V_{OUT} \le -15V$, Up to 700mA
LT®8300	Isolated Flyback Convertor with $100V_{IN}$, 150V/260mA Power Switch	$6V \le V_{IN} \le 100V$, No Opt-Isolator Required
LT8301	Isolated Flyback Convertor with 65V/1.2A Power Switch	$2.7V \le V_{IN} \le 42V$, No Opt-Isolator Required
LT8302	Isolated Flyback Convertor with 65V/3.6A Power Switch	$2.8V \le V_{IN} \le 42V$, No Opt-Isolator Required
LTM8049	Dual Outputs, SEPIC and/or Inverting µModule Regulator	$2.6V \le V_{IN} \le 20V$, $\pm2.5V \le V_{OUT} \le \pm25V$, 9mm × 15mm × 2.42mm BGA

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