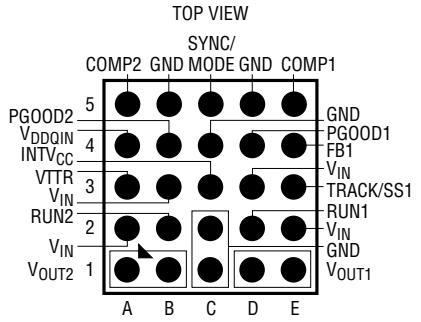
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} ..... –0.3V to 16V
V_{OUT} ..... –0.3V to 6V
PGOOD1, PGOOD2 ..... –0.3V to 16V
RUN1, RUN2 ..... –0.3V to V_{IN}+0.3V
$INTV_{CC}$, TRACK/SS1, V_{DDQIN}, VTTR ..... –0.3V to 3.6V
SYNC/MODE, COMP1, COMP2,
FB1, FB2 ..... –0.3V to $INTV_{CC}$
Operating Internal Temperature Range
(Notes 2, 3, 5) ..... –40°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Peak Solder Reflow Body Temperature ..... 260°C

PIN CONFIGURATION

(See Pin Functions, Pin Configuration Table)



LGA PACKAGE 25-LEAD (6.25mm × 6.25mm × 1.82mm)
BGA PACKAGE 25-LEAD (6.25mm × 6.25mm × 2.42mm)
T_{JMAX} = 125°C, θ_{JCtop} = 17°C/W, $\theta_{JCbottom}$ = 11°C/W,
θ_{JB} +θ_{BA} = 22°C/W, θ_{JA} = 20°C/W
WEIGHT = 0.21g

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTM4632EV#PBF	Au (RoHS)	LTM4632V	e4	LGA	3	–40°C to 125°C
LTM4632IV#PBF	Au (RoHS)	LTM4632V	e4	LGA	3	–40°C to 125°C
LTM4632EY#PBF	SAC305 (RoHS)	LTM4632Y	e1	BGA	3	–40°C to 125°C
LTM4632IY#PBF	SAC305 (RoHS)	LTM4632Y	e1	BGA	3	–40°C to 125°C
LTM4632IY	SnPb (63/37)	LTM4632Y	e0	BGA	3	–40°C to 125°C

- Contact the factory for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications that apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel at T_A = 25°C (Note 2), V_{IN} = 12V, unless otherwise noted, per the typical application in Figure 19

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input DC Voltage		●	3.6		15	V
$V_{IN\_3.3}$	3.3V Input DC Voltage	V_{IN} = $INTV_{CC}$	●	3.1	3.3	3.5	V
$V_{OUT1(RANGE)}$ $V_{OUT2(RANGE)}$	Output Voltage Range	V_{IN} = 3.6V to 15V	● ●	0.6		2.5 1.8	V V
Output Specification (Channel 1)							
V_{OUT1}(DC)	CH1 Output Voltage, Total Variation with Line and Load	C_{IN} = 22µF, C_{OUT} = 100µF Ceramic R_{FB1} = 51.7k, MODE = GND, I_{OUT} = –3A to 3A	●	1.28	1.30	1.32	V
I_{OUT1}(DC)	CH1 Output Continuous Current Range	V_{IN} = 12V, V_{OUT1} = 1.3V (Note 3)		–3		3	A
IQ1(V_{IN})	CH1 Input Supply Bias Current	V_{IN} = 12V, V_{OUT1} = 1.3V, MODE = GND V_{IN} = 12V, V_{OUT1} = 1.3V, MODE = $INTV_{CC}$ Shutdown, RUN1 = GND			13 400 40		mA µA µA
IS1(V_{IN})	CH1 Input Supply Current	V_{IN} = 12V, V_{OUT1} = 1.3V, I_{OUT} = 3A			0.4		A
ΔV_{OUT1}(Line)/V_{OUT1}	CH1 Line Regulation Accuracy	V_{OUT1} = 1.3V, V_{IN} = 3.6V to 15V, I_{OUT1} = 0A	●		0.01	0.05	%/V
ΔV_{OUT1}(Load)/V_{OUT1}	CH1 Load Regulation Accuracy	V_{OUT1} = 1.3V, I_{OUT} = –3A to 3A	●		0.2	1.0	%
V_{OUT1}(AC)	CH1 Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 47µF Ceramic V_{IN} = 12V, V_{OUT1} = 1.3V			30		mV
ΔV_{OUT1}(START)	CH1 Turn-On Overshoot	I_{OUT} = 0A, C_{OUT} = 47µF Ceramic, TRACK/SS1 = –0.1µF, V_{IN} = 12V, V_{OUT1} = 1.3V			30		mV
t_{START}	Turn-On Time	C_{OUT} = 100µF Ceramic, TRACK/SS1 = 0.01µF No Load, V_{IN} = 12V, V_{OUT1} = 1.3V			1.2		ms
ΔV_{OUTLS1}	CH1 Peak Deviation for Dynamic Load	Load: 0% to 25% to 0% of Full Load C_{OUT} = 47µF Ceramic, V_{IN} = 12V, V_{OUT1} = 1.3V			85		mV
$t_{SETTLE1}$	CH1 Settling Time for Dynamic Load Step	Load: 0% to 25% to 0% of Full Load C_{OUT} = 47µF Ceramic, V_{IN} = 12V, V_{OUT1} = 1.3V			20		µs
IOUTPK1	CH1 Output Current Limit	V_{IN} = 12V, V_{OUT1} = 1.3V			4.5		A
Output Specification (Channel 2)							
V_{OUT2}(DC)	CH2 Output Voltage, Total Variation with Line and Load	C_{IN} = 22µF, C_{OUT} = 100µF Ceramic V_{DDQIN}= 1.3V, MODE = GND, I_{OUT} = –3A to 3A	●	637	650	663	mV
I_{OUT2}(DC)	CH2 Output Continuous Current Range	V_{IN} = 12V, V_{DDQIN} = 1.3V (Note 3)		–3		3	A
IQ2(V_{IN})	CH2 Input Supply Bias Current	V_{IN} = 12V, V_{DDQIN} = 1.3V, MODE = GND Shutdown, RUN2 = 0			7 40		mA µA
IS2(V_{IN})	CH2 Input Supply Current	V_{IN} = 12V, V_{DDQIN} = 1.3V, I_{OUT} = 3A			0.25		A
ΔV_{OUT2}(Line)/V_{OUT2}	CH2 Line Regulation Accuracy	V_{DDQIN} = 1.3V, V_{IN} = 3.6V to 15V, I_{OUT2} = 0A	●		0.01	0.05	%/V
ΔV_{OUT2}(Load)/V_{OUT2}	CH2 Load Regulation Accuracy	V_{DDQIN} = 1.3V, I_{OUT} = –3A to 3A	●		0.2	1.0	%
V_{OUT2}(AC)	CH2 Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 100µF Ceramic V_{IN} = 12V, V_{DDQIN} = 1.3V			30		mV
ΔV_{OUTLS2}	CH2 Peak Deviation for Dynamic Load	Load: 0% to 25% to 0% of Full Load C_{OUT} = 47µF Ceramic, V_{IN} = 12V, V_{OUT1} = 1.3V			85		mV
$t_{SETTLE2}$	CH2 Settling Time for Dynamic Load Step	Load: 0% to 25% to 0% of Full Load C_{OUT} = 47µF Ceramic, V_{IN} = 12V, V_{OUT1} = 1.3V			20		µs
IOUTPK2	CH2 Output Current Limit				4.5		A

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications that apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel at T_A = 25°C (Note 2), V_{IN} = 12V, unless otherwise noted, per the typical application in Figure 19

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Control Section							
V_{FB1}	Voltage at V_{FB1} Pin	I_{OUT} = 0A, V_{OUT1} = 1.3V	●	0.593	0.600	0.607	V
I_{FB1}	Current at V_{FB1} Pin	(Note 4)				±30	nA
RFBHI1	Resistor Between V_{OUT1} and V_{FB1} Pins			60.00	60.40	60.80	kΩ
VTTR	VTTR Voltage Reference	V_{DDQIN} = 1.3V, IVTTR = ±10mA, CVTTR < 10nF	●	0.492x V_{DDQIN}	0.50x V_{DDQIN}	0.508x V_{DDQIN}	V
V_{RUN1}, V_{RUN2}	RUN Pin On Threshold	RUN Threshold Rising RUN Threshold Falling		1.18 0.95	1.28 1.01	1.39 1.05	V V
I_{RUN1}, I_{RUN2}	RUN Pin Leakage Current				0	±1	µA
$I_{TRACK/SS1}$	TRACK/SS1 Pin Soft-Start Pull-Up Current	TRACK/SS1 = 0V			1.2		µA
$t_{ON(MIN)}$	Minimum On-Time	(Note 4)			20		ns
$t_{OFF(MIN)}$	Minimum Off-Time	(Note 4)			45		ns
VPGOOD	PGOOD Trip Level	V_{FB} With Respect to 0.6V V_{OUT2} With Respect to V_{DDQIN}/2 (Note 4) Ramping Negative Ramping Positive			 –8 8	 –14 14	 % %
RPGOOD	PGOOD Pull-Down Resistance	1mA Load			15		Ω
V_{INTVCC}	Internal V_{CC} Voltage	V_{IN} = 3.6V to 15V		3.1	3.3	3.5	V
V_{INTVCC} Load Reg	$INTV_{CC}$ Load Regulation	I_{CC} = 0 to 50mA			1.3		%
f_{OSC}	Oscillator Frequency				1		MHz
SYNC	SYNC Threshold Voltage				0.95		V
$I_{SYNC/MODE}$	MODE Input Current	SYNC/MODE = $INTV_{CC}$			–1.5		µA

Note 1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2. The LTM4632 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4632E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4632I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

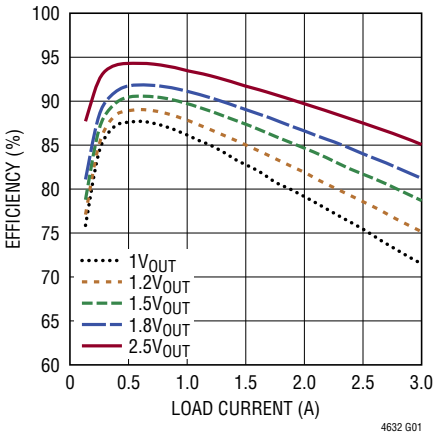
Note 3. See output current derating curves for different V_{IN}, V_{OUT} and T_A.

Note 4. 100% tested at wafer level.

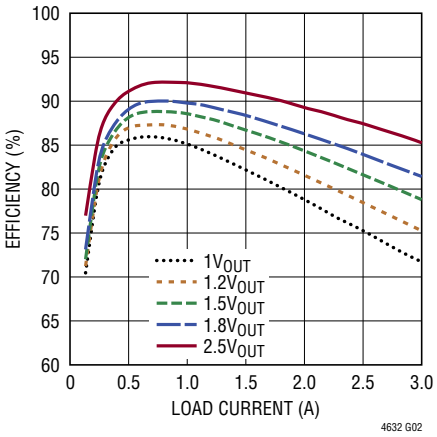
Note 5. This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS

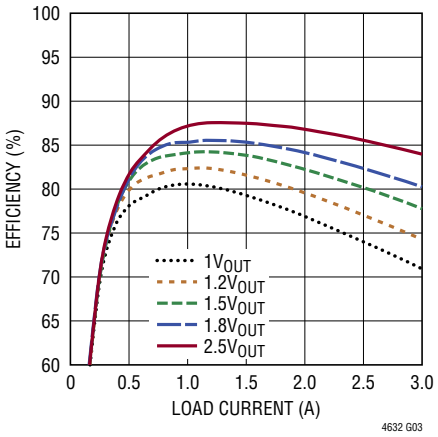
Efficiency vs Load Current at $3.6V_{IN}$



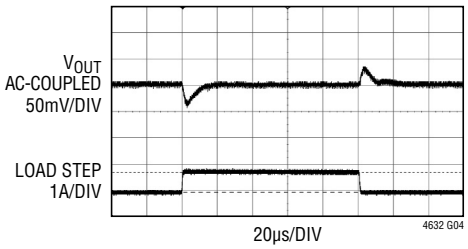
Efficiency vs Load Current at $5V_{IN}$



Efficiency vs Load Current at $12V_{IN}$

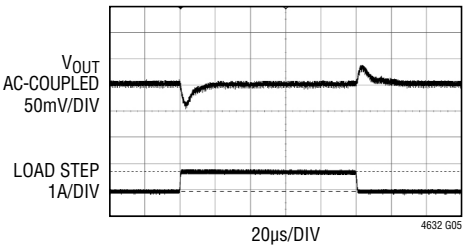


1V Output Transient Response



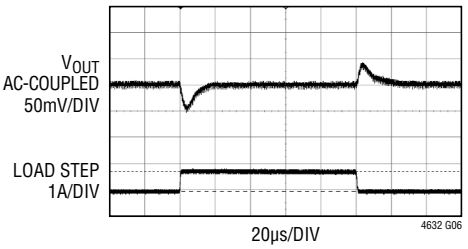
V_{IN} = 12V
V_{OUT} = 1V
f_S = 1MHz
OUTPUT CAPACITOR = 1 × 47µF CERAMIC
LOAD STEP = 2.25A TO 3A

1.2V Output Transient Response



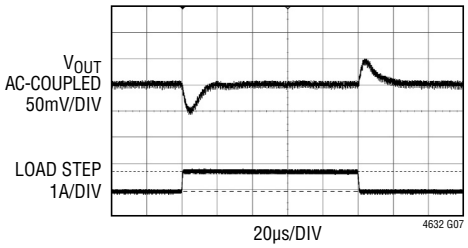
V_{IN} = 12V
V_{OUT} = 1.2V
f_S = 1MHz
OUTPUT CAPACITOR = 1 × 47µF CERAMIC
LOAD STEP = 2.25A TO 3A

1.5V Output Transient Response



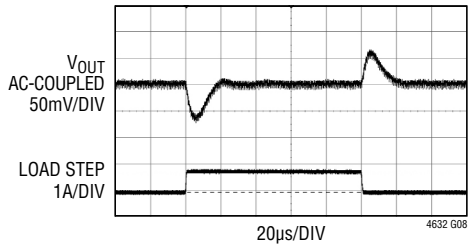
V_{IN} = 12V
V_{OUT} = 1.5V
f_S = 1MHz
OUTPUT CAPACITOR = 1 × 47µF CERAMIC
LOAD STEP = 2.25A TO 3A

1.8V Output Transient Response



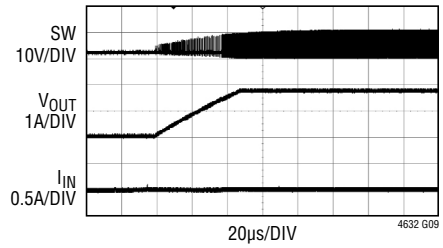
V_{IN} = 12V
V_{OUT} = 1.8V
f_S = 1MHz
OUTPUT CAPACITOR = 1 × 47µF CERAMIC
LOAD STEP = 2.25A TO 3A

2.5V Output Transient Response



V_{IN} = 12V
V_{OUT} = 2.5V
f_S = 1MHz
OUTPUT CAPACITOR = 1 × 47µF CERAMIC
LOAD STEP = 2.25A TO 3A

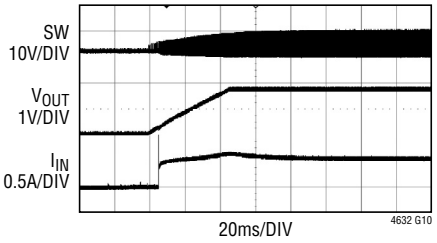
Start-Up with No Load Current Applied



V_{IN} = 12V
V_{OUT} = 1.8V
f_S = 1MHz
I_{OUT} = 0A
INPUT CAPACITOR = 1 × 22µF CERAMIC
OUTPUT CAPACITOR = 1 × 47µF CERAMIC
SOFT-START CAPACITOR = 0.1µF

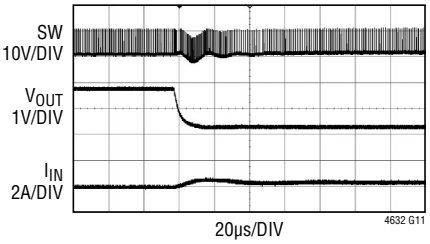
TYPICAL PERFORMANCE CHARACTERISTICS

Start-Up with 3A Load Current Applied



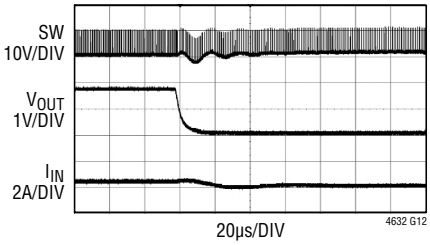
V_{IN} = 12V
V_{OUT} = 1.8V
f_S = 1MHz
I_{OUT} = 3A
INPUT CAPACITOR = 1 × 22µF CERAMIC
OUTPUT CAPACITOR = 1 × 47µF CERAMIC
SOFT-START CAPACITOR = 0.1µF

Short-Circuit with No Load Current Applied



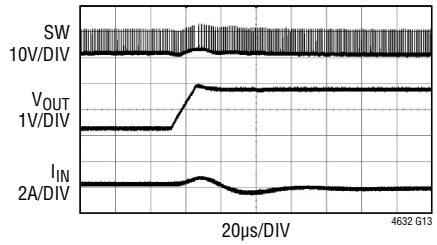
V_{IN} = 12V
V_{OUT} = 1.8V
f_S = 1MHz
I_{OUT} = 0A
INPUT CAPACITOR = 1 × 22µF CERAMIC
OUTPUT CAPACITOR = 1 × 47µF CERAMIC

Short-Circuit with 3A Load Current Applied



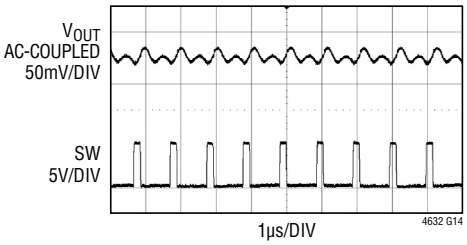
V_{IN} = 12V
V_{OUT} = 1.8V
f_S = 1MHz
I_{OUT} = 3A
INPUT CAPACITOR = 1 × 22µF CERAMIC
OUTPUT CAPACITOR = 1 × 47µF CERAMIC

Recover from Short-Circuit with No Load Current Applied



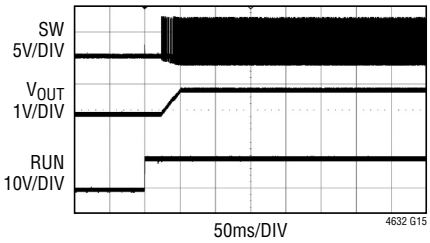
V_{IN} = 12V
V_{OUT} = 1.8V
f_S = 1MHz
I_{OUT} = 0A
INPUT CAPACITOR = 1 × 22µF CERAMIC
OUTPUT CAPACITOR = 1 × 47µF CERAMIC

Steady-State Output Voltage Ripple



V_{IN} = 12V
V_{OUT} = 1.8V
f_S = 1MHz
I_{OUT} = 0A
INPUT CAPACITOR = 1 × 22µF CERAMIC
OUTPUT CAPACITOR = 1 × 47µF CERAMIC

Start-Up Into Pre-Biased Output



V_{IN} = 12V
V_{OUT} = 1.8V
f_S = 1MHz
I_{OUT} = 0A
INPUT CAPACITOR = 1 × 22µF CERAMIC
OUTPUT CAPACITOR = 1 × 47µF CERAMIC

PIN FUNCTIONS

V_{IN} (A2, B3, D3, E2): Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitance directly between V_{IN} pins and GND pins.

V_{OUT1} (D1, E1), V_{OUT2} (A1, B1): Power Output Pins of each Switching Mode Regulator. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins.

GND (C1-C2, C4, B5, D5): Power Ground Pins for Both Input and Output Returns.

PGOOD1 (D4): Output Power Good with Open-Drain Logic of the Channel 1 Switching Mode Regulator. PGOOD1 is pulled to ground when the voltage on the FB1 pin is not within ±8% (typical) of the internal 0.6V reference. This threshold has 15mV of hysteresis.

PGOOD2 (B4): Output Power Good with Open-Drain Logic of the Channel 2 Switching Mode Regulator. PGOOD2 is pulled to ground when the voltage on the V_{OUT2} pin is not within ±8% (typical) of the $V_{DDQIN}/2$ voltage. This threshold has 15mV of hysteresis.

SYNC/MODE (C5): Mode Select and External Synchronization Input. Tie this pin to ground to force continuous synchronous operation at all output loads. Floating this pin or tying it to $INTV_{CC}$ enables high efficiency Burst Mode operation at light loads. Drive this pin with a clock to synchronize the LTM4632 switching frequency. An internal phase-locked loop will force the bottom power NMOS's turn on signal to be synchronized with the rising edge of the clock signal. When this pin is driven with a clock, forced continuous mode is automatically selected.

$INTV_{CC}$ (C3): Internal 3.3V Regulator Output of the Switching Mode Regulator Channel. The internal power drivers and control circuits are powered from this voltage. This pin is internally decoupled to GND with a 2.2µF low ESR ceramic capacitor. No more external decoupling capacitor needed.

RUN1 (D2), RUN2 (B2): Run Control Input of Each Switching Mode Regulator Channel. Enables chip operation by tying RUN above 1.28V. Tying this pin below 1V shuts down the specific regulator channel. Do not float this pin.

COMP1 (E5), COMP2 (A5): Current Control Threshold and Error Amplifier Compensation Point of Each Switching Mode Regulator Channel. The current comparator's trip threshold is linearly proportional to this voltage, whose normal range is from 0.3V to 1.8V. The device is internal compensated. Tie COMP pins together in Dual Phase Single Output VTT Configuration. See the Applications Information section for details.

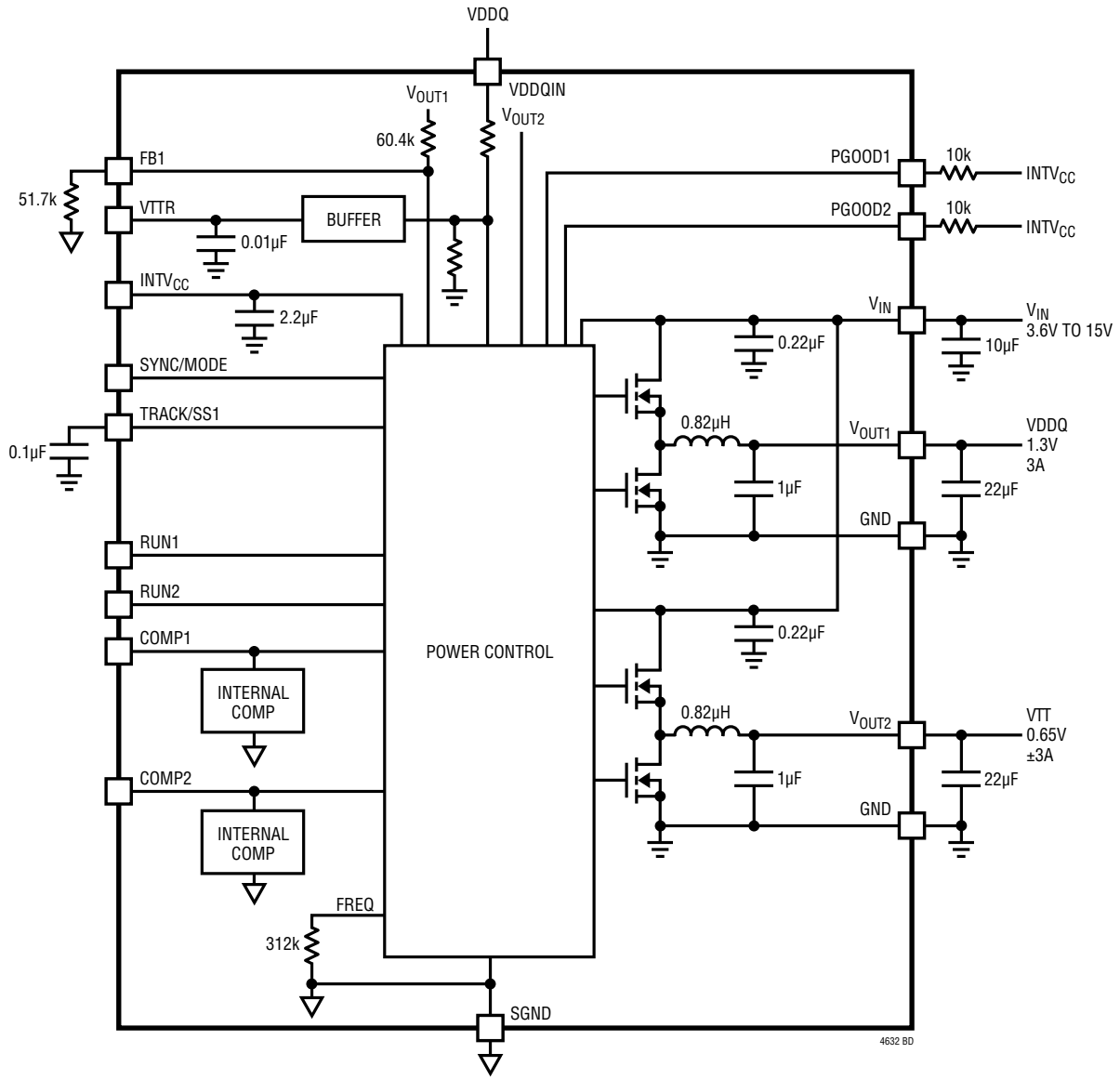
FB1 (E4): The Negative Input of the Error Amplifier for the Channel 1 Switching Mode Regulator. Internally, this pin is connected to V_{OUT1} with a 60.4k precision resistor. Different output voltages can be programmed with an additional resistor between FB1 and GND pins. Connect this pin to $INTV_{CC}$ in Dual Phase Single Output VTT Configuration. See the Applications Information section for details.

TRACK/SS1 (E3): Output Tracking and Soft-Start Pin of the Channel 1 Switching Mode Regulator. It allows the user to control the rise time of the output voltage. Putting a voltage below 0.6V on this pin bypasses the internal reference input to the error amplifier, instead it servos the FB pin to the TRACK/SS voltage. Above 0.6V, the tracking function stops and the internal reference resumes control of the error amplifier. There's an internal 1.2µA pull-up current from $INTV_{CC}$ on this pin, so putting a capacitor here provides a soft-start function.

VTTR (A3): Reference Output. This output is used to supply the VREF voltage for DDR memory. An on-chip buffer amplifier outputs a low noise reference voltage equal to $V_{DDQIN}/2$. This output is capable of supplying 10mA. VTTR has internal 0.01µF capacitor. Additional R-C filter can be used to further reduce the ripple on VTTR. The error amplifier for channel 2 uses this voltage as its reference voltage.

V_{DDQIN} (A4): External Reference Input for Channel 2. An internal resistor divider sets the VTTR pin voltage to be equal to half the voltage applied to this input. Channel 2 uses the VTTR pin voltage as its error amplifier reference.

BLOCK DIAGRAM



DECOUPLING REQUIREMENTS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	External Input Capacitor Requirement (V_{IN} = 3.6V to 15V, V_{OUT} = 1.5V)	I_{OUT} = 3A	4.7	10		µF
C_{OUT}	External Output Capacitor Requirement (V_{IN} = 3.6V to 15V, V_{OUT} = 1.5V)	I_{OUT} = 3A	10	22		µF

OPERATION

The LTM4632 is a dual output standalone non-isolated switch mode DC/DC power supply for DDR-QDR4 SRAM memory supplies and bus termination. It can deliver two output rails which could both sink and source 3A DC current with few external input and output ceramic capacitors, plus a 10mA buffered VTTR (VREF) reference voltage which equal to one half of V_{DDQIN} voltage.

Two or more module outputs can be easily paralleled to achieve a single VTT output with a higher sink and source current capability. Up to 8 phases can be paralleled to run simultaneously with a good current sharing guaranteed by current mode control loop.

This module provides precisely regulated output voltage (V_{OUT1}) programmable via one external resistor from 0.6V to 2.5V over 3.6V to 15V input voltage range. With $INTV_{CC}$ tied to V_{IN}, this module is able to operate from 3.3V input.

The LTM4632 has an integrated a dual constant on-time valley current mode regulator, power MOSFETs, inductor, and other supporting discrete components. The typical switching frequency is internally set to 1MHz. For switching noise-sensitive applications, the µModule can be externally synchronized to a clock within ±30% of the set frequency. See the Applications Information section.

With current mode control and internal feedback loop compensation, the LTM4632 module has sufficient stability margins and good transient performance with a wide range of output capacitors, even with all ceramic output capacitors.

Current mode control provides cycle-by-cycle fast current limiting. An internal overvoltage and undervoltage comparators pull the open-drain PGOOD output low if the output feedback voltage exits a ±8% window around the regulation point. Furthermore, an input overvoltage protection been utilized by shutting down both power MOSFETs when V_{IN} rises above 17.5V to protect internal devices.

Pulling the RUN pin below 1V forces the controller into its shutdown state, turning off both power MOSFETs and most of the internal control circuitry. At light load currents, burst mode operation can be enabled to achieve higher efficiency compared to continuous mode (CCM) by setting MODE pin to $INTV_{CC}$. The TRACK/SS pin is used for power supply tracking and soft-start programming. See the Applications Information section.

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The typical LTM4632 application circuit is shown in Figure 19. External component selection is primarily determined by the input voltage, the output voltage and the maximum load current. Refer to Table 5 for specific external capacitor requirements for a particular application.

V_{IN} to V_{OUT} Step-Down Ratios

There are restrictions in the maximum V_{IN} and V_{OUT} step down ratio that can be achieved for a given input voltage due to the minimum off-time and minimum on-time limits of the regulator. The minimum off-time limit imposes a maximum duty cycle which can be calculated as:

$$D_{MAX} = 1 - t_{OFF(MIN)} \bullet f_{SW}$$

where $t_{OFF(MIN)}$ is the minimum off-time, 45ns typical for LTM4632, and f_{SW} is the switching frequency. Conversely the minimum on-time limit imposes a minimum duty cycle of the converter which can be calculated as

$$D_{MIN} = t_{ON(MIN)} \bullet f_{SW}$$

where $t_{ON(MIN)}$ is the minimum on-time, 20ns typical for LTM4632. In the rare cases where the minimum duty cycle is surpassed, the output voltage will still remain in regulation, but the switching frequency will decrease from its programmed value. Note that additional thermal derating may be applied. See the Thermal Considerations and Output Current Deratingand section in this data sheet.

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Channel 1 Output Voltage Programming (Configured as VDDQ)

The PWM controller for the V_{OUT1} has an internal 0.6V reference voltage. As shown in the Block Diagram, a 60.4k internal feedback resistor connects V_{OUT1} and FB1 pins together. Adding a resistor R_{FB} from FB1 pin to GND programs the output voltage:

$$R_{FB} = \frac{0.6V}{V_{OUT} - 0.6V} \bullet 60.4k$$

Table 1. V_{FB} Resistor Table (1%) vs Various Output Voltages

V_{OUT}(V)	0.6	1.0	1.2	1.3	1.5	1.8	2.5
R_{FB}(k)	OPEN	90.9	60.4	52.3	40.2	30.1	19.1

Channel 2 Output Voltage Programming (Configured as VTT)

The PWM controller for the V_{OUT2} uses VTTR voltage as a reference voltage. V_{OUT2} is directly connected to the negative side of the error compiler to internally program V_{OUT2} to equal to VTTR voltage, which equals to one half of V_{DDQIN} voltage.

$$V_{OUT2} = VTTR = V_{DDQIN}/2$$

In a complete DDR memory power application which require both VDDQ supply and VTT terminal outputs, configure LTM4632 Channel 1 as VDDQ output by adding a feed-back resistor from FB1 pin to GND. Feed V_{OUT1} (VDDQ output) voltage to V_{DDQIN} pin to program Channel 2 as VTT output which equals half of the Channel 1 (VDDQ output) voltage.

Input Decoupling Capacitors

The LTM4632 module should be connected to a low AC-impedance DC source. For each regulator channel, one piece 4.7µF input ceramic capacitor is required for RMS ripple current decoupling. Bulk input capacitor is only needed when the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. The bulk capacitor can be an electrolytic aluminum capacitor and polymer capacitor.

Without considering the inductor current ripple, for each output, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1-D)}$$

where $\eta\%$ is the estimated efficiency of the power module.

Output Decoupling Capacitors

With an optimized high frequency, high bandwidth design, only single piece of 22µF low ESR output ceramic capacitor is required for each LTM4632 output to achieve low output voltage ripple and very good transient response. Additional output filtering may be required by the system designer, if further reduction of output ripples or dynamic transient spikes is required. Table 5 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 0.75A (25%) load step transient. Multiphase operation will reduce effective output ripple as a function of the number of phases. Application Note 77 discusses this noise reduction versus output ripple current cancellation, but the output capacitance will be more a function of stability and transient response. The Linear Technology LTpowerCAD Design Tool is available to download online for output ripple, stability and transient response analysis and calculating the output ripple reduction as the number of phases implemented increases by N times.

Burst Mode Operation

In applications where high efficiency at intermediate current are more important than output voltage ripple, burst mode operation could be used on Channel 1 by connecting SYNC/MODE pin to $INTV_{CC}$ to improve light load efficiency. In Burst Mode operation, a current reversal comparator (IREV) detects the negative inductor current and shuts off the bottom power MOSFET, resulting in discontinuous operation and increased efficiency. Both power MOSFETs will remain off and the output capacitor will supply the load current until the COMP voltage rises above the zero current level to initiate another cycle.

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Force Continuous Current Mode (CCM) Operation

In applications where fixed frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, forced continuous operation should be used. Forced continuous operation can be enabled by tying the SYNC/MODE pin to GND. In this mode, inductor current is allowed to reverse during low output loads, the COMP voltage is in control of the current comparator threshold throughout, and the top MOSFET always turns on with each oscillator pulse. During start-up, forced continuous mode is disabled and inductor current is prevented from reversing until the LTM4632's output voltage is in regulation.

Operating Frequency

The operating frequency of the LTM4632 is optimized to achieve the compact package size and the minimum output ripple voltage while still keeping high efficiency. The default operating frequency is internally set to 1MHz. In most applications, no additional frequency adjusting is required.

Frequency Synchronization

The power module has a phase-locked loop comprised of an internal voltage controlled oscillator and a phase detector. This allows the internal top MOSFET turn-on to be locked to the rising edge of the external clock. The external clock frequency range must be within ±30% around the set operating frequency. A pulse detection circuit is used to detect a clock on the SYNC/MODE pin to turn on the phase locked loop. The pulse width of the clock has to be at least 100ns. The clock high level must be above 2V and clock low level below 0.3V. The presence of an external clock will place both regulator channels into forced continuous mode operation. During the start-up of the regulator, the phase-locked loop function is disabled.

Multiphase Operation (Configured as Multiphase Single Output VTT)

For VTT termination output loads that demand more than 3A of current, two outputs in the LTM4632 or even multiple LTM4632s can be paralleled to run out of phase to provide a multiphase single output VTT termination supply capable of souring and sinking higher current.

The two switching mode regulator channels inside the LTM4632 are internally set to operate 180° out of phase. Multiple LTM4632s could easily operate 90 degrees, 60 degrees or 45 degrees shift which corresponds to 4-phase, 6-phase or 8-phase operation by letting SYNC/MODE of the LTM4632 synchronize to an external multiphase oscillator like LTC6902. Figure 2 shows a 4-phase single output VTT termination supply design example for clock phasing.

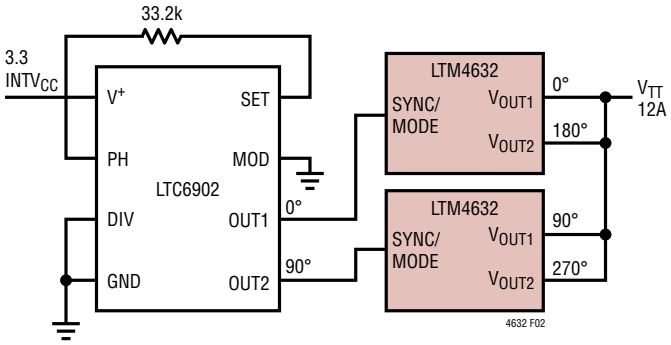

Figure 2. Example of Clock Phasing for 4-Phase Single Output VTT Operation with LTC6902

Tie FB1 pin of the LTM4632 to its $INTV_{CC}$ pin to put the module into two phase single VTT output operation mode. This will internally switch the Channel 1 error amplifier reference voltage from 0.6V to VTTR voltage, which is the same as Channel 2. Repeat this for each LTM4632 module in multiple LTM4632s paralleling application.

Also tie RUN, TRACK/SS and COMP pin of each paralleling channel together. Figure 20 shows an example of paralleled multiphase single output VTT termination supply operation and pin connection.

The LTM4632 device is an inherently current mode controlled device, so parallel modules will have very good current sharing. This will balance the thermals on the design.

Multiphase Operation (Configured as VDDQ+VTT)

For application which both VDDQ and VTT termination output loads demand more than 3A of current, two or multiple Channel 1 outputs from different LTM4632 modules can be easily paralleled to provide a multiphase single VDDQ output while Channel 2 outputs from different LTM4632 modules can paralleled to provide a multiphase single VTT output.

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In this case, multiple LTM4632s should be setup to operate 180 degrees, 120 degrees or 90 degrees shift which corresponds to 2-phase, 3-phase or 4-phase operation by letting SYNC/MODE of the LTM4632 synchronize to an external multiphase oscillator like LTC6902.

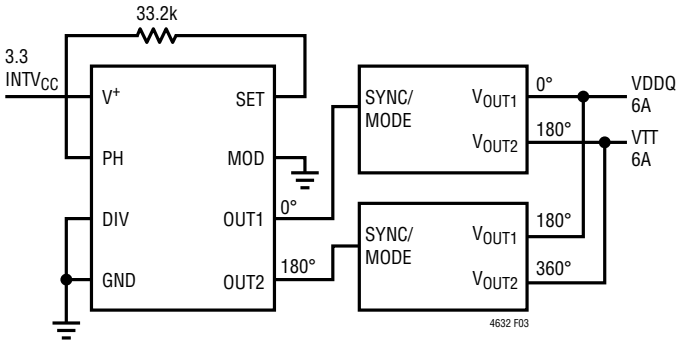

Figure 3. Example of Clock Phasing for 2-Phase VDDQ Plus 2-Phase VTT Operation with LTC6902

Tie RUN1, TRACK/SS1 FB1 and COMP1 pin of each paralleling module together for VDDQ output. Tie RUN2, V_{DDQIN}, FB2 and COMP2 pin of each paralleling module together for VTT output. Figure 22 shows an example of two LTM4632 get paralleled to provide 6A VDDQ and 6A VTT termination supply.

Input and Output RMS Ripple Current Cancellation

A multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is reduced by, and the effective ripple frequency is multiplied by, the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by the number of phases used when all of the outputs are tied together to achieve a single high output current design.

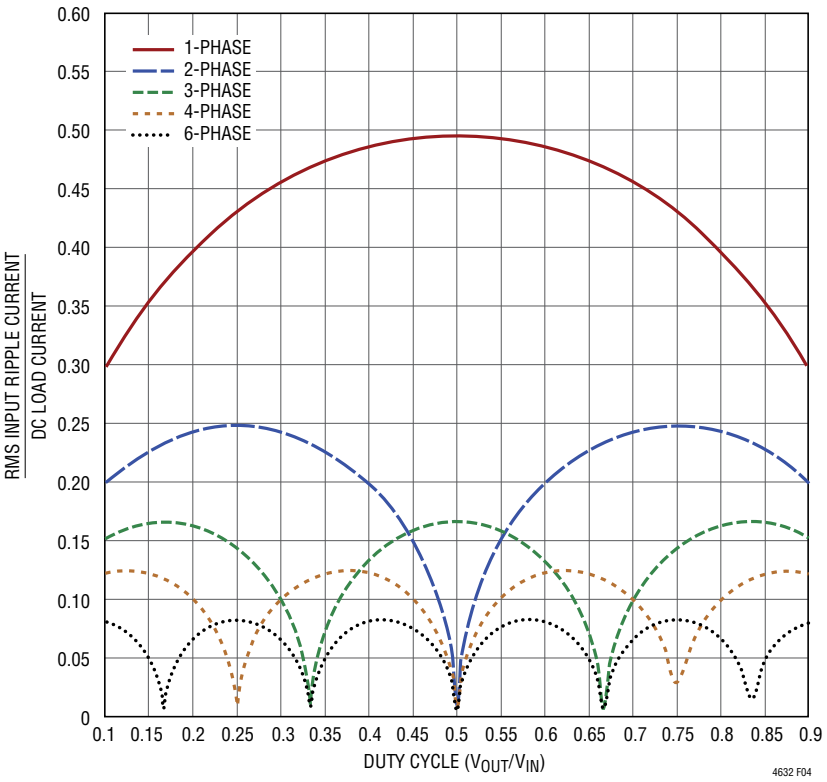

Figure 4. Input RMS Current Ratios to DC Load Current as a Function of Duty Cycle

APPLICATIONS INFORMATION

Application Note 77 provides a detailed explanation of multiphase operation. The input RMS ripple current cancellation mathematical derivations are presented, and a graph is displayed representing the RMS ripple current reduction as a function of the number of interleaved phases. Figure 4 shows this graph.

Channel 1 Output Voltage Tracking and Soft-Start

The TRACK/SS pin provides a means to either soft-start the Channel 1 regulator or track it to a different power supply. A capacitor on the TRACK/SS pin will program the ramp rate of the channel 1 output voltage. An internal 1.2µA current source will charge up the external soft-start capacitor towards $INTV_{CC}$ voltage. When the TRACK/SS voltage is below 0.6V, it will take over the internal 0.6V reference voltage to control the output voltage. The total soft-start time can be calculated as:

$$t_{SS} = 0.6 \bullet \frac{C_{SS}}{1.2\mu A}$$

where C_{SS} is the capacitance on the TRACK/SS pin. Forced continuous mode are disabled during the soft-start process.

Channel 1 output voltage tracking can also be programmed externally using the TRACK/SS pin. The output can be tracked up and down with another regulator. Figure 5 and Figure 6 show an example waveform and schematic of a Ratiometric tracking where the slave regulator's output slew rate is proportional to the master's.

Since the slave regulator's TRACK/SS is connected to the master's output through a $R_{TR(TOP)}/R_{TR(BOT)}$ resistor divider and its voltage used to regulate the slave output voltage when TRACK/SS voltage is below 0.6V, the slave output voltage and the master output voltage should satisfy the following equation during the start-up.

$$V_{OUT(SL)} \bullet \frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k} = V_{OUT(MA)} \bullet \frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}$$

The $R_{FB(SL)}$ is the feedback resistor and the $R_{TR(TOP)}/R_{TR(BOT)}$ is the resistor divider on the TRACK/SS pin of the slave regulator, as shown in Figure 6.

Following the upper equation, the master's output slew rate (MR) and the slave's output slew rate (SR) in Volts/Time is determined by:

$$\frac{MR}{SR} = \frac{\frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k}}{\frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}}$$

For example, $V_{OUT(MA)}$ = 1.5V, MR = 1.5V/1ms and $V_{OUT(SL)}$ = 1.2V, SR = 1.2V/1ms. From the equation, we could solve out that $R_{TR(TOP)}$ = 60.4k and $R_{TR(BOT)}$ = 40.2k is a good combination for the Ratiometric tracking.

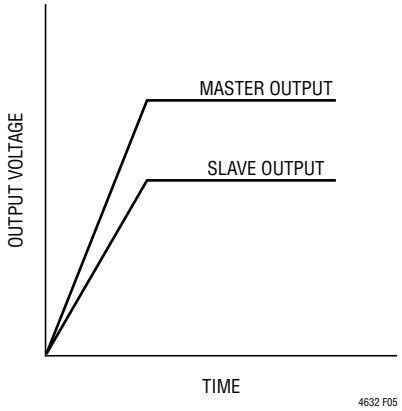

Figure 5. Output Ratiometric Tracking Waveform

The TRACK pins will have the 1.2µA current source on when a resistive divider is used to implement tracking on that specific channel. This will impose an offset on the TRACK pin input. Smaller values resistors with the same ratios as the resistor values calculated from the above equation can be used. For example, where the 60.4k is used then a 6.04k can be used to reduce the TRACK pin offset to a negligible value.

The Coincident output tracking can be recognized as a special Ratiometric output tracking which the master's output slew rate (MR) is the same as the slave's output slew rate (SR), as waveform shown in Figure 7.

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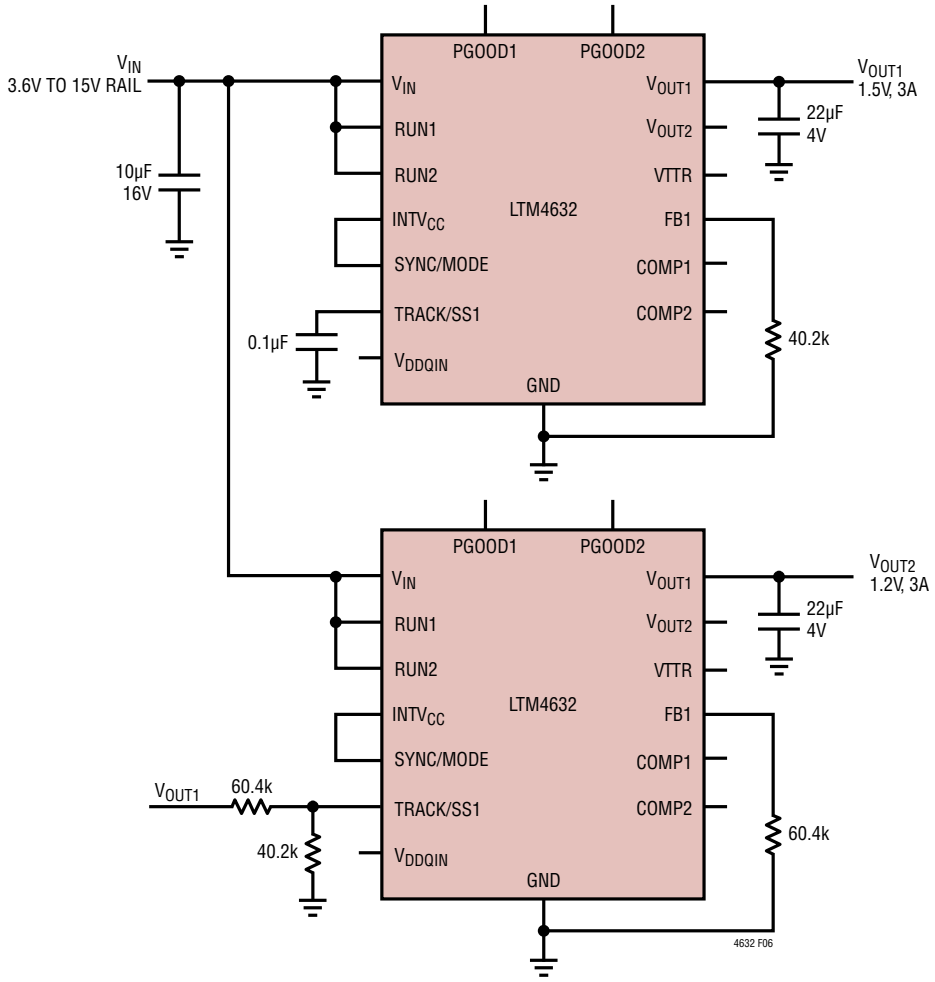

Figure 6. Example Schematic of Ratiometric Output Voltage Tracking

From the equation, we could easily find out that, in the Coincident tracking, the slave regulator's TRACK/SS pin resistor divider is always the same as its feedback divider.

$$\frac{R_{FB(SL)}}{R_{FB(SL)}+60.4k}=\frac{R_{TR(BOT)}}{R_{TR(TOP)}+R_{TR(BOT)}}$$

For example, $R_{TR(TOP)}$ = 60.4k and $R_{TR(BOT)}$ = 60.4k is a good combination for Coincident tracking for $V_{OUT(MA)}$ = 1.5V and $V_{OUT(SL)}$ = 1.2V application.

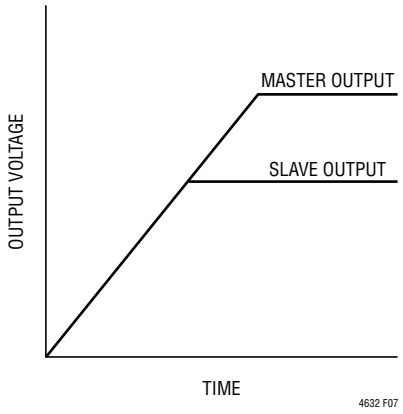

Figure 7. Output Coincident Tracking Waveform

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Power Good

The PGOOD pins are open drain pins that can be used to monitor valid output voltage regulation. This pin monitors a ±8% window around the regulation point. A resistor can be pulled up to a particular supply voltage for monitoring. To prevent unwanted PGOOD glitches during transients or dynamic V_{OUT} changes, the LTM4632's PGOOD falling edge includes a blanking delay of approximately 40µs.

Stability Compensation

The LTM4632 module internal compensation loop is de-signed and optimized for low ESR ceramic output capacitors only application. Table 5 is provided for most application requirements. The LTpowerCAD Design Tool is available to download for control loop analysis for further optimization.

RUN Enable

Pulling the RUN pin to ground forces the LTM4632 into its shutdown state, turning off both power MOSFETs and most of its internal control circuitry. Tying the RUN pin voltage above 1.28V will turn on the entire chip.

Low Input Application

The LTM4632 is capable to run from 3.3V input when the V_{IN} pin is tied to $INTV_{CC}$ pin. See Figure 21 for the application circuit. Please note the $INTV_{CC}$ pin has 3.6V ABS max voltage rating.

Pre-Biased Output Start-Up (Channel 1)

There may be situations that require the power supply to start up with a pre-bias on the output capacitors. In this case, it is desirable to start up without discharging that output pre-bias. The LTM4632 channel 1 can safely power up into a pre-biased output without discharging it.

The LTM4632 accomplishes this by forcing discontinuous mode (DCM) operation until the TRACK/SS1 pin voltage reaches 80% of the 0.6V reference voltage for channel 1. This will prevent the BG from turning on during the pre-biased output start-up which would discharge the output. Do not pre-bias LTM4632 with a voltage higher than $INTV_{CC}$ (3.3V) voltage.

Overtemperature Protection

The internal overtemperature protection monitors the junction temperature of the module. If the junction temperature reaches approximately 170°C, both power switches will be turned off until the temperature drops about 10°C cooler.

Input Overvoltage Protection

In order to protect the internal power MOSFET devices against transient voltage spikes, the LTM4632 constantly monitors each V_{IN} pin for an overvoltage condition. When V_{IN} rises above 17.5V, the regulator suspends operation by shutting off both power MOSFETs on the corresponding channel. Once V_{IN} drops below 16.5V, the regulator immediately resumes normal operation. The regulator executes its soft-start function when exiting an overvoltage condition.

Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD51-9 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation per-formed on a µModule package mounted to a hardware test board—also defined by JESD51-9 ("Test Boards for Area Array Surface Mount Package Thermal Measurements"). The motivation for providing these thermal coefficients in found in JESD51-12 ("Guidelines for Reporting and Using Electronic Package Thermal Information").

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to anticipate the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are in-and-of themselves not relevant to providing guidance of thermal performance; instead, the derating curves provided in the data sheet can be used in a manner that yields insight and guidance pertaining to one's application-usage, and can be adapted to correlate thermal performance to one's own application.

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The Pin Configuration section typically gives four thermal coefficients explicitly defined in JESD 51-12; these coefficients are quoted or paraphrased below:

1. θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.

2. $\theta_{JCbottom}$, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.

3. θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

4. θ_{JB}, the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two sided, two layer board. This board is described in JESD 51-9.

A graphical representation of the aforementioned thermal resistances is given in Figure 8; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule package.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule package as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package–granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within a SIP (system-in-package) module, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity–but also, not ignoring practical realities–an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the µModule and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD51-12 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the µModule with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same

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power loss as that which was simulated. The outcome of this process and due diligence yields the set of derating curves provided in other sections of this data sheet. After these laboratory test have been performed and correlated to the µModule model, then the θ_{JB} and θ_{BA} are summed together to correlate quite well with the µModule model with no airflow or heat sinking in a properly define chamber. This $\theta_{JB} + \theta_{BA}$ value is shown in the Pin Configuration section and should accurately equal the θ_{JA} value because approximately 100% of power loss flows from the junction through the board into ambient with no airflow or top mounted heat sink.

The 1.0V, 1.5V, and 2.5V power loss curves in Figure 9 to 11 can be used in coordination with the load current derating curves in Figure 12 troughout Figure 17 for calculating an approximate θ_{JA} thermal resistance for the LTM4632 with no heat sinking and various airflow conditions. The power loss curves are taken at room temperature, and are increased with multiplicative factors of 1.35 assuming junction temperature at 120°C. The derating curves are plotted with the output current starting at 6A by putting LTM4632 into two phase single output setup (Figure 20) and the ambient temperature at 40°C. These output voltages are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 120°C maximum while lowering output current or power with increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example in Figure 12 the load current is derated to ~3A at ~100°C with no air or heat sink and the power loss for the 5V to 1V at 3A output is about 0.95W. The 0.95W loss is calculated with the ~0.7W room temperature loss from the 5V to 1V power loss curve at 3A, and the 1.35 multiplying factor at 120°C measured junction temperature. If the 100°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 20°C divided by 0.95W equals a 20°C/W θ_{JA} thermal resistance. Table 2 specifies a 19°C~20°C/W value which is very close. Table 2 to 4 provide equivalent thermal resistances for 1.0V, 1.5V, and 2.5V outputs with and without airflow. The derived thermal resistances in Table 2 to 4 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with the above ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick four layer board with two ounce copper for the two outer layers and one ounce copper for the two inner layers. The PCB dimensions are 95mm × 76mm.

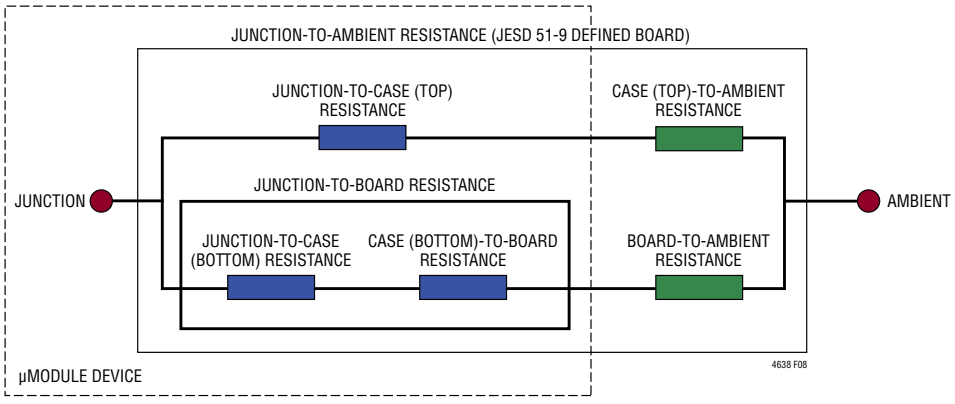

Figure 8. Graphical Representation of JESD51-12 Thermal Coefficients

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Figure 9. 1.0V Output Power Loss

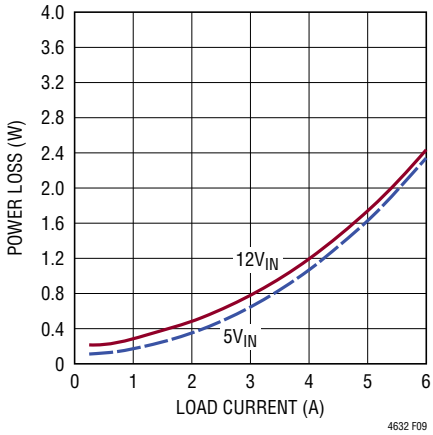


Figure 10. 1.5V Output Power Loss

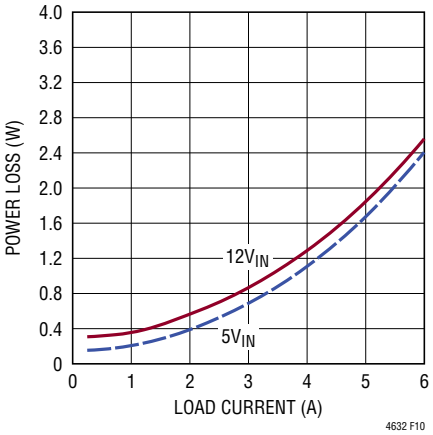


Figure 11. 2.5V Output Power Loss

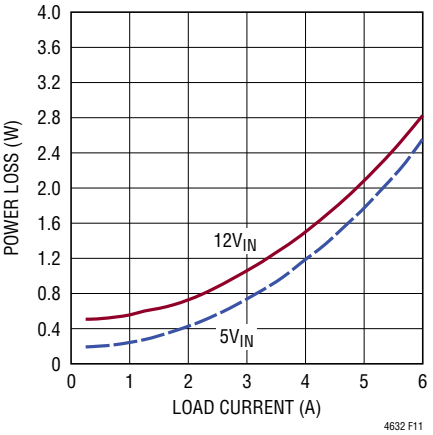


Figure 12. 5V to 1.0V Derating Curve, No Heat Sink

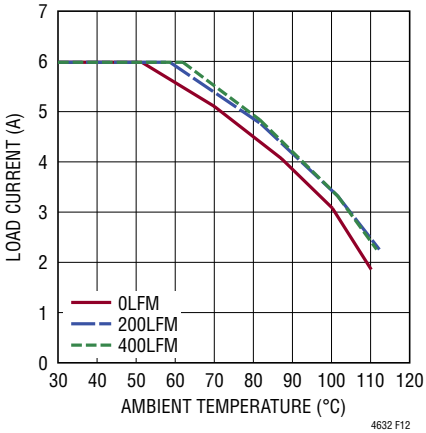


Figure 13. 12V to 1.0V Derating Curve, No Heat Sink

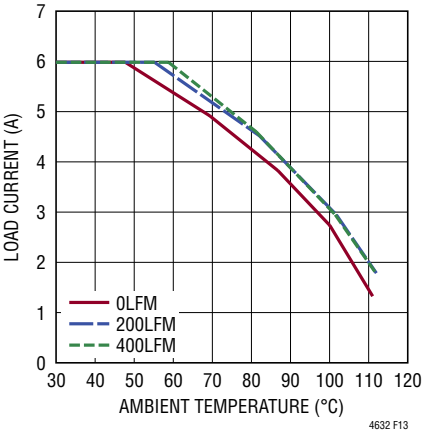


Figure 14. 5V to 1.5V Derating Curve, No Heat Sink

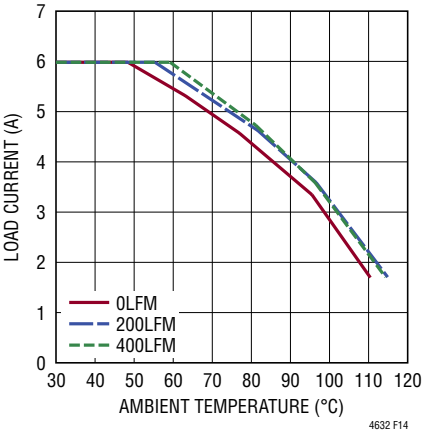


Figure 15. 12V to 1.5V Derating Curve, No Heat Sink

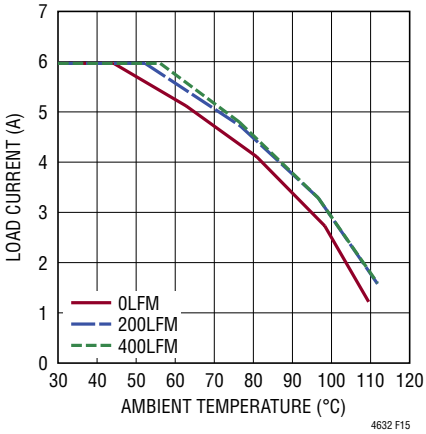


Figure 16. 5V to 2.5V Derating Curve, No Heat Sink

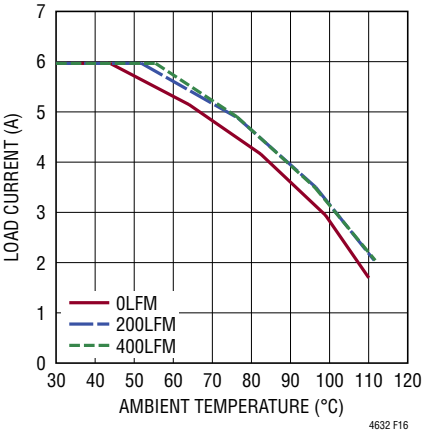
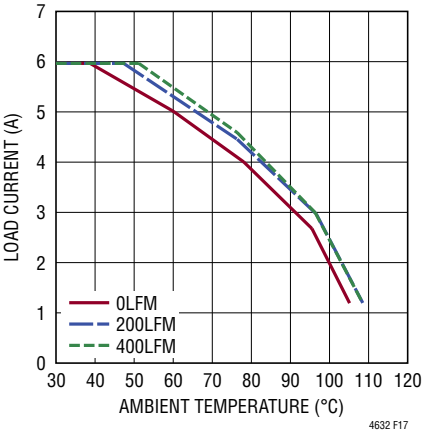


Figure 17. 12V to 2.5V Derating Curve, No Heat Sink



APPLICATIONS INFORMATION

Table 2. 1.0V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 12, Figure 13	5, 12	Figure 9	0	None	19 to 20
Figure 12, Figure 13	5, 12	Figure 9	200	None	18 to 19
Figure 12, Figure 13	5, 12	Figure 9	400	None	17 to 18

Table 3. 1.5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 14, Figure 15	5, 12	Figure 10	0	None	19 to 20
Figure 14, Figure 15	5, 12	Figure 10	200	None	18 to 19
Figure 14, Figure 15	5, 12	Figure 10	400	None	17 to 18

Table 4. 2.5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 16, Figure 17	5, 12	Figure 11	0	None	19 to 20
Figure 16, Figure 17	5, 12	Figure 11	200	None	18 to 19
Figure 16, Figure 17	5, 12	Figure 11	400	None	17 to 18

APPLICATIONS INFORMATION

Table 5. Output Voltage Response for Each Regulator Channel vs Component Matrix (Refer to Figure 19)
25% Load Step Typical Measured Values

C_{IN} (CERAMIC)	PART NUMBER	VALUE	C_{OUT1} (CERAMIC)	PART NUMBER	VALUE	C_{OUT2} (BULK)	PART NUMBER	VALUE
Murata	GRM188R61E475KE11#	4.7µF, 25V, 0603, X5R	Murata	GRM21R60J476ME15#	47µF, 6.3V, 0805, X5R	Panasonic	6TPC150M	150µF, 6.3V 3.5 × 2.8 × 1.4mm
Murata	GRM188R61E106MA73#	10µF, 25V, 0603, X5R	Murata	GRM188R60J226MEA0#	22µF, 6.3V, 0603, X5R			
Taiyo Yuden	TMK212BJ475KG-T	4.7µF, 25V, 0805, X5R	Taiyo Yuden	JMK212BJ476MG-T	47µF, 6.3V, 0805, X5R			

V_{OUT} (V)	C_{IN} (CERAMIC) (µF)	C_{IN} (BULK)	C_{OUT1} (CERAMIC) (µF)	C_{OUT2} (BULK) (µF)	C_{FF} (pF)	V_{IN} (V)	DROOP (mV)	P-P DERIVATION (mV)	RECOVERY TIME (µS)	LOAD STEP (A)	LOAD STEP SLEW RATE (A/µS)	R_{FB} (kΩ)
1	2 × 10	0	1 × 47µF	0	0	5, 12	0	77	15	0.75	10	90.9
1.2	2 × 10	0	1 × 47µF	0	0	5, 12	0	83	15	0.75	10	60.4
1.5	2 × 10	0	1 × 47µF	0	0	5, 12	0	94	18	0.75	10	40.2
1.8	2 × 10	0	1 × 47µF	0	0	5, 12	0	105	20	0.75	10	30.1
2.5	2 × 10	0	1 × 47µF	0	0	5, 12	0	138	20	0.75	10	19.1

APPLICATIONS INFORMATION

SAFETY CONSIDERATIONS

The LTM4632 modules do not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure. The device does support thermal shutdown and over current protection.

LAYOUT CHECKLIST/EXAMPLE

The high integration of LTM4632 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{IN}, GND, V_{OUT1} and V_{OUT2}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, PGND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put via directly on the pad, unless they are capped or plated over.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.
- For parallel modules, tie the V_{OUT}, V_{FB}, and COMP pins together. Use an internal layer to closely connect these pins together. The TRACK pin can be tied a common capacitor for regulator soft-start.
- Bring out test points on the signal pins for monitoring.

Figure 18 gives a good example of the recommended layout.

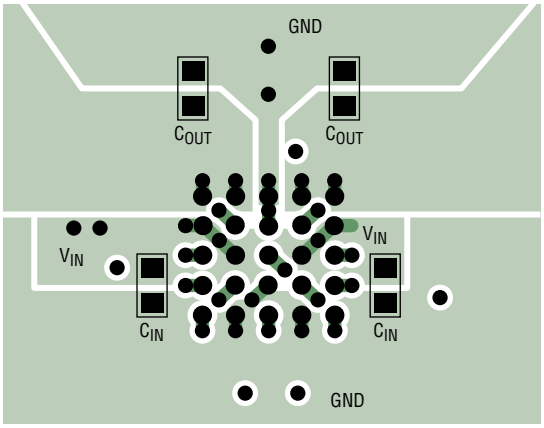


Figure 18. Recommend PCB Layout

APPLICATIONS INFORMATION

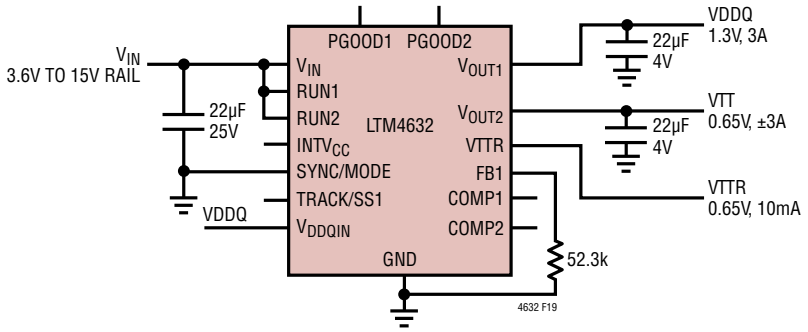


Figure 19. 3.6V to 15V Input, 1.3V/3A VDDQ, 0.65V/±3A VTT and 10mA VTTR Design

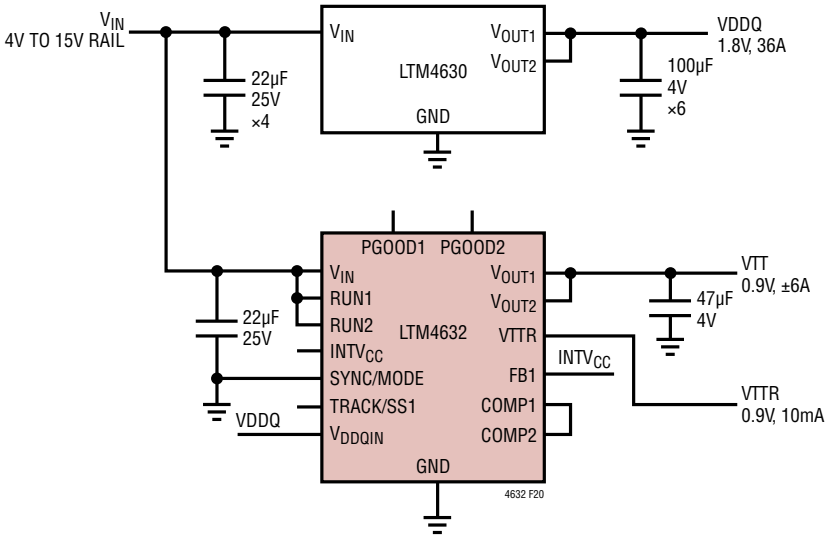


Figure 20. 4V to 15V Input, Two Phase Single Output ±6A VTT Termination Design with LTM4630 36A VDDQ Supply

APPLICATIONS INFORMATION

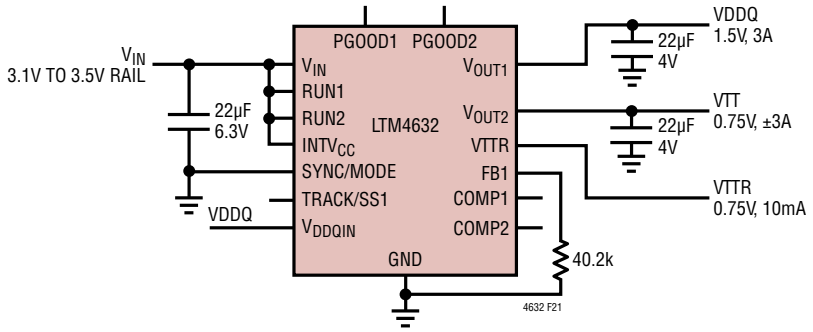


Figure 21. 3.3V Input, 1.5V/3A VDDQ, 0.75V/±3A VTT and 10mA VTTR Design

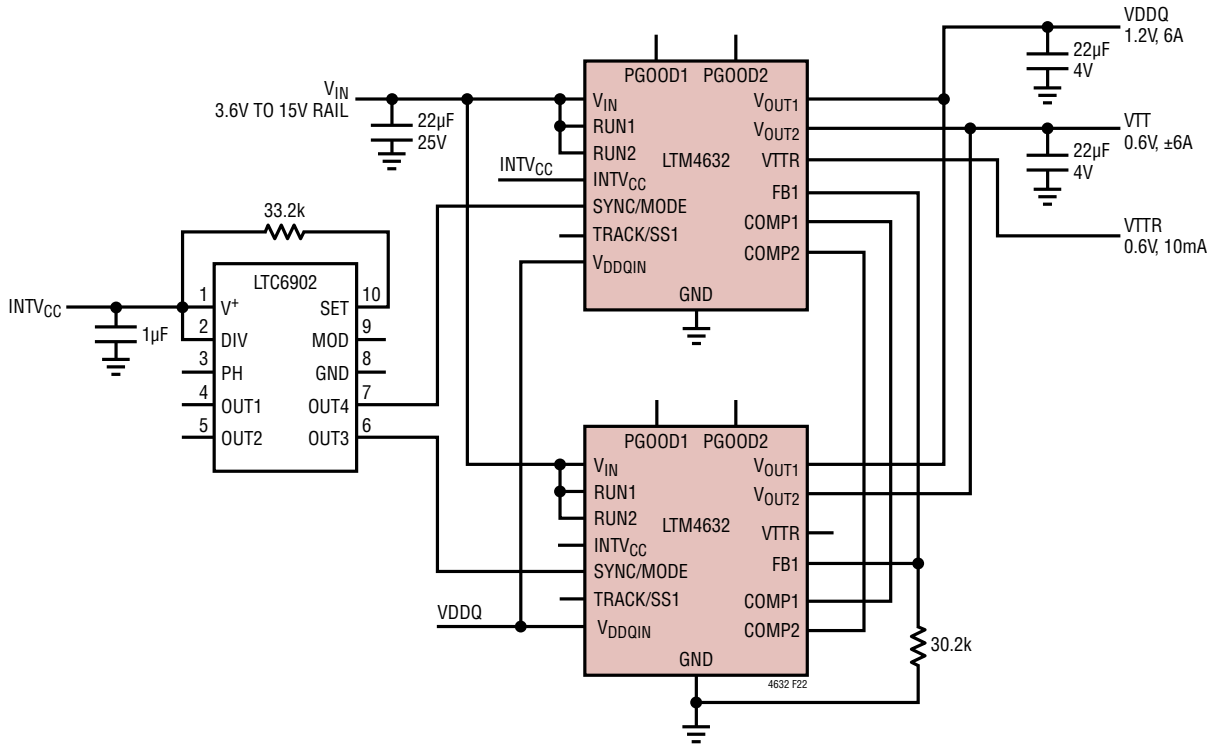


Figure 22. Two Module in Parallel, 3.6V to 15V Input, 1.2V/6A VDDQ, 0.6V/±6A VTT and 10mA VTTR Design

PACKAGE DESCRIPTION

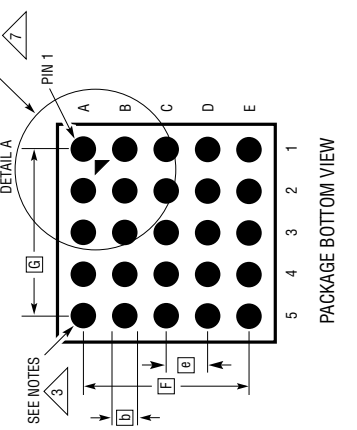
PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

LTM4632 Component LGA and BGA Pinout

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	V_{OUT2}	A2	V_{IN}	A3	VTTR	A4	V_{DDQIN}	A5	COMP2
B1	V_{OUT2}	B2	RUN2	B3	V_{IN}	B4	PGOOD2	B5	GND
C1	GND	C2	GND	C3	$INTV_{CC}$	C4	SGND	C5	SYNC/MODE
D1	V_{OUT1}	D2	RUN1	D3	V_{IN}	D4	PGOOD1	D5	GND
E1	V_{OUT1}	E2	V_{IN}	E3	TRACK/SS1	E4	FB1	E5	COMP1

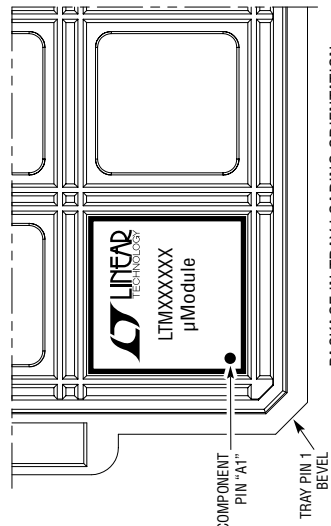
PACKAGE DESCRIPTION

LGA Package
25-Lead (6.25mm × 6.25mm × 1.82mm)
(Reference LTC DWG # 05-08-1949 Rev Ø)



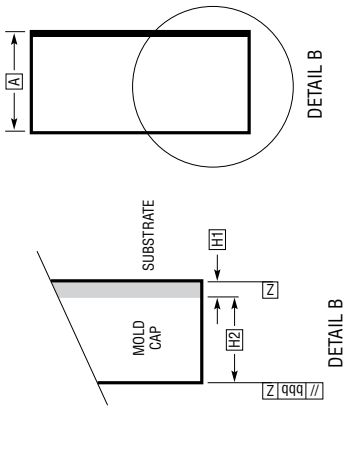
PACKAGE BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. LAND DESIGNATION PER JESD MO-222, SPP-010
4. DETAILS OF PAD #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PAD #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. THE TOTAL NUMBER OF PADS: 25
7. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY

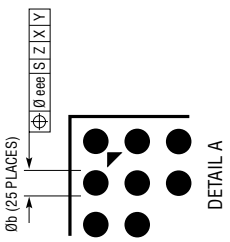


PACKAGE IN TRAY LOADING ORIENTATION

LGA 25 0613 REV Ø



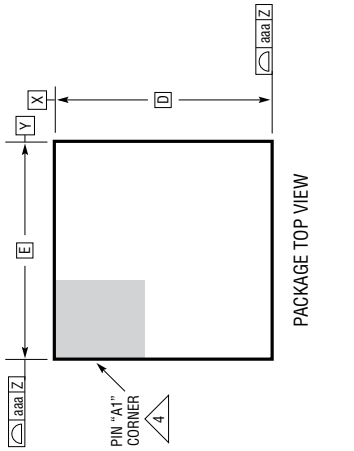
DETAIL B



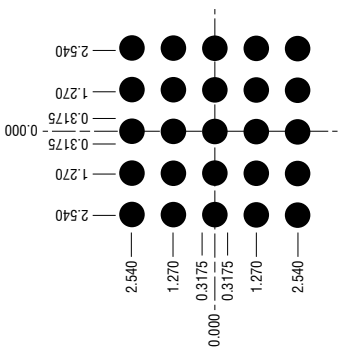
DETAIL A

DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	1.72	1.82	1.92	
b	0.60	0.63	0.66	
D		6.25		
E		6.25		
e		1.27		
F		5.08		
G		5.08		
H1	0.27	0.32	0.37	
H2	1.45	1.50	1.55	
aaa			0.15	
bbb			0.10	
eee			0.15	

TOTAL NUMBER OF LGA PADS: 25



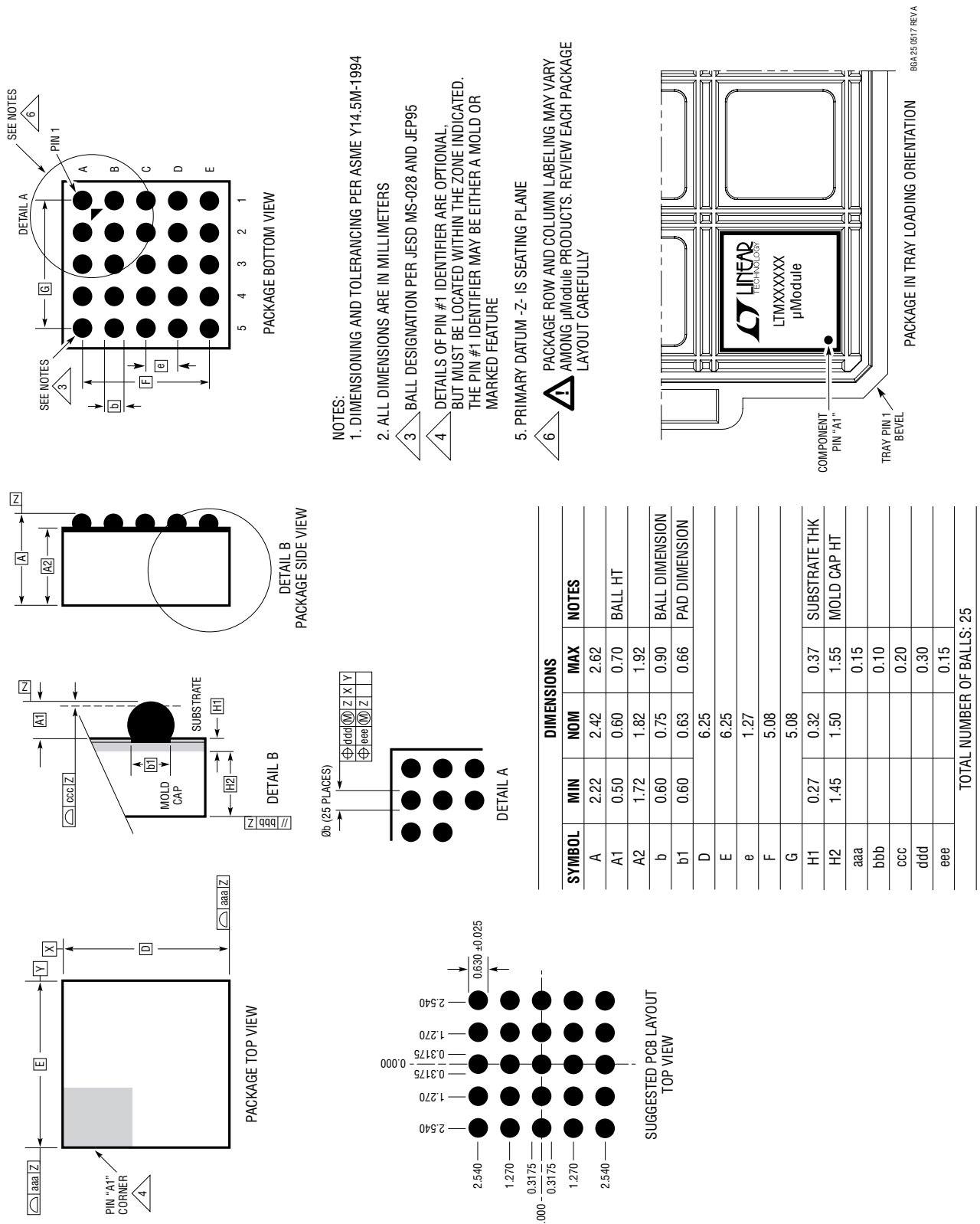
PACKAGE TOP VIEW



SUGGESTED PCB LAYOUT
TOP VIEW

PACKAGE DESCRIPTION

BGA Package
25-Lead (6.25mm × 6.25mm × 2.42mm)
(Reference LTC DWG # 05-08-1502 Rev A)

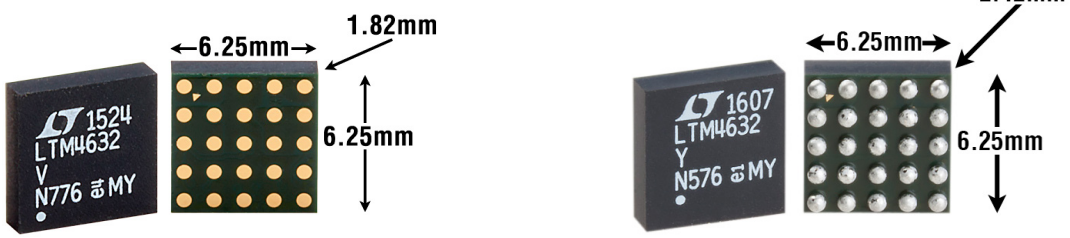


DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	2.22	2.42	2.62	
A1	0.50	0.60	0.70	BALL HT
A2	1.72	1.82	1.92	
b	0.60	0.75	0.90	BALL DIMENSION
b1	0.60	0.63	0.66	PAD DIMENSION
D		6.25		
E		6.25		
e		1.27		
F		5.08		
G		5.08		
H1	0.27	0.32	0.37	SUBSTRATE THK
H2	1.45	1.50	1.55	MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
TOTAL NUMBER OF BALLS: 25				

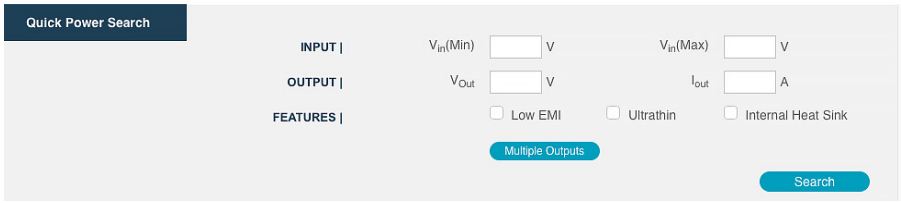
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	05/16	Added BGA package	1, 2, 26
B	09/16	Corrected equations of tracking start-up time from $R_{TR(TOP)}/[R_{TR(TOP)} + R_{TR(BOT)}]$ to $R_{TR(BOT)}/[R_{TR(TOP)} + R_{TR(BOT)}]$	13, 14
C	05/17	Changed VDDQ to 1.3V/3A and VTT to 0.65V	22
D	08/18	PGOOD1 and PGOOD2 were separated on Figure 20	22

PACKAGE PHOTO



DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. 	
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4622	Ultrathin, Dual 2.5A or Single 5A Step-Down µModule Regulator	3.6V < V_{IN} < 20V, 0.6V < V_{OUT} < 5.5V, 6.25mm × 6.25mm × 1.82mm LGA Package, 6.25mm × 6.25mm × 2.42 BGA Package
LTM4623	Ultrathin, Single 3A Step-Down µModule Regulator	4V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 5.5V, 6.25mm × 6.25mm × 1.82mm LGA Package, 6.25mm × 6.25mm × 2.42 BGA Package
LTM4644	Quad 4A Step-Down µModule Regulator	4V < V_{IN} < 14V, 0.6V < V_{OUT} < 5.5V, 9mm × 15mm × 5.01mm BGA Package
LTM4630	µModule Regulator for Higher Power VDDQ Supply	4.5V < V_{IN} < 15V, 0.6V <V_{OUT} <1.8V, Single 36A or Dual 18A, 16mm × 16mm × 5.01mm BGA Package, 16mm × 16mm × 4.41mm LGA Package
LTM4650	µModule Regulator for High Power FPGA/ASIC Core Supply	4.5V < V_{IN} < 15V, 0.6V <V_{OUT} <1.8V, Single 50A or Dual 25A, 16mm × 16mm × 5.01mm BGA Package
LTM4639	Low Input Voltage, Single 20A Step-Down µModule Regulator	2.375V < V_{IN} < 7V, 0.6V < V_{OUT} < 5.5V, 15mm × 15mm × 4.92mm BGA Package
LTM4675	µModule Regulator with PSM for High Power, High Accuracy FPGA/ASIC Core Supply	DC/DC µModule with Digital Power System Management, 4.5V < V_{IN} < 17V, 0.5V < V_{OUT} < 5.5V with ±0.5% Accuracy, Single 18A or Dual 9A
LTM4677	µModule Regulator with PSM for High Power, High Accuracy FPGA/ASIC Core Supply	DC/DC µModule with Digital Power System Management, 4.5V < V_{IN} < 16V, 0.5V < V_{OUT} < 1.8V with ±0.5% Accuracy, Single 36A or Dual 18A
LTC3717	Step-Down Controller for VTT for DDR Memory Termination	4V < V_{IN} < 36V, I_{OUT} = ±20A, Requires External Inductor and MOSFET
LTC6902	Multiphase Oscillator for Multiphase Operation	2-, 3- or 4-Phase, 5kHz to 20MHz Frequency Range