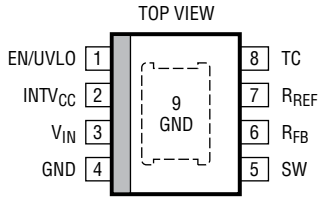
ABSOLUTE MAXIMUM RATINGS

(Note 1)

SW (Note 2) 65V
V_{IN} 42V
EN/UVLO ..... V_{IN}
R_{FB} ..... V_{IN} – 0.5V to V_{IN}
Current Into R_{FB} 200µA
$INTV_{CC}$, R_{REF}, TC 4V
Operating Junction Temperature Range (Notes 3, 4)
LT3002E, LT3002I ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



S8E PACKAGE
8-LEAD PLASTIC SO

θ_{JA} = 33°C/W
EXPOSED PAD (PIN 9) IS GND,
MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3002ES8E#PBF	LT3002ES8E#TRPBF	3002	8-Lead Plastic SO	–40°C to 125°C
LT3002IS8E#PBF	LT3002IS8E#TRPBF	3002	8-Lead Plastic SO	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V, $V_{EN/UVLO}$ = V_{IN}, C_{INTVCC} = 1µF to GND, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	V_{IN} Voltage Range			4		36	V
I_Q	V_{IN} Quiescent Current	$V_{EN/UVLO}$ = 0.2V Active Mode			0.5 380	2	µA µA
	EN/UVLO Shutdown Threshold	For Lowest Off I_Q		0.2	0.75		V
	EN/UVLO Enable Threshold	Falling		1.178	1.214	1.250	V
	EN/UVLO Enable Hysteresis				14		mV
I_{HYS}	EN/UVLO Hysteresis Current	$V_{EN/UVLO}$ = 1.1V $V_{EN/UVLO}$ = 1.3V		2.3 –0.1	2.5 0	2.7 0.1	µA µA
V_{INTVCC}	$INTV_{CC}$ Regulation Voltage	I_{INTVCC} = 0mA to 10mA		2.85	3	3.1	V
I_{INTVCC}	$INTV_{CC}$ Current Limit	V_{INTVCC} = 2.8V		10	13	20	mA
	$INTV_{CC}$ UVLO Threshold	Falling		2.39	2.47	2.55	V
	$INTV_{CC}$ UVLO Hysteresis				105		mV
	(R_{FB} – V_{IN}) Voltage	I_{RFB} = 75µA to 125µA		–50		50	mV
	R_{REF} Regulation Voltage		●	0.98	1.00	1.02	V
V_{TC}	TC Pin Voltage				1.00		V
I_{TC}	TC Pin Current	V_{TC} = 1.2V V_{TC} = 0.8V		12	15 –200	18	µA µA
f_{MIN}	Minimum Switching Frequency			11.3	12	12.7	kHz
$t_{ON(MIN)}$	Minimum Switch-On Time				160		ns
$I_{SW(MAX)}$	Maximum Switch Current Limit			3.6	4.5	5.4	A
$I_{SW(MIN)}$	Minimum Switch Current Limit			0.70	0.87	1.04	A
$R_{DS(ON)}$	Switch On-Resistance	I_{SW} = 1.5A			80		mΩ

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

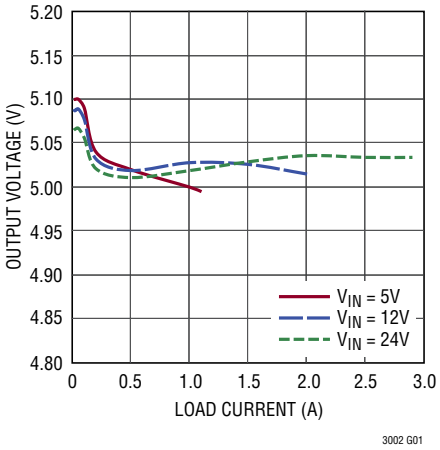
Note 2: The SW pin is rated to 65V for transients. Depending on the leakage inductance voltage spike, operating waveforms of the SW pin should be derated to keep the flyback voltage spike below 65V.

Note 3: The LT3002E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3002I is guaranteed over the full –40°C to 125°C operating junction temperature range.

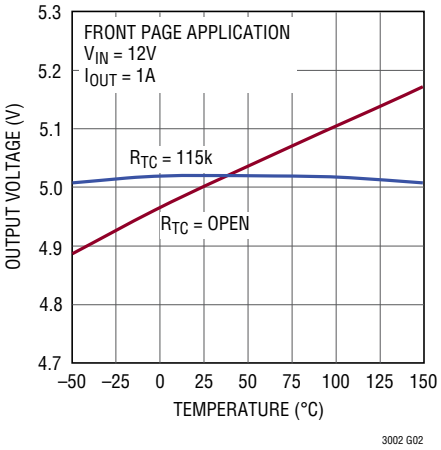
Note 4: The LT3002 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

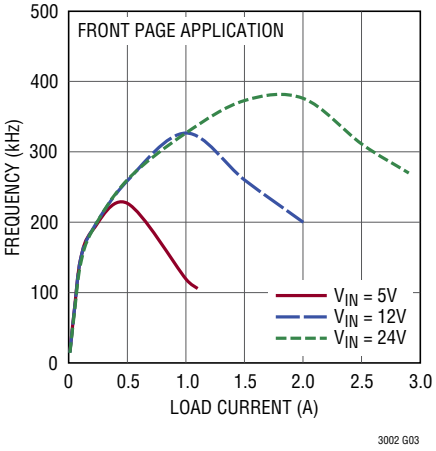
Output Load and Line Regulation



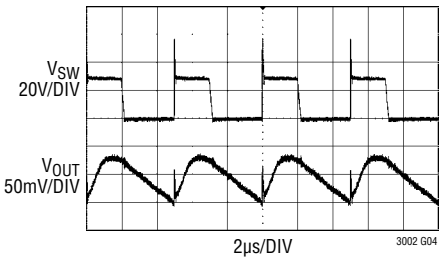
Output Temperature Variation



Switching Frequency vs Load Current

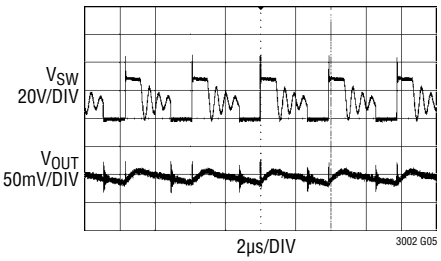


Boundary Mode Waveforms



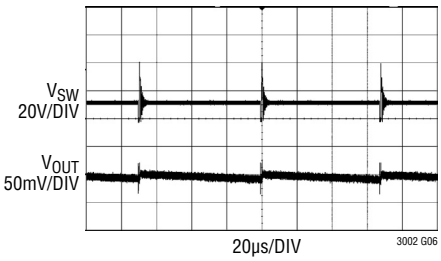
FRONT PAGE APPLICATION
V_{IN} = 12V
I_{OUT} = 2A

Discontinuous Mode Waveforms



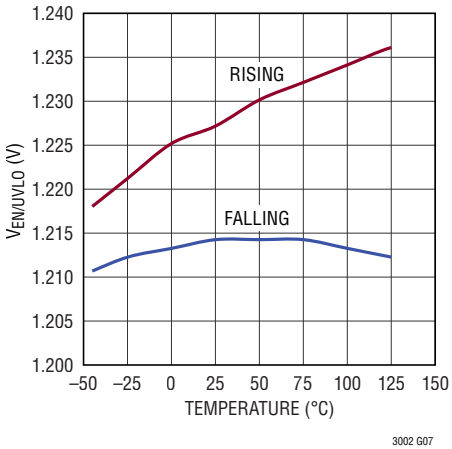
FRONT PAGE APPLICATION
V_{IN} = 12V
I_{OUT} = 0.5A

Burst Mode Waveforms

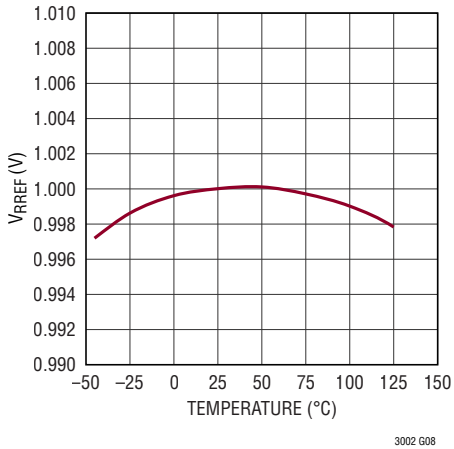


FRONT PAGE APPLICATION
V_{IN} = 12V
I_{OUT} = 10mA

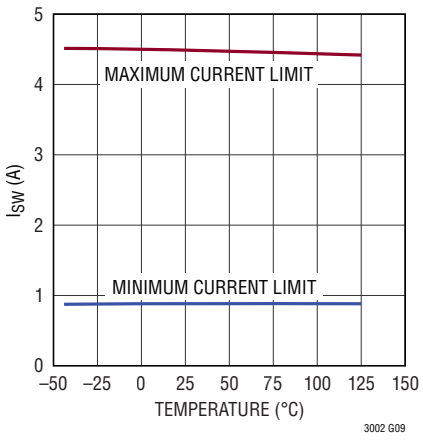
EN/UVLO Enable Threshold



R_{REF} Regulation Voltage



Switch Current Limit



PIN FUNCTIONS

EN/UVLO (Pin 1): Enable/Undervoltage Lockout. The EN/UVLO pin is used to enable the LT3002. Pull the pin below 0.3V to shut down the LT3002. This pin has an accurate 1.214V threshold and can be used to program a V_{IN} undervoltage lockout (UVLO) threshold using a resistor divider from V_{IN} to ground. A 2.5µA current hysteresis allows the programming of V_{IN} UVLO hysteresis. If neither function is used, tie this pin directly to V_{IN}.

$INTV_{CC}$ (Pin 2): Internal 3V Linear Regulator Output. The $INTV_{CC}$ pin is supplied from V_{IN} and powers the internal control circuitry and gate driver. Do not overdrive the $INTV_{CC}$ pin with any external supply, such as a third winding supply. Locally bypass this pin to ground with a minimum 1µF ceramic capacitor.

V_{IN} (Pin 3): Input Supply. The V_{IN} pin supplies current to the internal circuitry and serves as a reference voltage for the feedback circuitry connected to the R_{FB} pin. Locally bypass this pin to ground with a capacitor.

GND (Pin 4, Exposed Pad Pin 9): Ground. The exposed pad provides both electrical contact to ground and good thermal contact to the printed circuit board. Solder the exposed pad directly to the ground plane.

SW (Pin 5): Drain of the Internal DMOS Power Switch. Minimize trace area at this pin to reduce EMI and voltage spikes.

R_{FB} (Pin 6): Input Pin for External Feedback Resistor. Connect a resistor from this pin to the transformer primary SW pin. The ratio of the R_{FB} resistor to the R_{REF} resistor, times the internal voltage reference, determines the output voltage (plus the effect of any non-unity transformer turns ratio). Minimize trace area at this pin.

R_{REF} (Pin 7): Input Pin for External Ground Referred Reference Resistor. The resistor at this pin should be in the range of 10k, but for convenience in selecting a resistor divider ratio, the value may range from 9.09k to 11.0k.

TC (Pin 8): Output Voltage Temperature Compensation. The voltage at this pin is proportional to absolute temperature (PTAT) with temperature coefficient equal to 3.35mV/°K, i.e., equal to 1V at room temperature 25°C. The TC pin voltage can be used to estimate the LT3002 junction temperature. Connect a resistor from this pin to the R_{REF} pin to compensate the output diode temperature coefficient.

OPERATION

The LT3002 is a current mode switching regulator IC designed specially for the isolated flyback topology. The key problem in isolated topologies is how to communicate the output voltage information from the isolated secondary side of the transformer to the primary side for regulation. Historically, opto-isolators or extra transformer windings communicate this information across the isolation boundary. Opto-isolator circuits waste output power, and the extra components increase the cost and physical size of the power supply. Opto-isolators can also cause system issues due to limited dynamic response, nonlinearity, unit-to-unit variation and aging over lifetime. Circuits employing extra transformer windings also exhibit deficiencies, as using an extra winding adds to the transformer's physical size and cost, and dynamic response is often mediocre.

The LT3002 samples the isolated output voltage through the primary-side flyback pulse waveform. In this manner, neither opto-isolator nor extra transformer winding is required for regulation. Since the LT3002 operates in either boundary conduction mode or discontinuous conduction mode, the output voltage is always sampled on the SW pin when the secondary current is zero. This method improves load regulation without the need of external load compensation components.

APPLICATIONS INFORMATION

Output Voltage

The R_{FB} and R_{REF} resistors are external resistors used to program the output voltage.

The output voltage is set by:

$$V_{OUT} = V_{REF} \bullet \left(\frac{R_{FB}}{R_{REF}}\right) \bullet \left(\frac{1}{N_{PS}}\right) - V_F$$

V_F = Output diode forward voltage

N_{PS} = Transformer effective primary-to-secondary turns ratio

V_{REF} = Internal reference voltage 1.00V

Output Temperature Compensation

To cancel the output diode temperature coefficient, the following two equations should be satisfied:

$$V_{OUT} = V_{REF} \bullet \left(\frac{R_{FB}}{R_{REF}}\right) \bullet \left(\frac{1}{N_{PS}}\right) - V_F(T0)$$

$$\left(\delta V_{TC}/\delta T\right) \bullet \left(\frac{R_{FB}}{R_{TC}}\right) \bullet \left(\frac{1}{N_{PS}}\right) = -\left(\delta V_F/\delta T\right)$$

T0 = Room temperature 25°C

$\left(\delta V_F / \delta T\right)$ = Output diode forward voltage temperature coefficient

$\left(\delta V_{TC} / \delta T\right) = 3.35mV/°C$

Primary Inductance Requirement

The LT3002 obtains output voltage information from the reflected output voltage on the SW pin. The conduction of secondary current reflects the output voltage on the primary SW pin. The sample-and-hold error amplifier needs a minimum 350ns to settle and sample the reflected output voltage. In order to ensure proper sampling, the secondary winding needs to conduct current for a minimum of 350ns. The following equation gives the minimum value for primary-side magnetizing inductance:

$$L_{PRI} \geq \frac{t_{OFF(MIN)} \bullet N_{PS} \bullet \left(V_{OUT} + V_F\right)}{I_{SW(MIN)}}$$

$t_{OFF(MIN)}$ = Minimum switch-off time = 350ns (TYP)

$I_{SW(MIN)}$ = Minimum switch current limit = 0.87A (TYP)

In addition to the primary inductance requirement for the minimum switch-off time, the LT3002 has minimum switch-on time that prevents the chip from turning on the power switch shorter than approximately 160ns. This minimum switch-on time is mainly for leading-edge blanking the initial switch turn-on current spike. If the inductor current exceeds the desired current limit during that time, oscillation may occur at the output as the current control loop will lose its ability to regulate. Therefore, the following equation relating to maximum input voltage must also be followed in selecting primary-side magnetizing inductance:

$$L_{PRI} \geq \frac{t_{ON(MIN)} \bullet V_{IN(MAX)}}{I_{SW(MIN)}}$$

$t_{ON(MIN)}$ = Minimum switch-on time = 160ns (TYP)

In general, choose a transformer with its primary magnetizing inductance about 40% to 60% larger than the minimum values calculated above. A transformer with much larger inductance will have a bigger physical size and may cause instability at light load.

Undervoltage Lockout (UVLO)

A resistive divider from V_{IN} to the EN/UVLO pin implements undervoltage lockout (UVLO). The EN/UVLO enable falling threshold is set at 1.214V with 14mV hysteresis. In addition, the EN/UVLO pin sinks 2.5µA when the voltage on the pin is below 1.214V. This current provides user programmable hysteresis based on the value of R1. The programmable UVLO thresholds are:

$$V_{IN(UVLO^+)} = \frac{1.228V \bullet (R1+R2)}{R2} + 2.5\mu A \bullet R1$$

$$V_{IN(UVLO^-)} = \frac{1.214V \bullet (R1+R2)}{R2}$$

Figure 1 shows the implementation of external shutdown control while still using the UVLO function. The NMOS grounds the EN/UVLO pin when turned on, and puts the LT3002 in shutdown with quiescent current less than 2µA.

APPLICATIONS INFORMATION

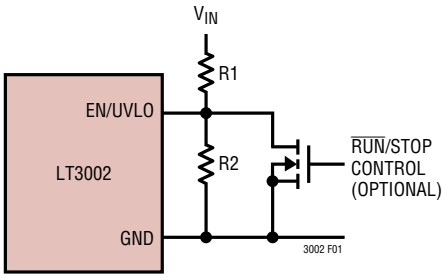


Figure 1. Undervoltage Lockout (UVLO)

Minimum Load Requirement

The LT3002 samples the isolated output voltage from the primary-side flyback pulse waveform. The flyback pulse occurs once the primary switch turns off and the secondary winding conducts current. In order to sample the output voltage, the LT3002 has to turn on and off for a minimum amount of time and with a minimum frequency. The LT3002 delivers a minimum amount of energy even during light load conditions to ensure accurate output voltage information. The minimum energy delivery creates a minimum load requirement, which can be approximately estimated as:

$$I_{LOAD(MIN)} = \frac{L_{PRI} \bullet I_{SW(MIN)}^2 \bullet f_{MIN}}{2 \bullet V_{OUT}}$$

L_{PRI} = Transformer primary inductance

$I_{SW(MIN)}$ = Minimum switch current limit = 1.04A (MAX)

f_{MIN} = Minimum switching frequency = 12.7kHz (MAX)

The LT3002 typically needs less than 0.5% of its full output power as minimum load. Alternatively, a Zener diode with its breakdown of 10% higher than the output voltage can serve as a minimum load if pre-loading is not acceptable. For a 5V output, use a 5.6V Zener with cathode connected to the output.

Design Example

Use the following design example as a guide to designing applications for the LT3002. The design example involves designing a 5V output with a 1.5A load current and an input range from 8V to 32V.

$V_{IN(MIN)}$ = 8V, $V_{IN(NOM)}$ = 12V, $V_{IN(MAX)}$ = 32V, V_{OUT} = 5V, I_{OUT} = 1.5A

Step 1: Select the transformer turns ratio.

$$N_{PS} < \frac{65V - V_{IN(MAX)} - V_{LEAKAGE}}{V_{OUT} + V_F}$$

$V_{LEAKAGE}$ = Margin for transformer leakage spike = 15V

V_F = Output diode forward voltage = ~0.3V

Example:

$$N_{PS} < \frac{65V - 32V - 15V}{5V + 0.3V} = 3.4$$

The choice of transformer turns ratio is critical in determining output current capability of the converter. Table 1 shows the switch voltage stress and output current capability at different transformer turns ratio.

Table 1. Switch Voltage Stress and Output Current Capability vs Turns Ratio

NPS	$V_{SW(MAX)}$ at $V_{IN(MAX)}$ (V)	$I_{OUT(MAX)}$ at $V_{IN(MIN)}$ (A)	DUTY CYCLE (%)
1:1	37.3	0.92	14-40
2:1	42.6	1.31	25-57
3:1	47.9	1.53	33-67

Clearly, only N_{PS} = 3 can meet the 1.5A output current requirement, so N_{PS} = 3 is chosen as the turns ratio in this example.

Step 2: Determine the primary inductance.

Primary inductance for the transformer must be set above a minimum value to satisfy the minimum switch-off and switch-on time requirements:

$$L_{PRI} \geq \frac{t_{OFF(MIN)} \bullet N_{PS} \bullet (V_{OUT} + V_F)}{I_{SW(MIN)}}$$

$$L_{PRI} \geq \frac{t_{ON(MIN)} \bullet V_{IN(MAX)}}{I_{SW(MIN)}}$$

$t_{OFF(MIN)}$ = 350ns

$t_{ON(MIN)}$ = 160ns

$I_{SW(MIN)}$ = 0.87A

APPLICATIONS INFORMATION

Example:

$$L_{PRI} \geq \frac{350ns \bullet 3 \bullet (5V + 0.3V)}{0.87A} = 6.4\mu H$$

$$L_{PRI} \geq \frac{160ns \bullet 32V}{0.87A} = 5.9\mu H$$

Most transformers specify primary inductance with a tolerance of ±20%. With other component tolerance considered, choose a transformer with its primary inductance 40% to 60% larger than the minimum values calculated above. L_{PRI} = 9µH is then chosen in this example.

Once the primary inductance has been determined, the maximum load switching frequency can be calculated as:

$$f_{SW} = \frac{1}{t_{ON} + t_{OFF}} = \frac{1}{\frac{L_{PRI} \bullet I_{SW}}{V_{IN}} + \frac{L_{PRI} \bullet I_{SW}}{N_{PS} \bullet (V_{OUT} + V_F)}}$$

$$I_{SW} = \frac{V_{OUT} \bullet I_{OUT} \bullet 2}{\eta \bullet V_{IN} \bullet D}$$

Example:

$$D = \frac{(5V + 0.3V) \bullet 3}{(5V + 0.3V) \bullet 3 + 12V} = 0.57$$

$$I_{SW} = \frac{5V \bullet 1.5A \bullet 2}{0.8 \bullet 12V \bullet 0.57}$$

$$f_{SW} = 277kHz$$

The transformer also needs to be rated for the correct saturation current level across line and load conditions. A saturation current rating larger than 7A is necessary to work with the LT3002.

Step 3: Choose the output diode.

Two main criteria for choosing the output diode include forward current rating and reverse-voltage rating. The maximum load requirement is a good first-order guess at the average current requirement for the output diode. Under output short-circuit condition, the output diode needs to conduct much higher current. Therefore, a conservative metric is 60% of the maximum switch current limit multiplied by the turns ratio:

$$I_{DIODE(MAX)} = 0.6 \bullet I_{SW(MAX)} \bullet N_{PS}$$

Example:

$$I_{DIODE(MAX)} = 8.1A$$

Next calculate reverse voltage requirement using maximum V_{IN}:

$$V_{REVERSE} = V_{OUT} + \frac{V_{IN(MAX)}}{N_{PS}}$$

Example:

$$V_{REVERSE} = 5V + \frac{32V}{3} = 15.7V$$

The PDS835L (8A, 35V diode) from Diodes Inc. is chosen.

Step 4: Choose the output capacitor.

The output capacitor should be chosen to minimize the output voltage ripple while considering the increase in size and cost of a larger capacitor. Use the following equation to calculate the output capacitance:

$$C_{OUT} = \frac{L_{PRI} \bullet I_{SW}^2}{2 \bullet V_{OUT} \bullet \Delta V_{OUT}}$$

Example:

Design for output voltage ripple less than ±1% of V_{OUT}, i.e., 100mV.

$$C_{OUT} = \frac{9\mu H \bullet (4.5A)^2}{2 \bullet 5V \bullet 0.1V} = 182\mu F$$

Remember ceramic capacitors lose capacitance with applied voltage. The capacitance can drop to 40% of quoted capacitance at the maximum voltage rating. So a 220µF, 6.3V rating X5R or X7R ceramic capacitor is chosen.

APPLICATIONS INFORMATION

Step 5: Design snubber circuit.

The snubber circuit protects the power switch from leakage inductance voltage spike. A (RC + DZ) snubber is recommended for this application. A 470pF capacitor in series with a 39Ω resistor is chosen as the RC snubber.

The maximum Zener breakdown voltage is set according to the maximum V_{IN}:

$V_{ZENNER(MAX)} \leq 60V - V_{IN(MAX)}$

Example:

$V_{ZENNER(MAX)} \leq 60V - 32V = 28V$

A 24V Zener with a maximum of 26V will provide optimal protection and minimize power loss. So a 24V, 1.5W Zener from Central Semiconductor (CMZ5934B) is chosen.

Choose a diode that is fast and has sufficient reverse voltage breakdown:

$V_{REVERSE} > V_{SW(MAX)}$

$V_{SW(MAX)} = V_{IN(MAX)} + V_{ZENNER(MAX)}$

Example:

$V_{REVERSE} > 60V$

A 100V, 1A diode from Diodes Inc. (DFLS1100) is chosen.

Step 6: Select the R_{REF} and R_{FB} resistors.

Use the following equation to calculate the starting values for R_{REF} and R_{FB}:

$$R_{FB} = \frac{R_{REF} \bullet N_{PS} \bullet \left(V_{OUT} + V_F(T0)\right)}{V_{REF}}$$

R_{REF} = 10k

Example:

$$R_{FB} = \frac{10k \bullet 3 \bullet (5V + 0.3V)}{1.00V} = 159k$$

For 1% standard values, a 158k resistor is chosen.

Step 7: Adjust R_{FB} resistor based on output voltage.

Build and power up the application with application components and measure the regulated output voltage. Adjust R_{FB} resistor based on the measured output voltage:

$$R_{FB(NEW)} = \frac{V_{OUT}}{V_{OUT(MEASURED)}} \bullet R_{FB}$$

Example:

$$R_{FB} = \frac{5V}{5.14V} \bullet 158k = 154k$$

Step 8: Select R_{TC} resistor based on output voltage temperature variation.

Measure output voltage in a controlled temperature environment like an oven to determine the output temperature coefficient. Measure output voltage at a consistent load current and input voltage, across the operating temperature range.

Calculate the temperature coefficient of V_F:

$$-(\delta V_F/\delta T) = \frac{V_{OUT}(T1) - V_{OUT}(T2)}{T1 - T2}$$

$$R_{TC} = \frac{3.35mV/°C}{-(\delta V_F/\delta T)} \bullet \left(\frac{R_{FB}}{N_{PS}}\right)$$

Example:

$$-(\delta V_F/\delta T) = \frac{5.189V - 5.041V}{100°C - (0°C)} = 1.48mV/°C$$

$$R_{TC} = \frac{3.35mV/°C}{1.48mV/°C} \bullet \left(\frac{154}{3}\right) = 115k$$

Step 9: Select the EN/UVLO resistors.

Determine the amount of hysteresis required and calculate R1 resistor value:

$V_{IN(HYS)} = 2.5\mu A \bullet R1$

Example:

Choose 2V of hysteresis, R1 = 806k

APPLICATIONS INFORMATION

Determine the UVLO thresholds and calculate R2 resistor value:

$$V_{IN(UVLO+)} = \frac{1.228V \bullet (R1 + R2)}{R2} + 2.5\mu A \bullet R1$$

Example:

Set V_{IN} UVLO rising threshold to 7.5V:

R2 = 232k

$V_{IN(UVLO+)}$ = 7.5V

$V_{IN(UNLO-)}$ = 5.5V

Step 10: Ensure minimum load.

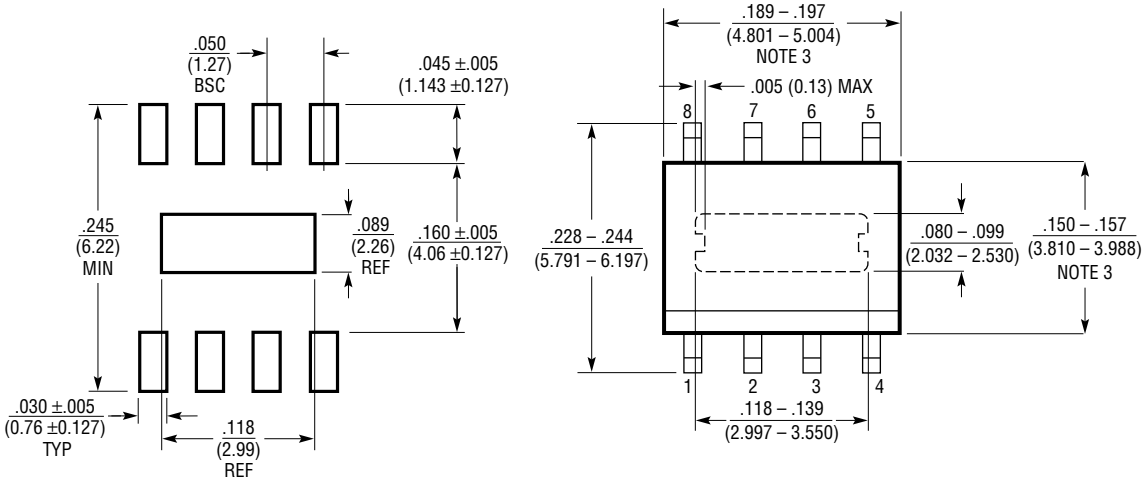
The theoretical minimum load can be approximately estimated as:

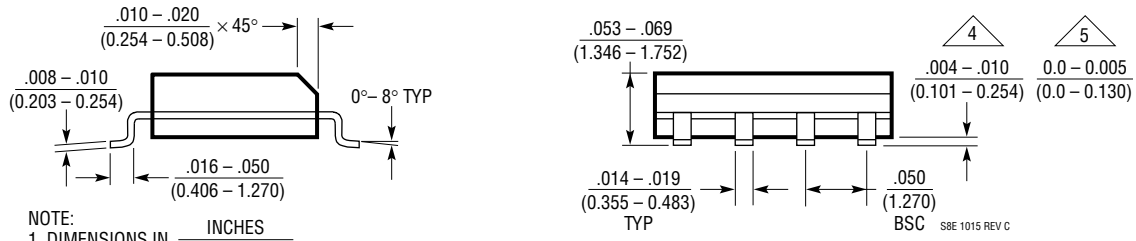
$$I_{LOAD(MIN)} = \frac{9\mu H \bullet (1.04A)^2 \bullet 12.7kHz}{2 \bullet 5V} = 12.4mA$$

Remember to check the minimum load requirement in real application. The minimum load occurs at the point where the output voltage begins to climb up as the converter delivers more energy than what is consumed at the output. The real minimum load for this application is about 10mA. In this example, a 500Ω resistor is selected as the minimum load.

PACKAGE DESCRIPTION

S8E Package
8-Lead Plastic SOIC (Narrow .150 Inch) Exposed Pad
(Reference LTC DWG # 05-08-1857 Rev C)





NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010" (0.254mm)
4. STANDARD LEAD STANDOFF IS 4mils TO 10mils (DATE CODE BEFORE 542)
5. LOWER LEAD STANDOFF IS 0mils TO 5mils (DATE CODE AFTER 542)