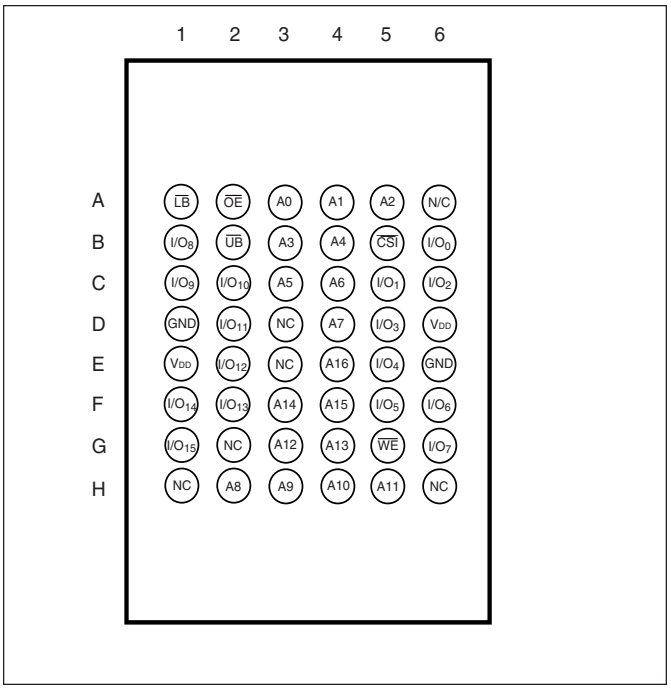
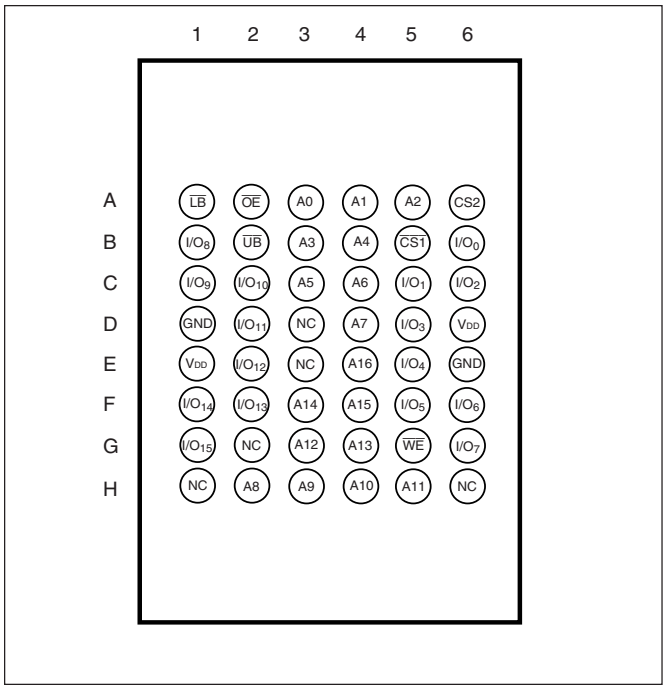
PIN CONFIGURATIONS

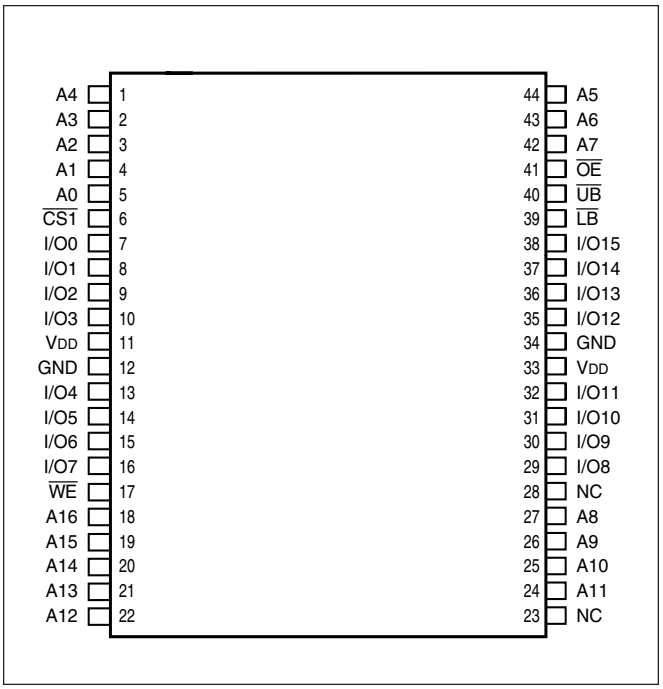
48-Pin mini BGA (6mm x 8mm) (Package Code B)



48-Pin mini BGA (6mm x 8mm) 2 CS Option (Package Code B2)



44-Pin mini TSOP (Type II) (Package Code T)



PIN DESCRIPTIONS

A0-A16	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
CS1, CS2	Chip Enable Input
OE	Output Enable Input
WE	Write Enable Input
LB	Lower-byte Control (I/O0-I/O7)
UB	Upper-byte Control (I/O8-I/O15)
NC	No Connection
VDD	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O PIN I/O0-I/O7	I/O PIN I/O8-I/O15	Vdd Current
Not Selected	X	H	X	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
	X	X	L	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
	X	X	X	X	H	H	High-Z	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	H	L	X	High-Z	High-Z	I_{CC}
	H	L	H	H	X	L	High-Z	High-Z	I_{CC}
Read	H	L	H	L	L	H	D_{OUT}	High-Z	I_{CC}
	H	L	H	L	H	L	High-Z	D_{OUT}	
	H	L	H	L	L	L	D_{OUT}	D_{OUT}	
Write	L	L	H	X	L	H	D_{IN}	High-Z	I_{CC}
	L	L	H	X	H	L	High-Z	D_{IN}	
	L	L	H	X	L	L	D_{IN}	D_{IN}	

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.2 to V_{DD}+0.3	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE (V_{DD})

Option	Ambient Temperature	IS65WV12816ALL	IS65WV12816BLL
A	0°C to +70°C	1.65V - 2.2V	2.5V - 3.6V
A1	–40°C to +85°C	1.65V - 2.2V	2.5V - 3.6V
A2	–40°C to +105°C	1.65V - 2.2V	2.5V - 3.6V
A3	–40°C to +125°C	1.65V - 2.2V	2.5V - 3.6V

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Vdd	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA	1.65-2.2V	1.4	—	V
		I_{OH} = -1 mA	2.5-3.6V	2.2	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	1.65-2.2V	—	0.2	V
		I_{OL} = 2.1 mA	2.5-3.6V	—	0.4	V
V_{IH}	Input HIGH Voltage		1.65-2.2V	1.4	V_{DD} + 0.2	V
			2.5-3.6V	2.2	V_{DD} + 0.3	V
V_{IL}(1)	Input LOW Voltage		1.65-2.2V	–0.2	0.4	V
			2.5-3.6V	–0.2	0.6	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}		–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled		–1	1	µA

Notes:
1. V_{IL} (min.) = –1.0V for pulse width less than 10 ns.

CAPACITANCE(1)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	10	pF

Note:
1. Tested initially and after any design or process changes that may affect these parameters.

IS65WV12816ALL, POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions	Options	Max. -70 ns	Unit
I_{CC}	Vdd Dynamic Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX}	A, A1 A2, A3	15 20	mA
I_{CC1}	Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = 0	A, A1 A2, A3	7 7	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CS1}$ = V_{IH}, CS2 = V_{IL}, f = 1 MHz **OR**	A, A1 A2, A3	0.6 0.6	mA
	ULB Control	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CS1}$ = V_{IL}, f = 0, $\overline{UB}$ = V_{IH}, $\overline{LB}$ = V_{IH}			
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., $\overline{CS1} \geq V_{DD} - 0.2V$, CS2 $\leq$ 0.2V, $V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq 0.2V$, f = 0 **OR**	A, A1 A2 A3	15 20 50	µA
	ULB Control	V_{DD} = Max., $\overline{CS1}$ = V_{IL}, CS2 = V_{IH} $V_{IN} \leq 0.2V$, f = 0; $\overline{UB}$/$\overline{LB}$ = $V_{DD} - 0.2V$			

IS65WV12816BLL, POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions	Options	Max. -55 ns	Max. -70 ns	Unit
I_{CC}	Vdd Dynamic Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX}	A, A1 A2, A3	25 30	20 25	mA
I_{CC1}	Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = 0	A, A1 A2, A3	7 7	7 7	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CS1}$ = V_{IH}, CS2 = V_{IL}, f = 1 MHz **OR**	A, A1 A2, A3	0.6 0.6	0.6 0.6	mA
	ULB Control	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CS1}$ = V_{IL}, f = 0, $\overline{UB}$ = V_{IH}, $\overline{LB}$ = V_{IH}				
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., $\overline{CS1} \geq V_{DD} - 0.2V$, CS2 $\leq$ 0.2V, $V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq 0.2V$, f = 0 **OR**	A, A1 A2 A3	15 25 65	15 25 65	µA
	ULB Control	V_{DD} = Max., $\overline{CS1}$ = V_{IL}, CS2 = V_{IH} $V_{IN} \leq 0.2V$, f = 0; $\overline{UB}$/$\overline{LB}$ = $V_{DD} - 0.2V$				

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

AC TEST CONDITIONS

Parameter	65WV12816ALL (Unit)	65WV12816BLL (Unit)
Input Pulse Level	0.4V to V_{DD}-0.2V	0.4V to V_{DD}-0.3V
Input Rise and Fall Times	5 ns	5ns
Input and Output Timing and Reference Level	V_{REF}	V_{REF}
Output Load	See Figures 1 and 2	See Figures 1 and 2

	65WV12816ALL (1.65V-2.2V)	65WV12816BLL (2.5V - 3.6V)
R1(Ω)	3070	3070
R2(Ω)	3150	3150
V_{REF}	0.9V	1.5V
V_{TM}	1.8V	2.8V

AC TEST LOADS

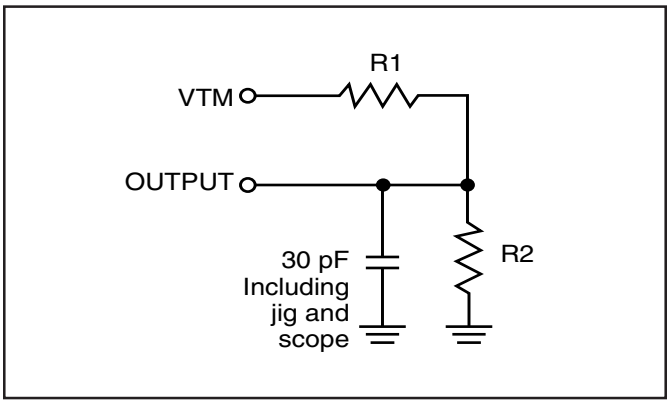


Figure 1

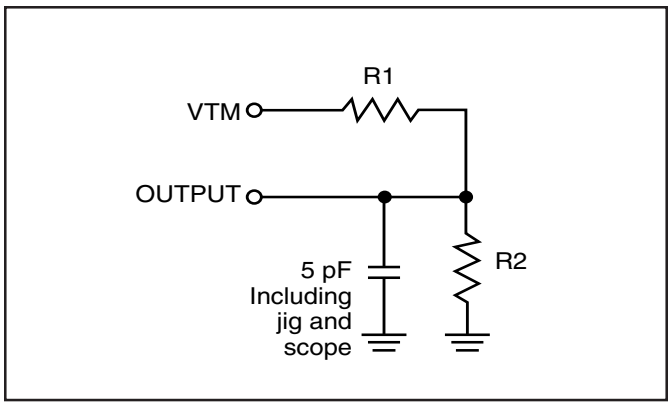


Figure 2

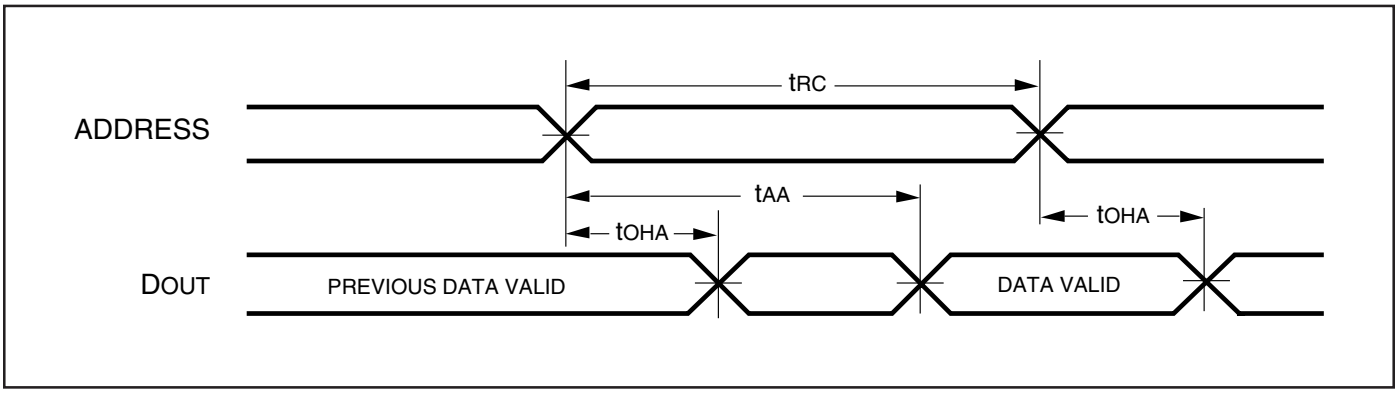
READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-55 ns Min.	-55 ns Max.	-70 ns Min.	-70 ns Max.	Unit
t_{RC}	Read Cycle Time	55	—	70	—	ns
t_{AA}	Address Access Time	—	55	—	70	ns
t_{OHA}	Output Hold Time	10	—	10	—	ns
t_{ACS1}/t_{ACS2}	$\overline{CS1}$/CS2 Access Time	—	55	—	70	ns
t_{DOE}	$\overline{OE}$ Access Time	—	25	—	35	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	20	—	25	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	5	—	5	—	ns
t_{HZCS1}/t_{HZCS2}[2]	$\overline{CS1}$/CS2 to High-Z Output	0	20	0	25	ns
t_{LZCS1}/t_{LZCS2}[2]	$\overline{CS1}$/CS2 to Low-Z Output	10	—	10	—	ns
t_{BA}	$\overline{LB}$, $\overline{UB}$ Access Time	—	55	—	70	ns
t_{HZB}	$\overline{LB}$, $\overline{UB}$ to High-Z Output	0	20	0	25	ns
t_{LZB}	$\overline{LB}$, $\overline{UB}$ to Low-Z Output	0	—	0	—	ns

Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V, input pulse levels of 0.4 to 1.4V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

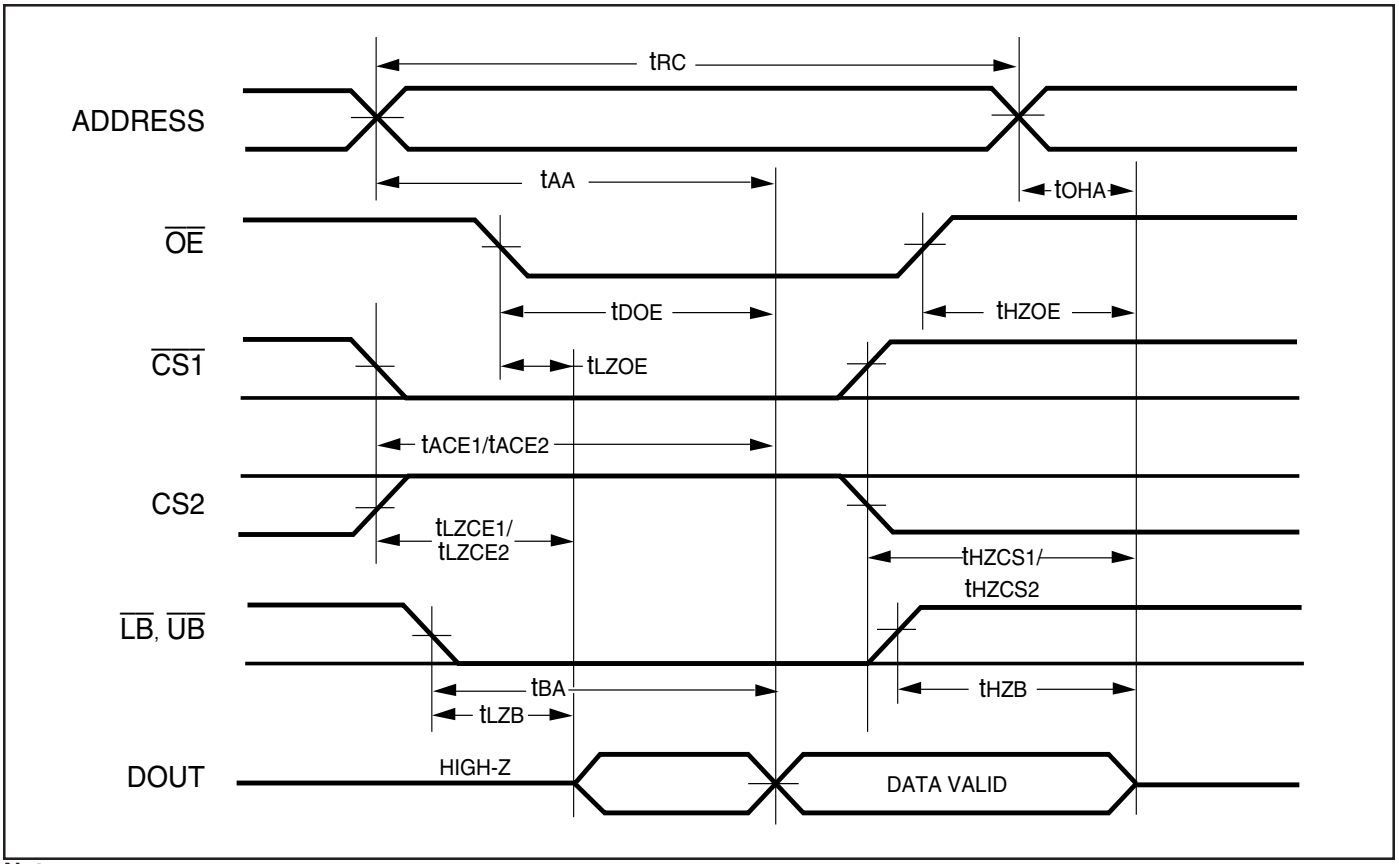
AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CS1}$ = $\overline{OE}$ = VIL, $\overline{CS2}$ = $\overline{WE}$ = VIH, $\overline{UB}$ or $\overline{LB}$ = VIL)



AC WAVEFORMS

READ CYCLE NO. 2[1,3] ($\overline{CS1}$, $\overline{CS2}$, $\overline{OE}$, AND $\overline{UB}$/$\overline{LB}$ Controlled)



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CS1}$, $\overline{UB}$, or $\overline{LB}$ = VIL. CS2=$\overline{WE}$=VIH.
3. Address is valid prior to or coincident with $\overline{CS1}$ LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range)

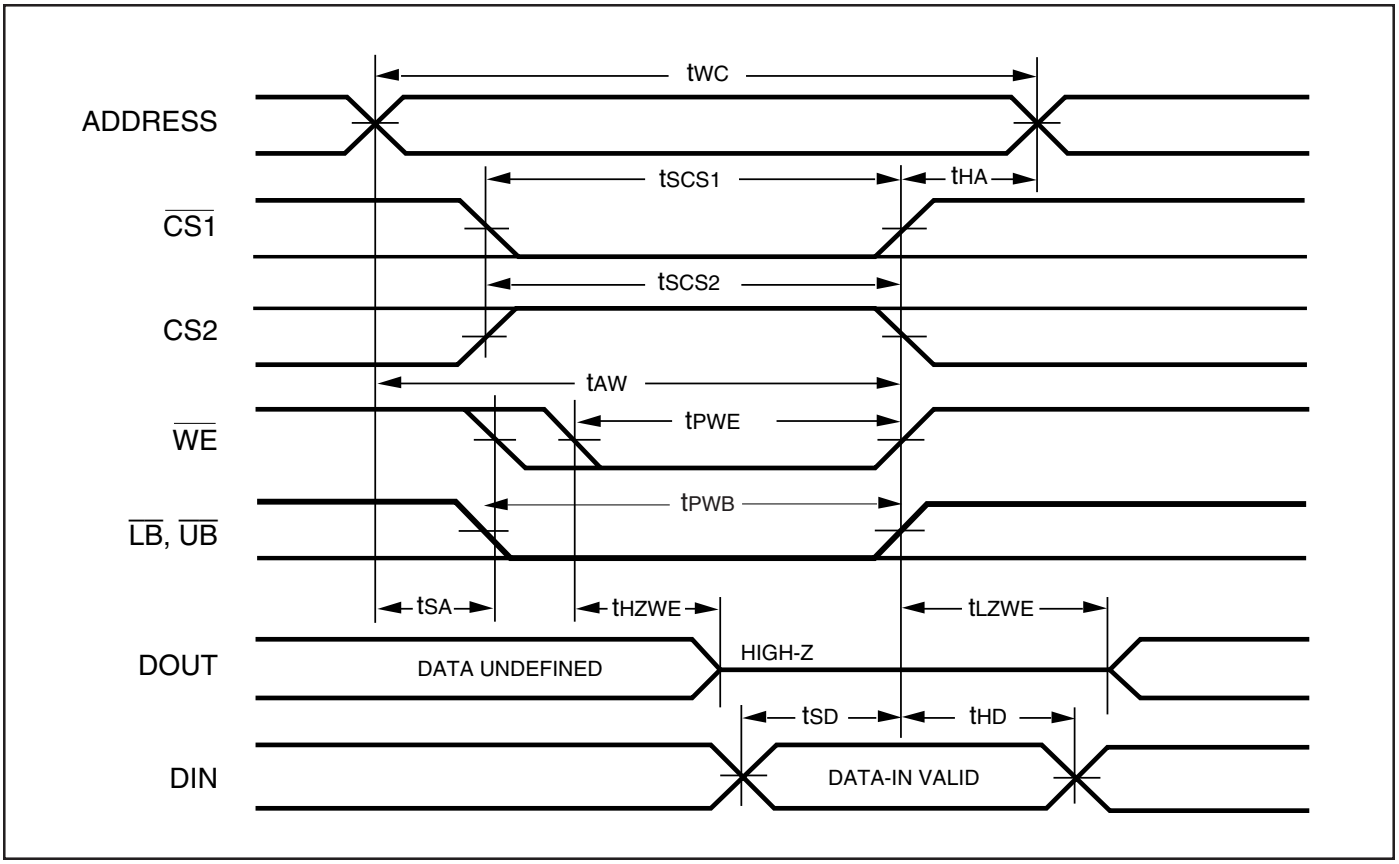
Symbol	Parameter	-55 ns Min.	-55 ns Max.	-70 ns Min.	-70 ns Max.	Unit
t_{WC}	Write Cycle Time	55	—	70	—	ns
t_{SCS1}/t_{SCS2}	$\overline{CS1}$/CS2 to Write End	45	—	60	—	ns
t_{AW}	Address Setup Time to Write End	45	—	60	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PWB}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	45	—	60	—	ns
t_{PWE}	$\overline{WE}$ Pulse Width	40	—	50	—	ns
t_{SD}	Data Setup to Write End	25	—	30	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns
t_{HZWE}[3]	$\overline{WE}$ LOW to High-Z Output	—	20	—	20	ns
t_{LZWE}[3]	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	ns

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V, input pulse levels of 0.4V to 1.4V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{CS1}$ LOW, CS2 HIGH and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

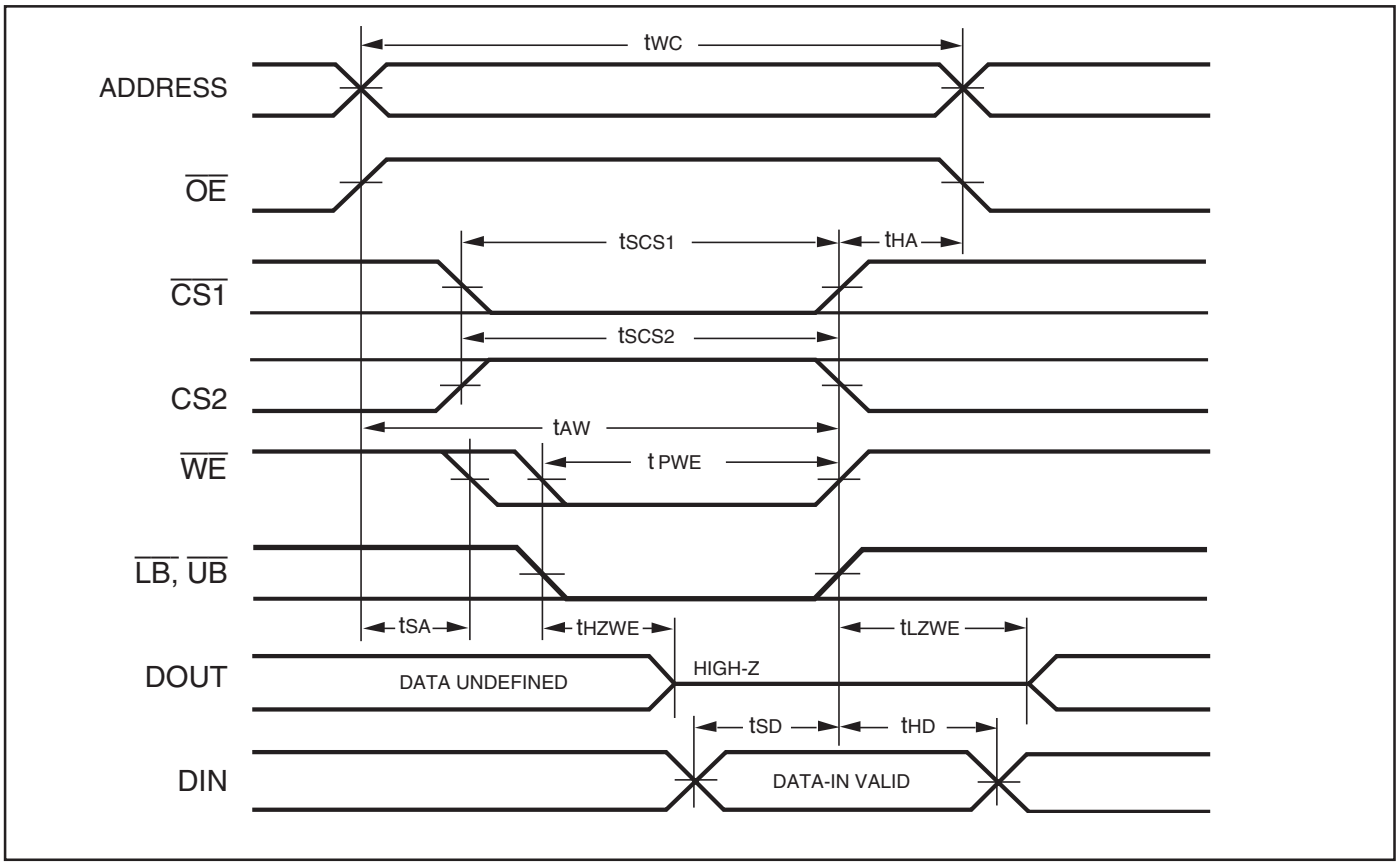
WRITE CYCLE NO. 1[1,2] ($\overline{CS1}$ Controlled, $\overline{OE}$ = HIGH or LOW)



Notes:
1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{CS1}$, CS2 and $\overline{WE}$ inputs and at least one of the $\overline{LB}$ and $\overline{UB}$ inputs being in the LOW state.
2. WRITE = ($\overline{CS1}$) [($\overline{LB}$) = ($\overline{UB}$)] ($\overline{WE}$).

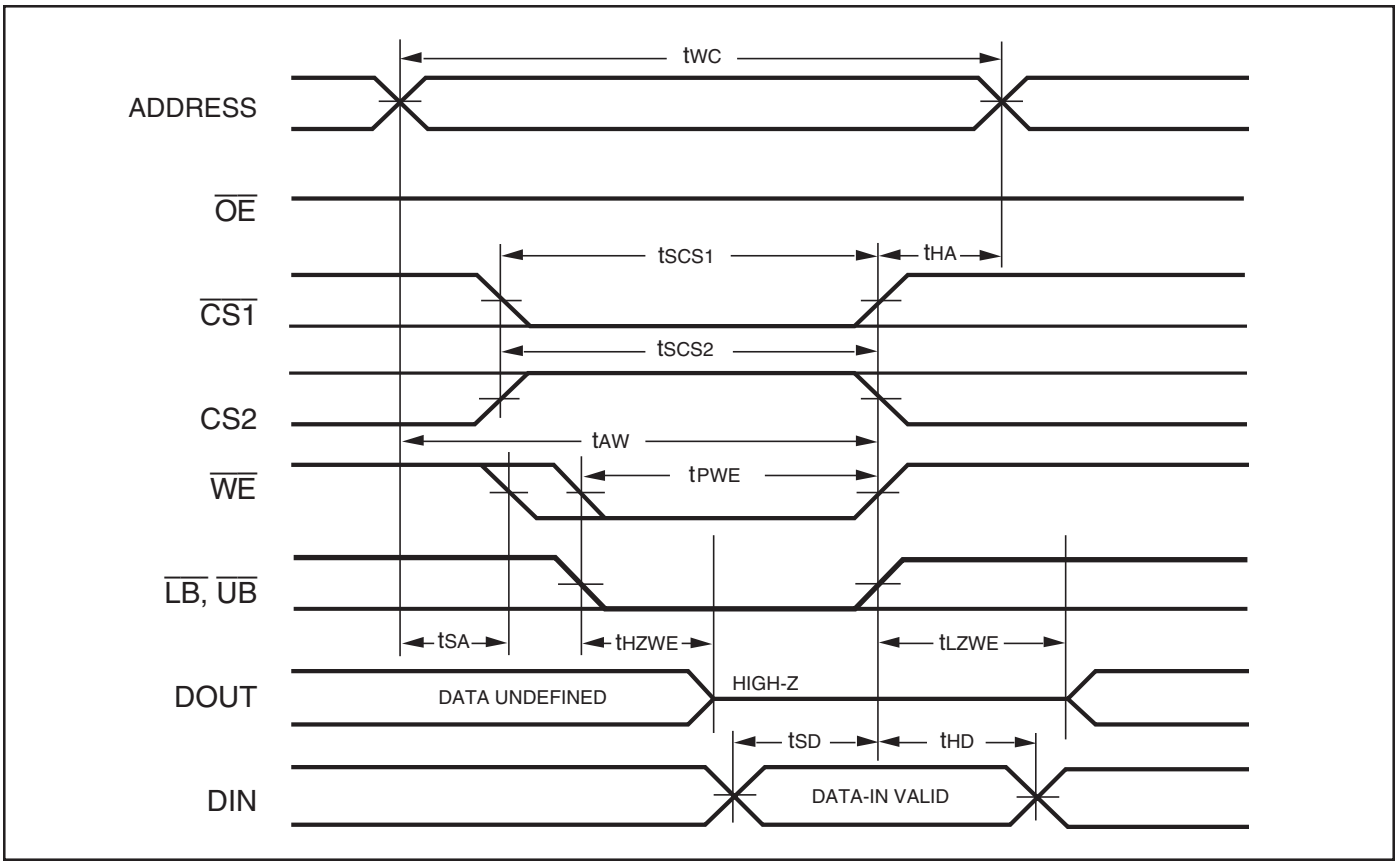
AC WAVEFORMS

WRITE CYCLE NO. 2 ($\overline{WE}$ Controlled: $\overline{OE}$ is HIGH During Write Cycle)



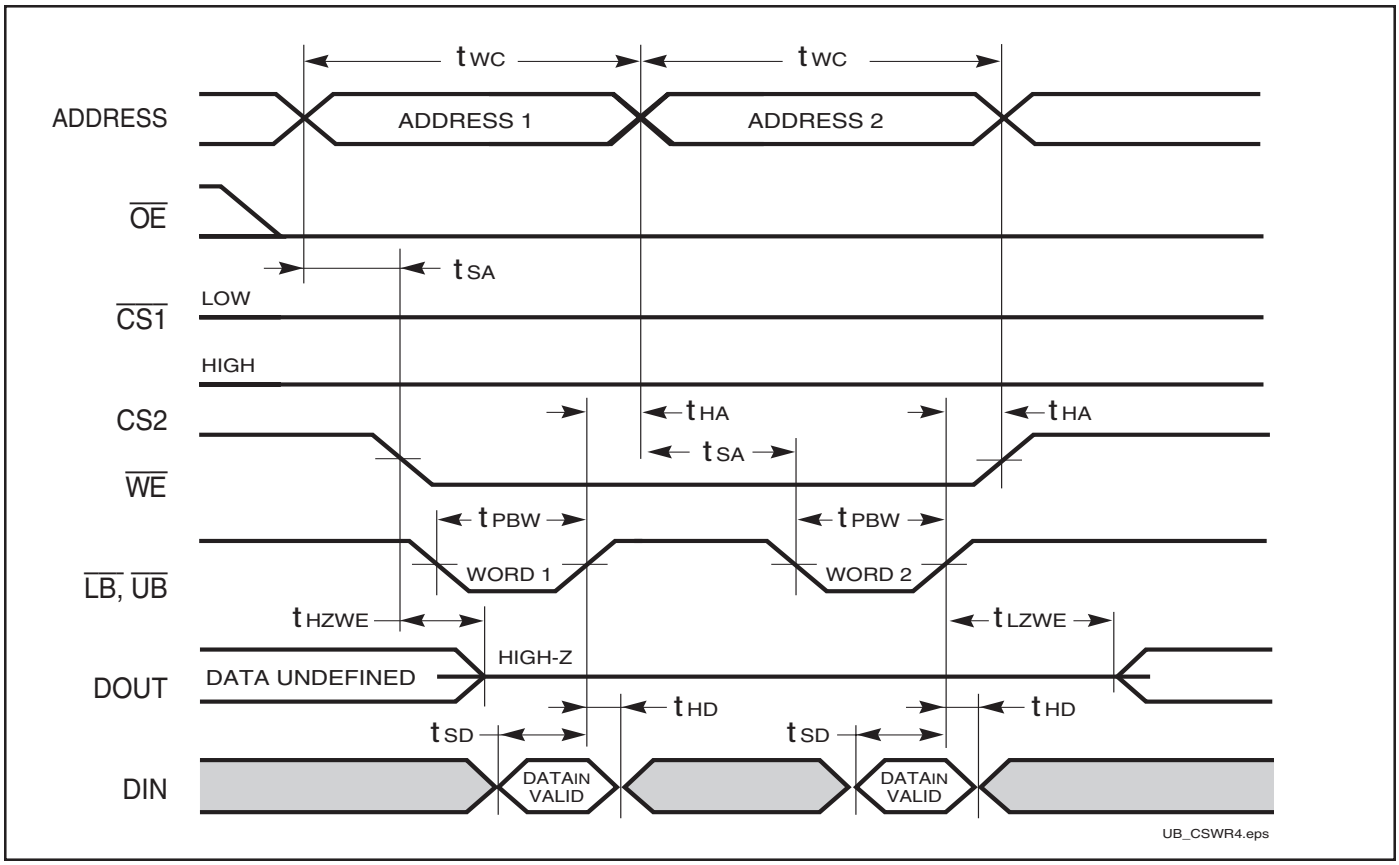
AC WAVEFORMS

WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)



AC WAVEFORMS

WRITE CYCLE NO. 4 ($\overline{UB}$/$\overline{LB}$ Controlled)

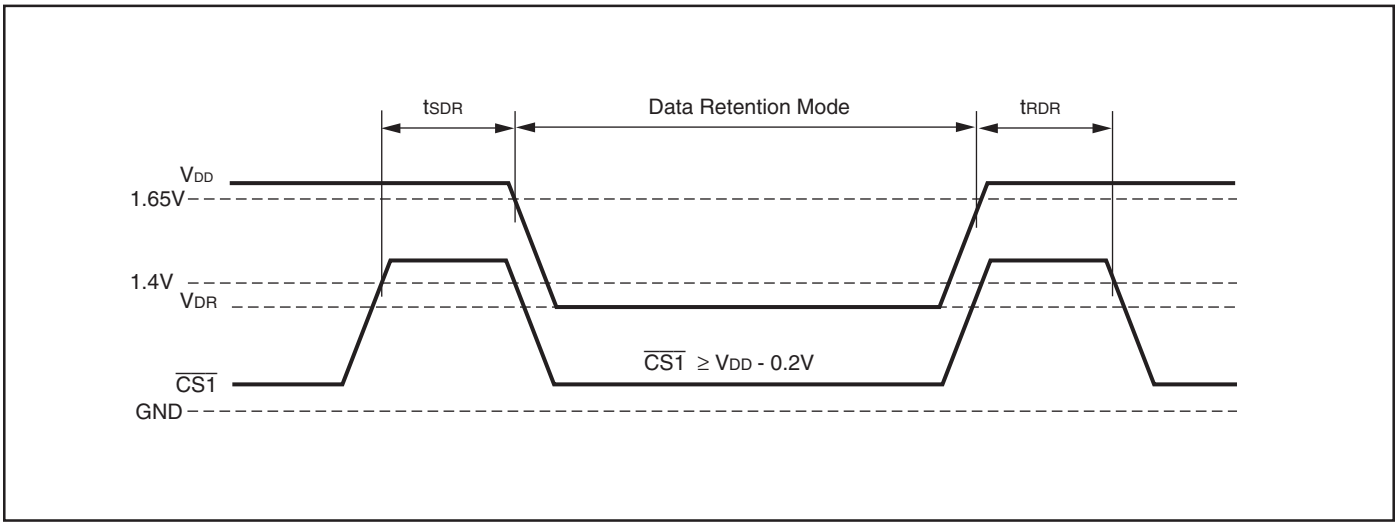


DATA RETENTION SWITCHING CHARACTERISTICS (LL)

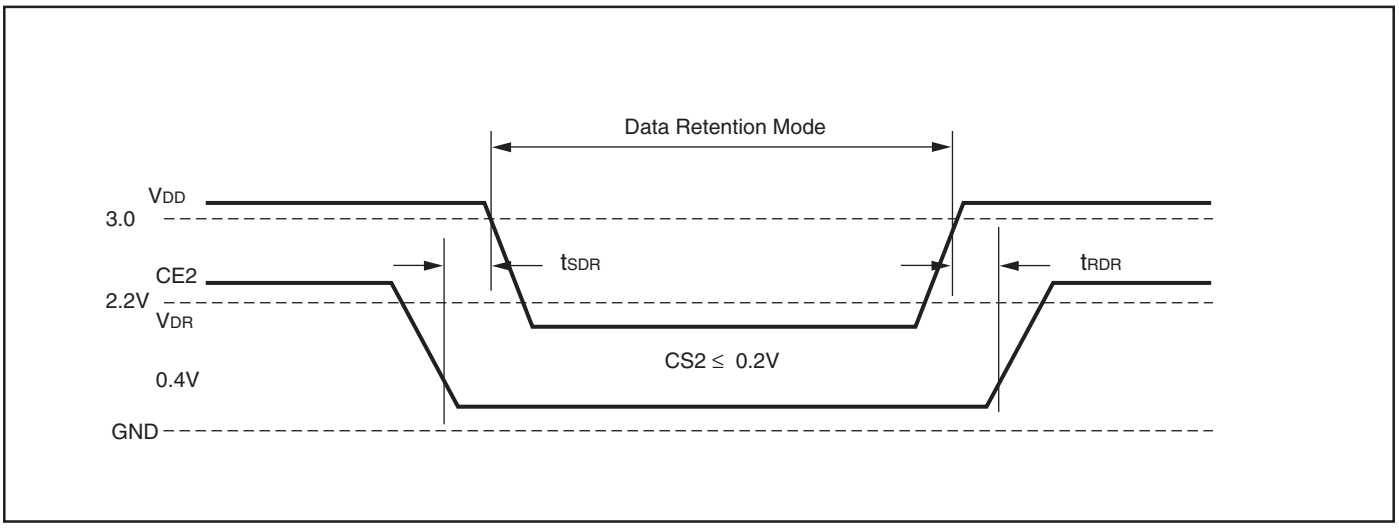
Symbol	Parameter	Test Condition	Options	Min.	Typ.(1)	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		1.2	—	3.6	V
I_{DR}	Data Retention Current	Vdd = 1.2V, $\overline{CS1} \geq V_{DD} - 0.2V$	A, A1	—	5	15	µA
			A2	—	—	25	
			A3	—	—	65	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}	—	—	ns

Note 1: Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CS1}$ Controlled)



DATA RETENTION WAVEFORM (CS2 Controlled)



ORDERING INFORMATION

IS65WV12816ALL (1.65V - 2.2V)

Temperature Range (A): 0°C to +70°C

Speed (ns)	Order Part No.	Package
70	IS65WV12816ALL-70TA	TSOP
	IS65WV12816ALL-70BA	mini BGA (6mm x 8mm)
	IS65WV12816ALL-70B2A	mini BGA (6mm x 8mm), 2 CS Option

Temperature Range (A1): –40°C to +85°C

Speed (ns)	Order Part No.	Package
70	IS65WV12816ALL-70TA1	TSOP
	IS65WV12816ALL-70BA1	mini BGA (6mm x 8mm)
	IS65WV12816ALL-70B2A1	mini BGA (6mm x 8mm), 2 CS Option

Temperature Range (A2): –40°C to +105°C

Speed (ns)	Order Part No.	Package
70	IS65WV12816ALL-70TA2	TSOP
	IS65WV12816ALL-70BA2	mini BGA (6mm x 8mm)
	IS65WV12816ALL-70B2A2	mini BGA (6mm x 8mm), 2 CS Option

Temperature Range (A3): –40°C to +125°C

Speed (ns)	Order Part No.	Package
70	IS65WV12816ALL-70TA3	TSOP
	IS65WV12816ALL-70BA3	mini BGA (6mm x 8mm)
	IS65WV12816ALL-70B2A3	mini BGA (6mm x 8mm), 2 CS Option

ORDERING INFORMATION

IS65WV12816BLL (2.5V - 3.6V)

Temperature Range (A): 0°C to +70°C

Speed (ns)	Order Part No.	Package
55	IS65WV12816BLL-55TA	TSOP
	IS65WV12816BLL-55BA	mini BGA (6mm x 8mm)
	IS65WV12816BLL-55B2A	mini BGA (6mm x 8mm), 2 CS Option
70	IS65WV12816BLL-70TA	TSOP
	IS65WV12816BLL-70BA	mini BGA (6mm x 8mm)
	IS65WV12816BLL-70B2A	mini BGA (6mm x 8mm), 2 CS Option

Temperature Range (A1): –40°C to +85°C

Speed (ns)	Order Part No.	Package
55	IS65WV12816BLL-55TA1	TSOP
	IS65WV12816BLL-55BA1	mini BGA (6mm x 8mm)
	IS65WV12816BLL-55B2A1	mini BGA (6mm x 8mm), 2 CS Option
70	IS65WV12816BLL-70TA1	TSOP
	IS65WV12816BLL-70BA1	mini BGA (6mm x 8mm)
	IS65WV12816BLL-70B2A1	mini BGA (6mm x 8mm), 2 CS Option

ORDERING INFORMATION (continual)

IS65WV12816BLL (2.5V - 3.6V)

TEMPERATURE RANGE (A2): –40°C TO +105°C

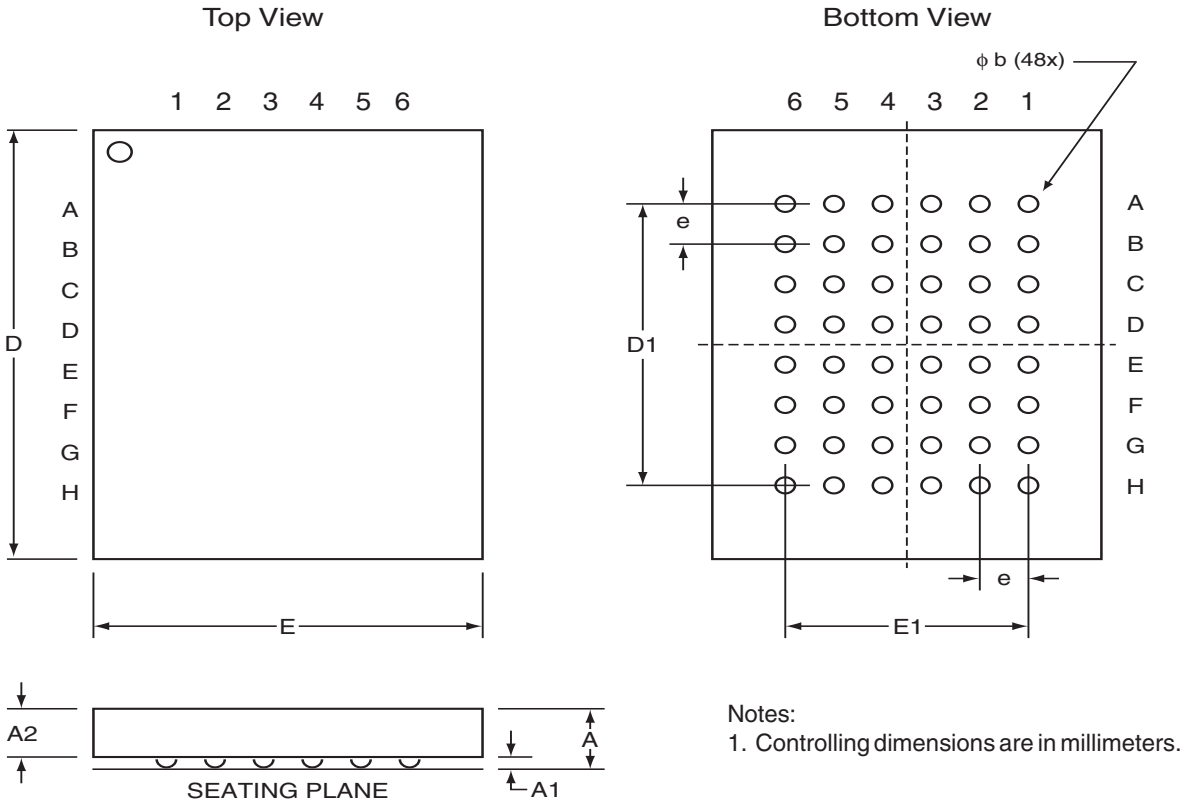
Speed (ns)	Order Part No.	Package
55	IS65WV12816BLL-55TA2	TSOP
	IS65WV12816BLL-55BA2	mini BGA (6mm x 8mm)
	IS65WV12816BLL-55B2A2	mini BGA (6mm x 8mm), 2 CS Option
70	IS65WV12816BLL-70TA2	TSOP
	IS65WV12816BLL-70BA2	mini BGA (6mm x 8mm)
	IS65WV12816BLL-70B2A2	mini BGA (6mm x 8mm), 2 CS Option

Temperature Range (A3): –40°C to +125°C

Speed (ns)	Order Part No.	Package
55	IS65WV12816BLL-55TA3	TSOP
	IS65WV12816BLL-55TLA3	TSOP, Lead-free
	IS65WV12816BLL-55BA3	mini BGA (6mm x 8mm)
	IS65WV12816BLL-55BLA3	mini BGA (6mm x 8mm), Lead-free
	IS65WV12816BLL-55B2A3	mini BGA (6mm x 8mm), 2 CS Option
70	IS65WV12816BLL-70TA3	TSOP
	IS65WV12816BLL-70BA3	mini BGA (6mm x 8mm)
	IS65WV12816BLL-70B2A3	mini BGA (6mm x 8mm), 2 CS Option

PACKAGING INFORMATION

Mini Ball Grid Array
Package Code: B (48-pin)



Notes:
1. Controlling dimensions are in millimeters.

mBGA - 6mm x 8mm

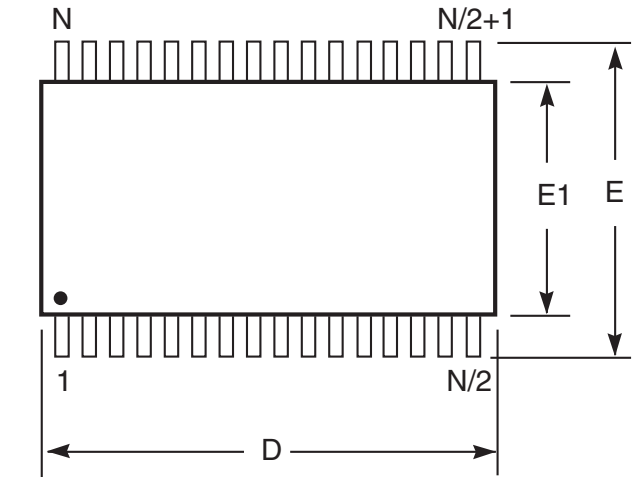
	MILLIMETERS			INCHES		
Sym.	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
N0. Leads		**48**				
A	—	—	1.20	—	—	0.047
A1	0.24	—	0.30	0.009	—	0.012
A2	0.60	—	—	0.024	—	—
D	7.90	—	8.10	0.311	—	0.319
D1		5.25 BSC			0.207 BSC	
E	5.90	—	6.10	0.232	—	0.240
E1		3.75 BSC			0.148 BSC	
e		0.75 BSC			0.030 BSC	
b	0.30	0.35	0.40	0.012	0.014	0.016

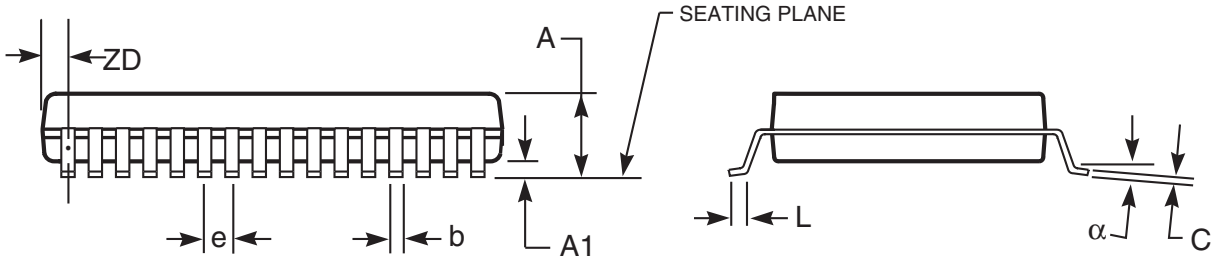
mBGA - 8mm x 10mm

	MILLIMETER			INCHES		
Sym.	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
N0. Leads		**48**				
A	—	—	1.20	—	—	0.047
A1	0.24	—	0.30	0.009	—	0.012
A2	0.60	—	—	0.024	—	—
D	9.90	—	10.10	0.390	—	0.398
D1		5.25 BSC			0.207 BSC	
E	7.90	—	8.10	0.311	—	0.319
E1		3.75 BSC			0.148 BSC	
e		0.75 BSC			0.030 BSC	
b	0.30	0.35	0.40	0.012	0.014	0.016

PACKAGING INFORMATION

Plastic TSOP
Package Code: T (Type II)





Notes:
1. Controlling dimension: millimieters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

Plastic TSOP (T - Type II)

	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Ref. Std.												
No. Leads (N)		**32**				**44**				**50**		
A	—	1.20	—	0.047	—	1.20	—	0.047	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006
b	0.30	0.52	0.012	0.020	0.30	0.45	0.012	0.018	0.30	0.45	0.012	0.018
C	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008
D	20.82	21.08	0.820	0.830	18.31	18.52	0.721	0.729	20.82	21.08	0.820	0.830
E1	10.03	10.29	0.391	0.400	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E	11.56	11.96	0.451	0.466	11.56	11.96	0.455	0.471	11.56	11.96	0.455	0.471
e	1.27 BSC		0.050 BSC		0.80 BSC		0.032 BSC		0.80 BSC		0.031 BSC	
L	0.40	0.60	0.016	0.024	0.41	0.60	0.016	0.024	0.40	0.60	0.016	0.024
ZD	0.95 REF		0.037 REF		0.81 REF		0.032 REF		0.88 REF		0.035 REF	
α	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°