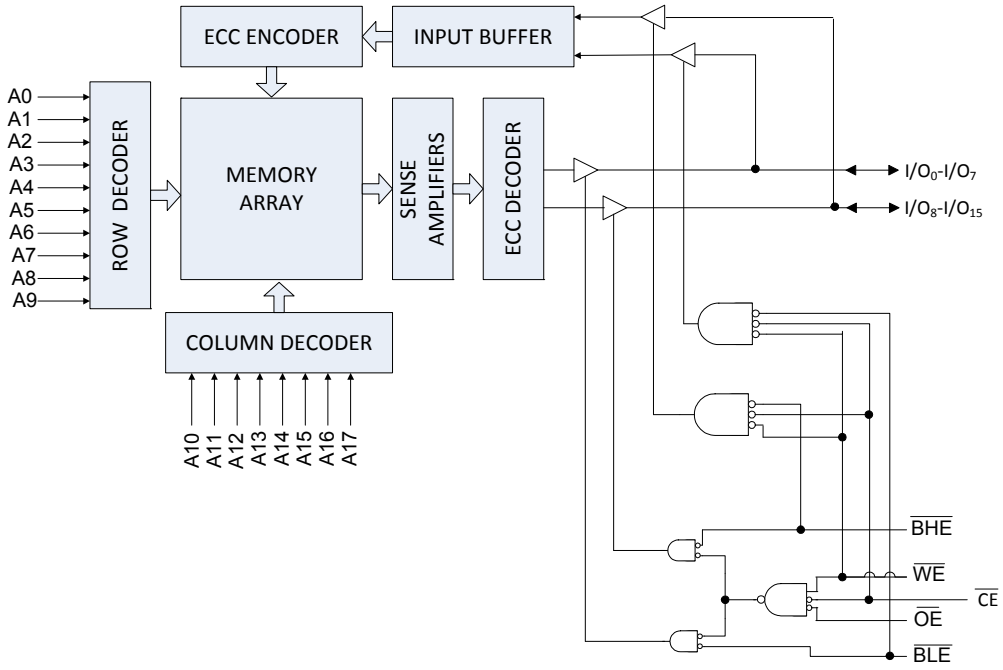
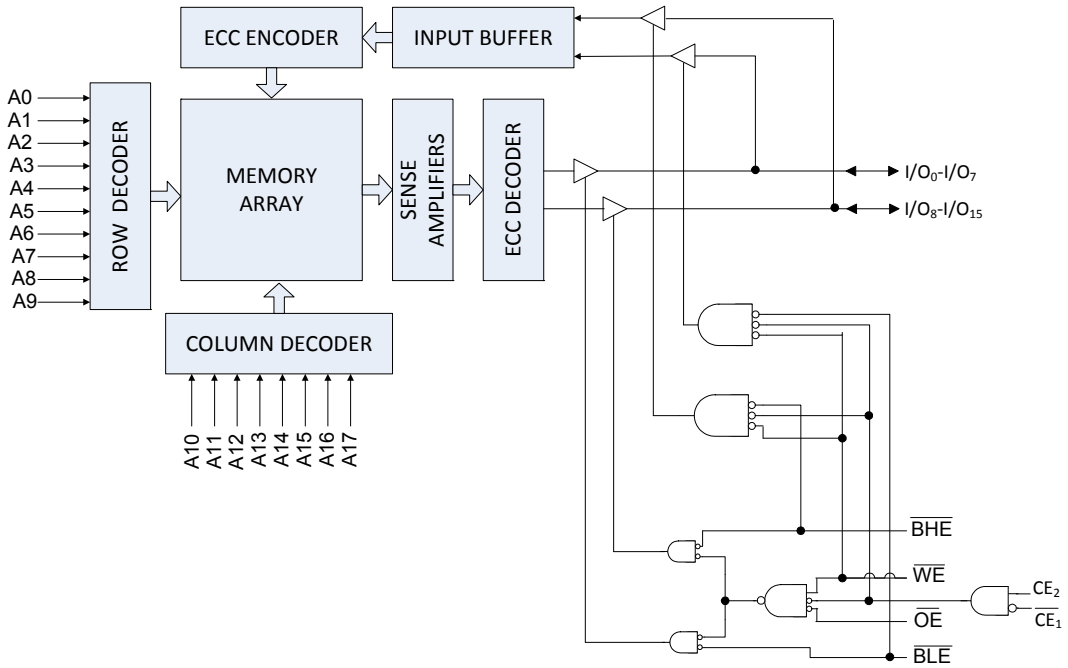
Logic Block Diagram – CY62147G



Logic Block Diagram – CY621472G



Contents

Pin Configuration – CY62147G

Figure 1. 48-ball VFBGA pinout (Single Chip Enable without ERR) – CY62147G [2]

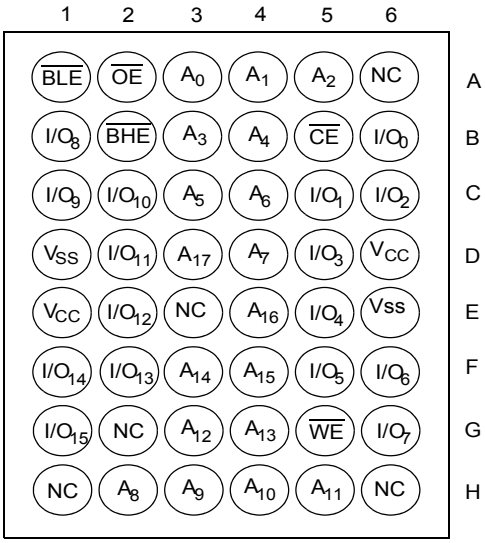
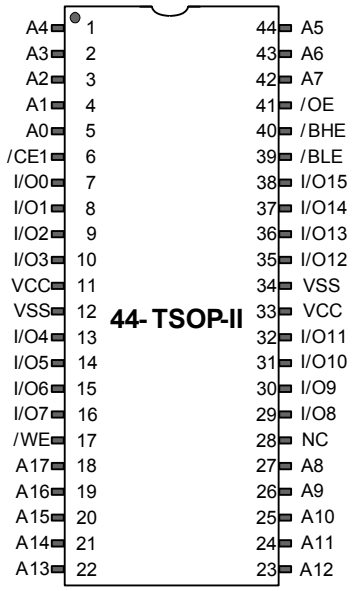


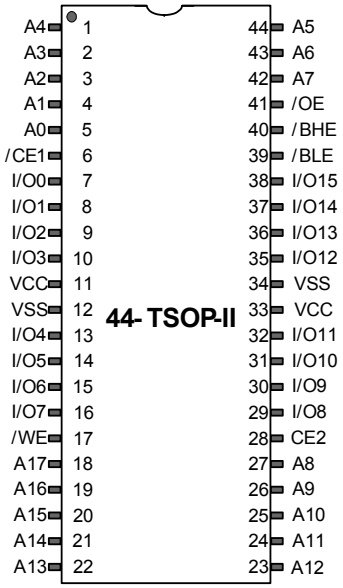
Figure 2. 44-pin TSOP II pinout (Single Chip Enable without ERR) – CY62147G [2]



Note
2. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.

Pin Configuration – CY621472G

Figure 3. 44-pin TSOP II pinout (Dual Chip Enable without ERR) – CY621472G



Product Portfolio

Product	Features and Options (see the Pin Configurations section)	Range	V_{CC} Range (V)	Speed (ns)	Power Dissipation			
					Operating I_{CC}, (mA) f = f_{max}		Standby, I_{SB2} (µA)	
					Typ [3]	Max	Typ [3]	Max
CY62147G30/ CY621472G30	Single or dual Chip Enables	Automotive-A	2.2 V–3.6 V	45	15	20	3.5	8.7
		Automotive-E		55	15	24	–	35

Note
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for a V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to + 150 °C

Ambient temperature with power applied ..... –55 °C to + 125 °C

Supply voltage to ground potential [4] ..... –0.3 V to V_{CC} + 0.3 V

DC voltage applied to outputs in HI-Z state [4] ..... –0.3 V to V_{CC} + 0.3 V

DC input voltage [4] ..... –0.3 V to V_{CC} + 0.3 V

Output current into outputs (in low state) ..... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) ..... >2001 V

Latch-up current ..... >140 mA

Operating Range

Grade	Ambient Temperature	V_{CC}
Automotive-A	–40 °C to +85 °C	2.2 V to 3.6 V
Automotive-E	–40 °C to +125 °C	

DC Electrical Characteristics

Over the operating range

Parameter	Description		Test Conditions		45 ns (Automotive-A)			55 ns (Automotive-E)			Unit
					Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH voltage	2.2 V to 2.7 V	V_{CC} = Min, I_{OH} = –0.1 mA		2	–	–	2	–	–	V
		2.7 V to 3.6 V	V_{CC} = Min, I_{OH} = –1.0 mA		2.4	–	–	2.4	–	–	
V_{OL}	Output LOW voltage	2.2 V to 2.7 V	V_{CC} = Min, I_{OL} = 0.1 mA		–	–	0.4	–	–	0.4	V
		2.7 V to 3.6 V	V_{CC} = Min, I_{OL} = 2.1 mA		–	–	0.4	–	–	0.4	
V_{IH}	Input HIGH voltage	2.2 V to 2.7 V	–		1.8	–	V_{CC} + 0.3[4]	2	–	V_{CC} + 0.3[4]	V
		2.7 V to 3.6 V	–		2	–	V_{CC} + 0.3[4]	2	–	V_{CC} + 0.3[4]	
V_{IL}	Input LOW voltage	2.2 V to 2.7 V	–		–0.3[4]	–	0.6	–0.3[4]	–	0.6	V
		2.7 V to 3.6 V	–		–0.3[4]	–	0.8	–0.3[4]	–	0.8	
I_{IX}	Input leakage current		GND ≤ V_{IN} ≤ V_{CC}		–1	–	+1	–5	–	+5	µA
I_{OZ}	Output leakage current		GND ≤ V_{OUT} ≤ V_{CC}, Output disabled		–1	–	+1	–5	–	+5	µA
I_{CC}	V_{CC} operating supply current		Max V_{CC}, I_{OUT} = 0 mA, CMOS levels	f = f_{MAX}	–	15	20	–	15	24	mA
				f = 1 MHz	–	3.5	6	–	3.5	10	

Note
4. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 20 ns.

DC Electrical Characteristics (continued)

Over the operating range

Parameter	Description	Test Conditions	45 ns (Automotive-A)			55 ns (Automotive-E)			Unit
			Min	Typ	Max	Min	Typ	Max	
I_{SB1}[5]	Automatic power down current – CMOS inputs; V_{CC} = 2.2 V to 3.6 V and 4.5 V to 5.5 V	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, f = f_{max} (address and data only), f = 0 ($\overline{OE}$, and $\overline{WE}$), Max V_{CC}	–	3.5	8.7	–	–	35	µA
I_{SB2}[5]	Automatic power down current – CMOS inputs V_{CC} = 2.2 V to 3.6 V and 4.5 V to 5.5 V	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, f = 0, Max V_{CC}	–	3.5	8.7	–	–	35	µA

Note
5. Chip enables ($\overline{CE}_1$ and CE_2) must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

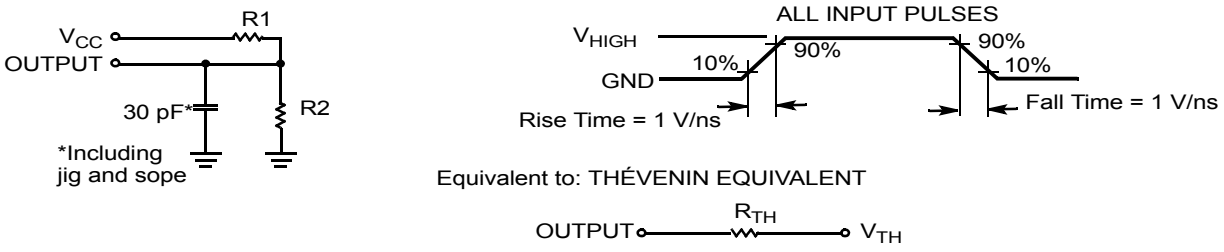
Parameter [6]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [6]	Description	Test Conditions	48-ball VFBGA	44-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	31.17	66.82	°C/W
Θ_{JC}	Thermal resistance (junction to case)		14.90	15.97	°C/W

AC Test Loads and Waveforms

Figure 4. AC Test Loads and Waveforms [7]



Parameters	1.8 V	2.5 V	3.0 V	5.0 V	Unit
R1	13500	16667	1103	1800	Ω
R2	10800	15385	1554	990	Ω
R_{TH}	6000	8000	645	639	Ω
V_{TH}	0.80	1.20	1.75	1.77	V

Notes
6. Tested initially and after any design or process changes that may affect these parameters.
7. Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)}$ ≥ 100 µs or stable at $V_{CC(min)}$ ≥ 100 µs.

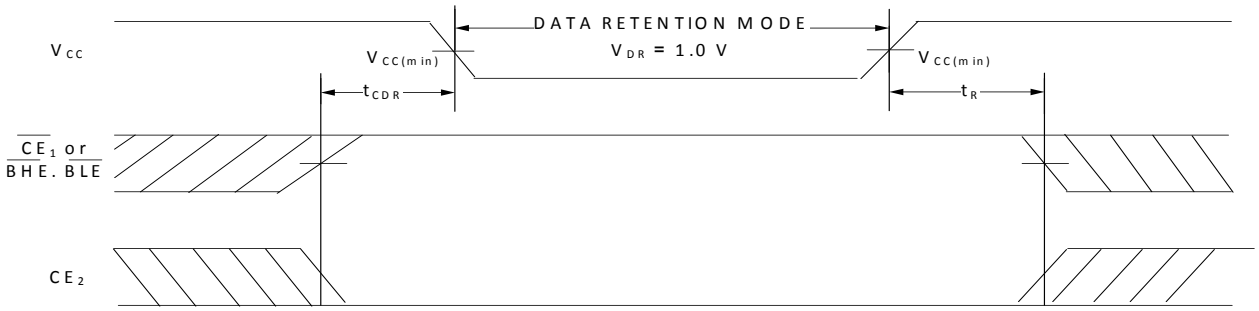
Data Retention Characteristics

Over the operating range

Parameter	Description	Conditions	(Automotive-A)			(Automotive-E)			Unit
			Min	Typ[8]	Max	Min	Typ[8]	Max	
V_{DR}	V_{CC} for data retention		1	–	–	1	–	–	V
I_{CCDR}[9, 10]	Data retention current	Vcc = 1.2 V, $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	–	13	–	–	50	µA
t_{CDR}[11]	Chip deselect to data retention time		0	–	–	0	–	–	ns
t_R[11, 12]	Operation recovery time		45	–	–	55	–	–	ns

Data Retention Waveform

Figure 5. Data Retention Waveform [13]



Notes

8. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.
9. Chip enables ($\overline{CE}_1$ and CE_2) must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
10. I_{CCDR} is guaranteed only after the device is first powered up to $V_{CC(min)}$ and then brought down to V_{DR}.
11. These parameters are guaranteed by design.
12. Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.
13. $\overline{BHE}$.$\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

AC Switching Characteristics

Parameter [14]	Description	45 ns		55 ns		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	45	–	55	–	ns
t_{AA}	Address to data valid	–	45	–	55	ns
t_{OHA}	Data hold from address change	10	–	10	–	ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to data valid	–	45	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	–	25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low impedance[15, 16]	5	–	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to HI-Z[15, 16, 17]	–	18	–	18	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low impedance[15, 16]	10	–	10	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to HI-Z[15, 16, 17]	–	18	–	18	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to power-up[16]	0	–	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to power-down[16]	–	45	–	55	ns
t_{DBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to data valid	–	45	–	55	ns
t_{LZBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low impedance[15, 16]	5	–	5	–	ns
t_{HZBE}	$\overline{BLE}$ / $\overline{BHE}$ HIGH to HI-Z[15, 16, 17]	–	18	–	18	ns
Write Cycle [18, 19]						
t_{WC}	Write cycle time	45	–	55	–	ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to write end	35	–	40	–	ns
t_{AW}	Address setup to write end	35	–	40	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	40	–	ns
t_{BW}	$\overline{BLE}$ / $\overline{BHE}$ LOW to write end	35	–	45	–	ns
t_{SD}	Data setup to write end	25	–	25	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to HI-Z[15, 16, 17]	–	18	–	20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low impedance[15, 16]	10	–	10	–	ns

Notes

14. Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$ V). Test conditions for the read cycle use output loading shown in AC Test Loads and Waveforms section, unless specified otherwise.
15. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
16. These parameters are guaranteed by design.
17. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
18. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}_1$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$, or both = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
19. The minimum pulse width in Write Cycle No 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 6. Read Cycle No. 1 of CY62147G/CY621472G (Address Transition Controlled) [20, 21]

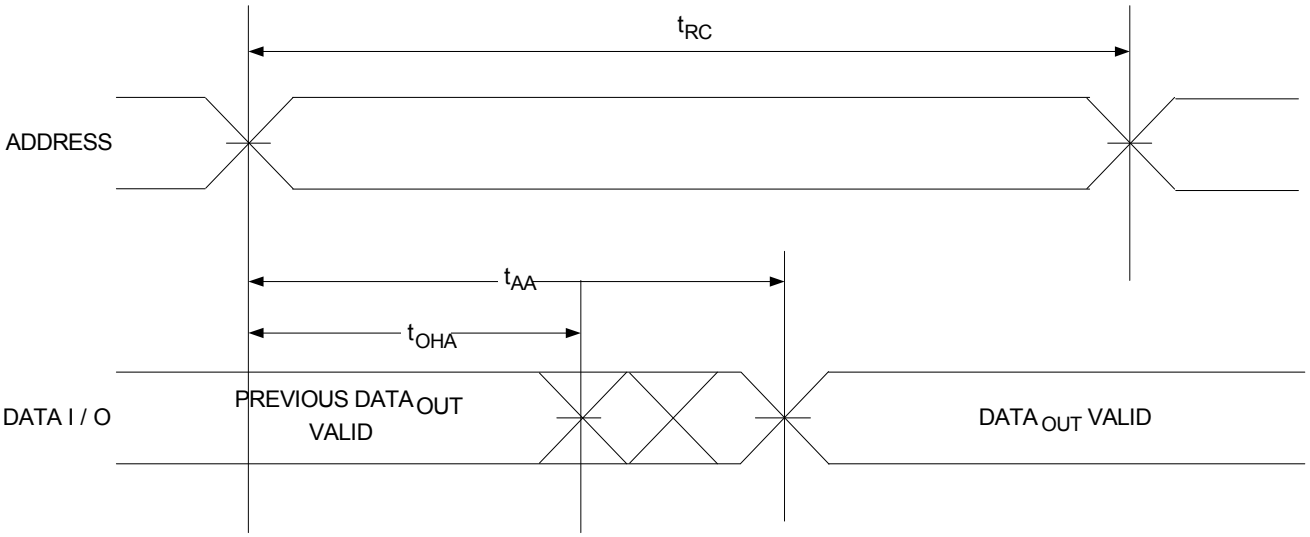
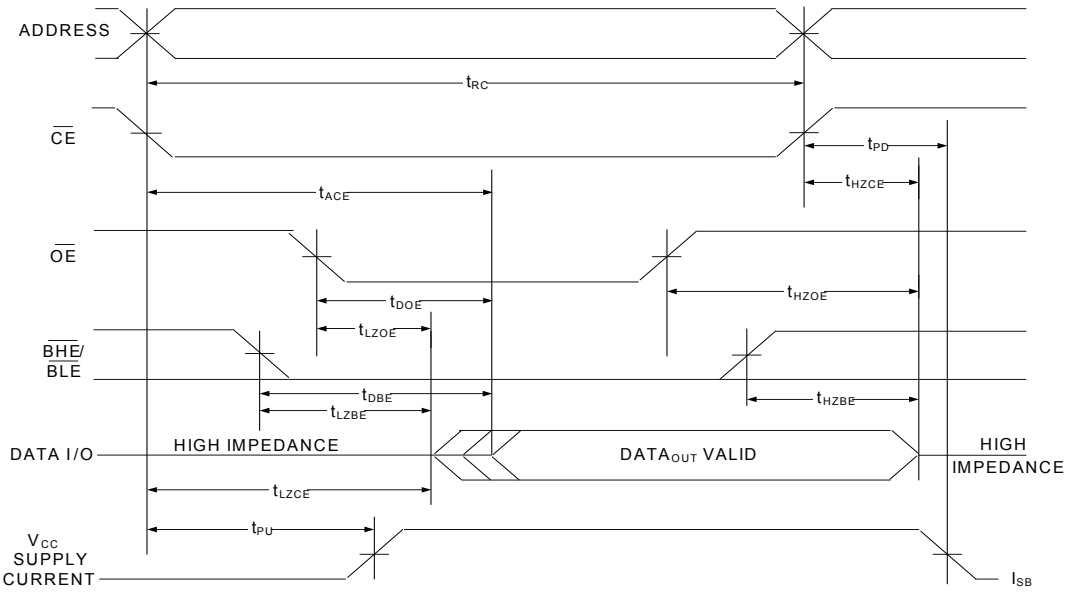


Figure 7. Read Cycle No. 2 ($\overline{OE}$ Controlled) [21, 22, 23]

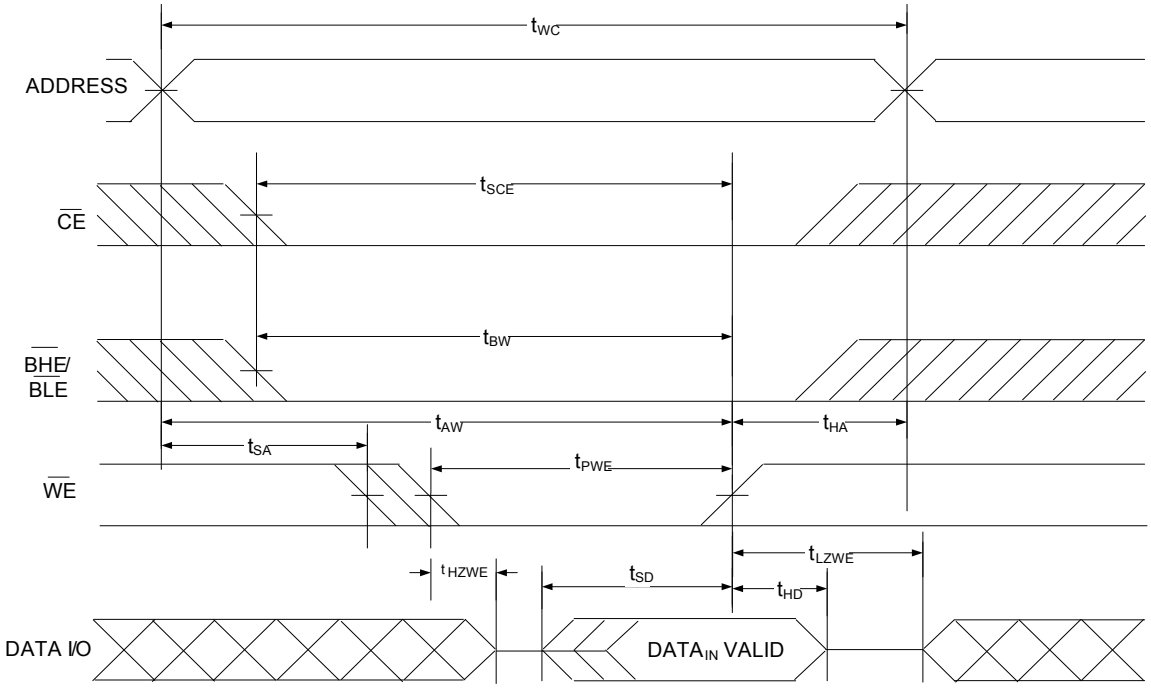


Notes

20. The device is continuously selected. $\overline{OE}$ = V_{IL}, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}.
21. $\overline{WE}$ is HIGH for Read cycle.
22. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
23. Address valid prior to or coincident with $\overline{CE}$ LOW transition.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 1 (WE Controlled) [24, 25, 26]



Notes

24. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
25. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}_1$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
26. Data I/O is in a HI-Z state if $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH} or $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 2 ($\overline{CE}$ Controlled) [27, 28, 29]

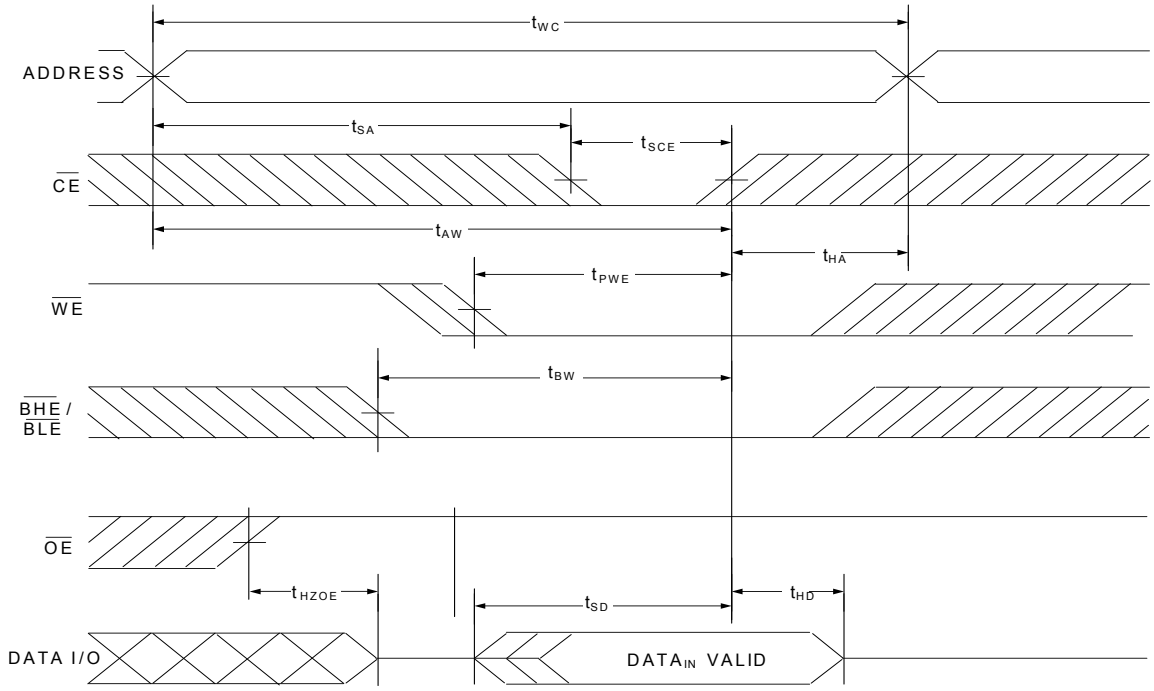
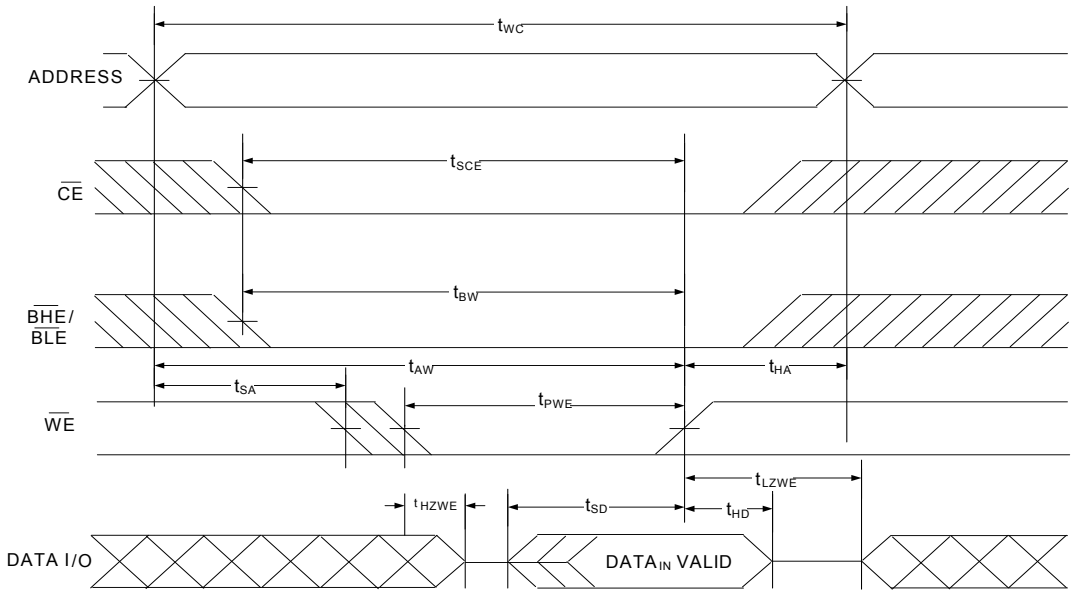


Figure 10. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [27, 28, 29, 30]

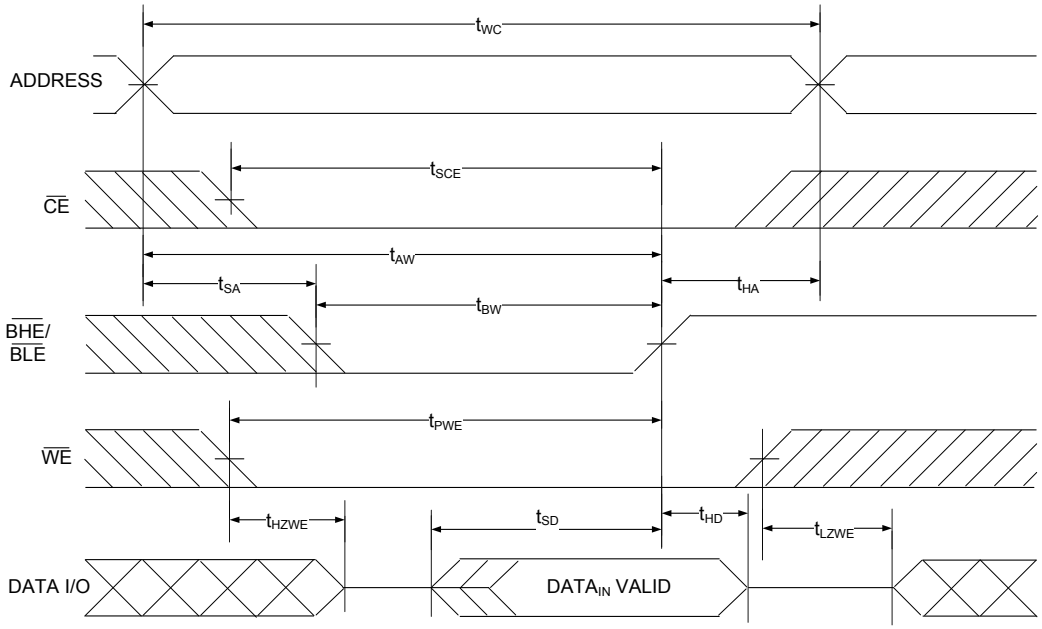


Notes

27. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
28. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}_1$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
29. Data I/O is in HI-Z state if $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH} or $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
30. The minimum write pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be sum of t_{HZWE} and t_{SD}.

Switching Waveforms (continued)

Figure 11. Write Cycle No. 4 (BHE/BLE Controlled) [31, 32, 33]



Notes

31. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
32. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}_1$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
33. Data I/O is in a HI-Z state if $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH} or $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.

Truth Table – CY62147G/CY621472G

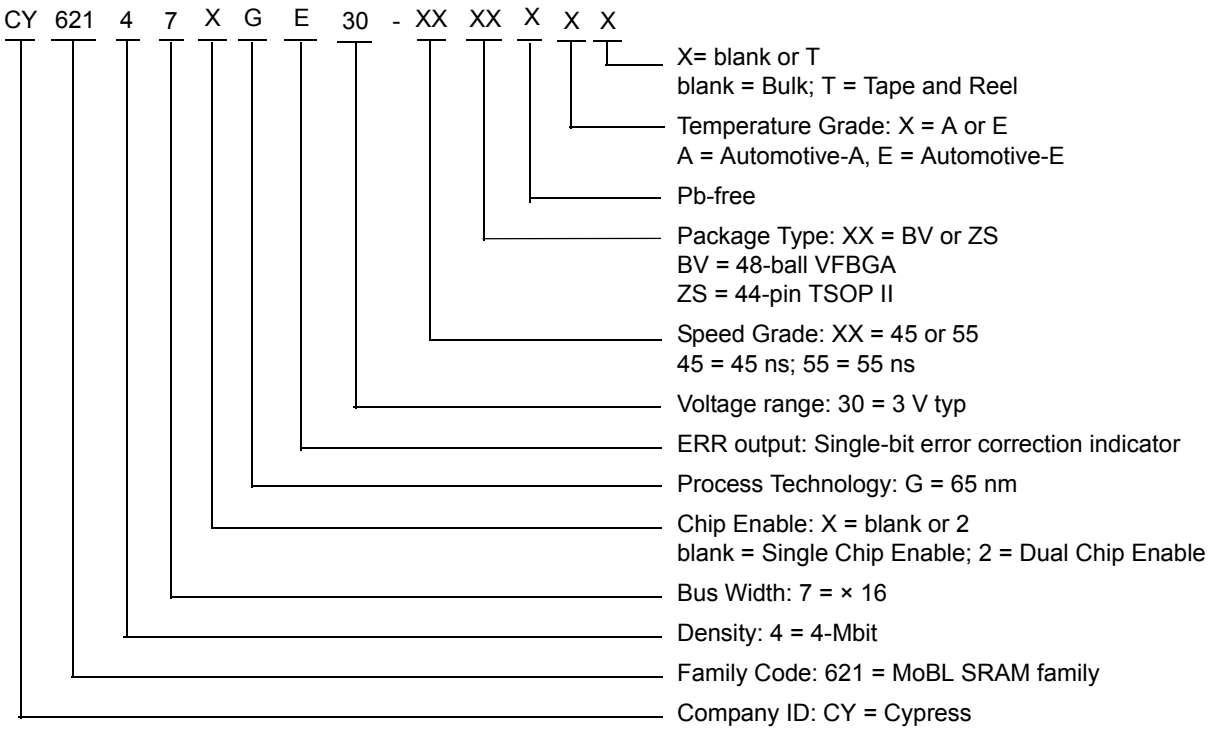
$\overline{CE}$ / $\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X[34]	X	X	X	X	HI-Z	Deselect/Power-down	Standby (I_{SB})
X[34]	L	X	X	X	X	HI-Z	Deselect/Power-down	Standby (I_{SB})
X[34]	X[34]	X	X	H	H	HI-Z	Deselect/Power-down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	Data Out (I/O_0–I/O_7); HI-Z (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	L	H	HI-Z (I/O_0–I/O_7); Data Out (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	H	L	H	HI-Z	Output disabled	Active (I_{CC})
L	H	H	H	H	L	HI-Z	Output disabled	Active (I_{CC})
L	H	H	H	L	L	HI-Z	Output disabled	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	Data In (I/O_0–I/O_7); HI-Z (I/O_8–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	L	H	HI-Z (I/O_0–I/O_7); Data In (I/O_8–I/O_{15})	Write	Active (I_{CC})

Note
34. The 'X' (Don't care) state for the chip enables refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type	Operating Range
45	2.2 V–3.6 V	CY62147G30-45BVXA	51-85150	48-ball VFBGA (6 × 8 × 1 mm), Single Chip Enable	Automotive-A
		CY62147G30-45BVXAT	51-85150	48-ball VFBGA (6 × 8 × 1 mm), Single Chip Enable, Tape and Reel	
		CY62147G30-45ZSXA	51-85087	44-pin TSOP II without ERR	
		CY62147G30-45ZSXAT	51-85087	44-pin TSOP II without ERR, Tape and Reel	
		CY621472G30-45ZSXA	51-85087	44-pin TSOP II, Dual Chip Enable	
		CY621472G30-45ZSXAT	51-85087	44-pin TSOP II, Dual Chip Enable, Tape and Reel	
55	2.2 V–3.6 V	CY62147G30-55BVXE	51-85150	48-ball VFBGA (6 × 8 × 1 mm), Single Chip Enable	Automotive-E
		CY62147G30-55BVXET	51-85150	48-ball VFBGA (6 × 8 × 1 mm), Single Chip Enable, Tape and Reel	
		CY62147G230-55ZSXE	51-85087	44-pin TSOP II, Dual Chip Enable	
		CY62147G230-55ZSXET	51-85087	44-pin TSOP II, Dual Chip Enable, Tape and Reel	
		CY62147G30-55ZSXE	51-85087	44-pin TSOP II	
		CY62147G30-55ZSXET	51-85087	44-pin TSOP II, Tape and Reel	

Ordering Code Definitions



Package Diagrams

Figure 12. 44-pin TSOP Z44-II Package Outline, 51-85087

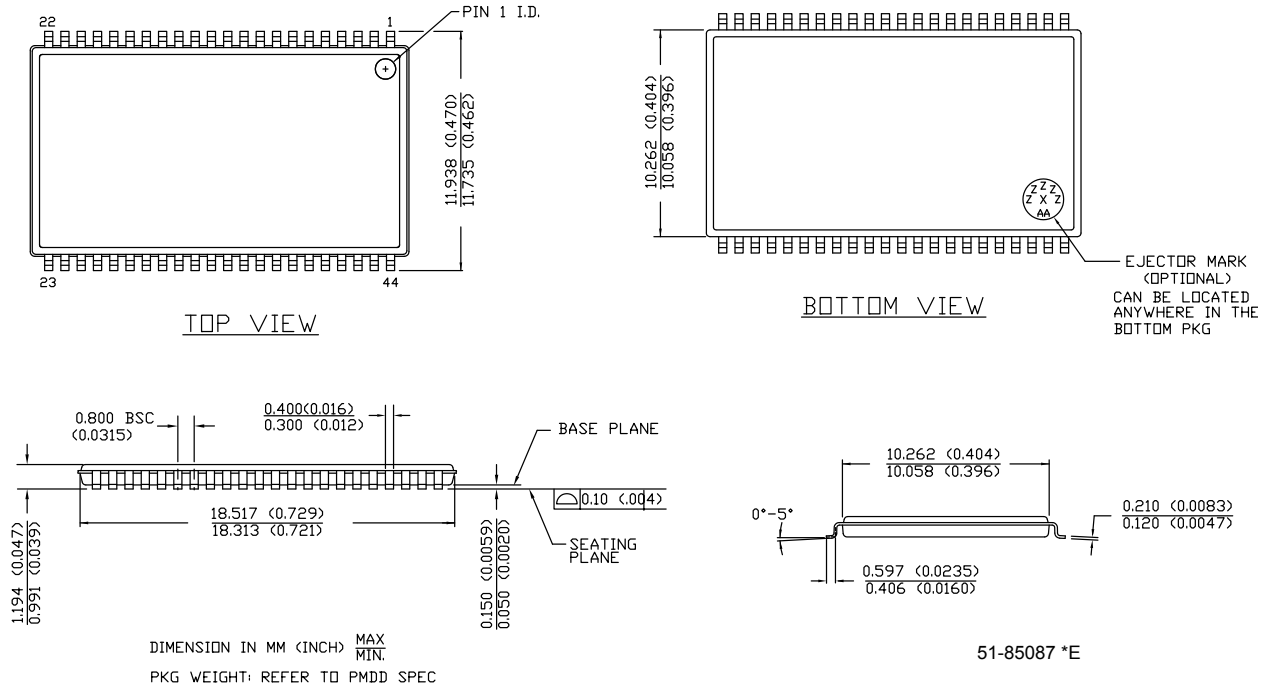
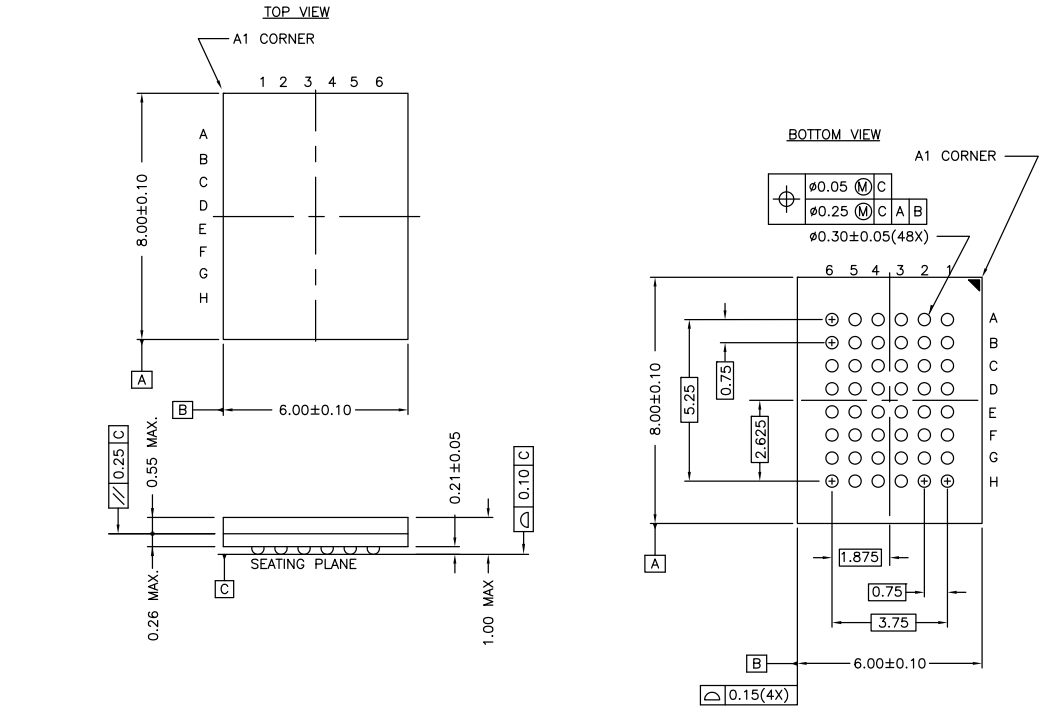


Figure 13. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150



NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62147G/CY621472G MoBL® Automotive, 4-Mbit (256K words × 16 bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-95424				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*B	5032662	NILE	12/01/2015	Changed status from Preliminary to Final.
*C	5428830	NILE	09/07/2016	Updated Maximum Ratings: Updated Note 4 (Replaced “2 ns” with “20 ns”). Updated DC Electrical Characteristics: Changed minimum value of V_{OH} parameter from 2.2 V to 2.4 V corresponding to Operating Range “2.7 V to 3.6 V” and Test Condition “V_{CC} = Min, I_{OH} = –1.0 mA”. Changed minimum value of V_{IH} parameter from 2.0 V to 1.8 V corresponding to Operating Range “2.2 V to 2.7 V”. Updated Ordering Information: Updated part numbers. Updated to new template.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Lighting & Power Control	cypress.com/powerpsoc
Memory	cypress.com/memory
PSoC	cypress.com/psoc
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless/RF	cypress.com/wireless

PSoC®Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Forums | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support