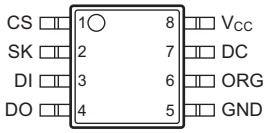
1. Pin Configurations and Pinouts

Table 1-1. Pin Configurations

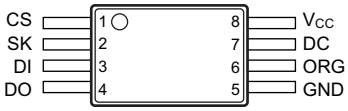
Pin Name	Function
CS	Chip Select
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
ORG	Internal Organization
SK	Serial Data Clock
V_{CC}	Power Supply

8-lead SOIC



(Top View)

8-lead TSSOP



(Top View)

Note: Drawings are not to scale.

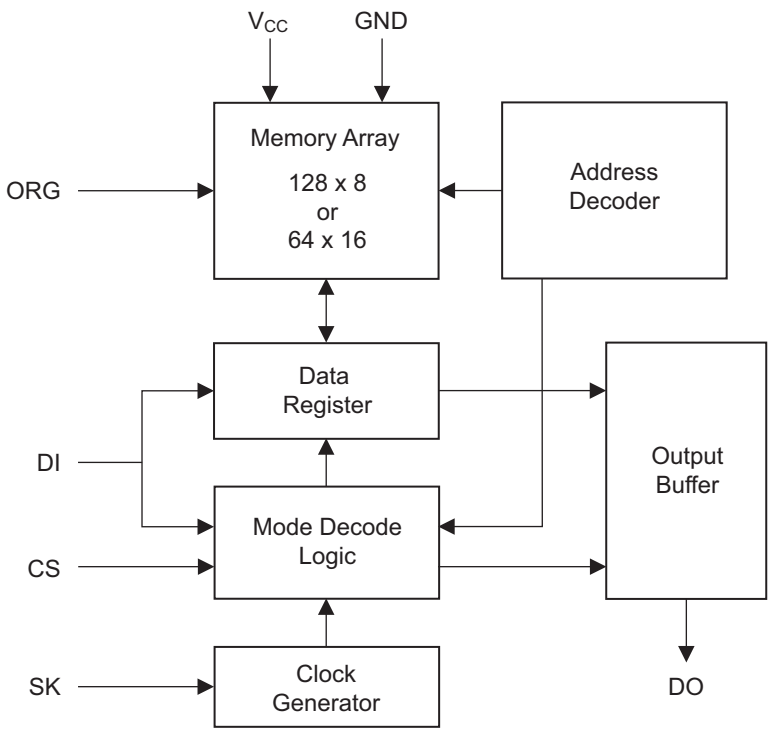
2. Absolute Maximum Ratings*

Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground	–1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0mA

*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

3. Block Diagram

Figure 3-1. Block Diagram



Note: When the ORG pin is connected to V_{CC}, the x16 organization is selected. When it is connected to ground, the x8 organization is selected.

4. Memory Organization

4.1 Pin Capacitance

Table 4-1. Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0MHz, V_{CC} = +5.0V (unless otherwise noted).

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance (CS, SK, DI)	5	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

4.2 DC Characteristics

Table 4-2. DC Characteristics

Applicable over recommended operating range from: T_A = -40° C to +125° C, V_{CC} = +2.5V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
V_{CC1}	Supply Voltage			2.5		5.5	V
V_{CC2}	Supply Voltage			4.5		5.5	V
I_{CC}	Supply Current	V_{CC} = 5.0V	Read at 1.0MHz		0.5	2.0	mA
			WRITE at 1.0MHz		0.5	2.0	mA
I_{SB1}	Standby Current	V_{CC} = 2.5V	CS = 0V		6.0	10.0	µA
I_{SB2}	Standby Current	V_{CC} = 5.0V	CS = 0V		10.0	15.0	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}			0.1	1.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}			0.1	1.0	µA
V_{IL1}[1]	Input Low Voltage	2.5V ≤ V_{CC} ≤ 5.5V		–0.6		0.8	
V_{IH1}[1]	Input High Voltage			2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	2.5V ≤ V_{CC} ≤ 5.5V	I_{OL} = 2.1mA			0.4	V
V_{OH1}	Output High Voltage		I_{OH} = –0.4mA	2.4			V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

4.3 AC Characteristics

Table 4-3. AC Characteristics

Applicable over recommended operating range from T_A = –40°C to + 125°C, V_{CC} = As Specified, CL = 1 TTL Gate and 100pF (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
f_{SK}	SK Clock Frequency	$4.5V \le V_{CC} \le 5.5V$		0		2	MHz
		$2.5V \le V_{CC} \le 5.5V$		0		1	
t_{SKH}	SK High Time	$4.5V \le V_{CC} \le 5.5V$		250			ns
		$2.5V \le V_{CC} \le 5.5V$		250			
t_{SKL}	SK Low Time	$4.5V \le V_{CC} \le 5.5V$		250			ns
		$2.5V \le V_{CC} \le 5.5V$		250			
t_{CS}	Minimum CS Low Time	$4.5V \le V_{CC} \le 5.5V$		250			ns
		$2.5V \le V_{CC} \le 5.5V$		250			
t_{CSS}	CS Setup Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$	50			ns
			$2.5V \le V_{CC} \le 5.5V$	50			
t_{DIS}	DI Setup Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$	100			ns
			$2.5V \le V_{CC} \le 5.5V$	100			
t_{CSH}	CS Hold Time	Relative to SK		0			ns
t_{DIH}	DI Hold Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$	100			ns
			$2.5V \le V_{CC} \le 5.5V$	100			
t_{PD1}	Output Delay to ‘1’	AC Test	$4.5V \le V_{CC} \le 5.5V$			250	ns
			$2.5V \le V_{CC} \le 5.5V$			500	
t_{PD0}	Output Delay to ‘0’	AC Test	$4.5V \le V_{CC} \le 5.5V$			250	ns
			$2.5V \le V_{CC} \le 5.5V$			500	
t_{SV}	CS to Status Valid	AC Test	$4.5V \le V_{CC} \le 5.5V$			250	ns
			$2.5V \le V_{CC} \le 5.5V$			250	
t_{DF}	CS to DO in High-impedance	AC Test	$4.5V \le V_{CC} \le 5.5V$			100	ns
		$CS = V_{IL}$	$2.5V \le V_{CC} \le 5.5V$			150	
t_{WP}	Write Cycle Time		$2.5V \le V_{CC} \le 5.5V$		3	10	ms
Endurance[1]	5.0V, 25°C			1,000,000			Write Cycles

Note: 1. This parameter is ensured by characterization only.

5. Instruction Set for the AT93C46D

Table 5-1. Instruction Set for the AT93C46D

Instruction	SB	Opcode	Address		Data		Comments
			x8	x16	x8	x16	
READ	1	10	$A_6 – A_0$	$A_5 – A_0$			Reads data stored in memory, at specified address.
EWEN	1	00	11XXXXX	11XXXX			Write enable must precede all programming modes.
ERASE	1	11	$A_6 – A_0$	$A_5 – A_0$			Erase memory location $A_n – A_0$.
WRITE	1	01	$A_6 – A_0$	$A_5 – A_0$	$D_7 – D_0$	$D_{15} – D_0$	Writes memory location $A_n – A_0$.
ERAL	1	00	10XXXXX	10XXXX			Erases all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
WRAL	1	00	01XXXXX	01XXXX	$D_7 – D_0$	$D_{15} – D_0$	Writes all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
EWDS	1	00	00XXXXX	00XXXX			Disables all programming. instructions.

Note: The ‘X’ in the address field represent don’t care values and must be clocked.

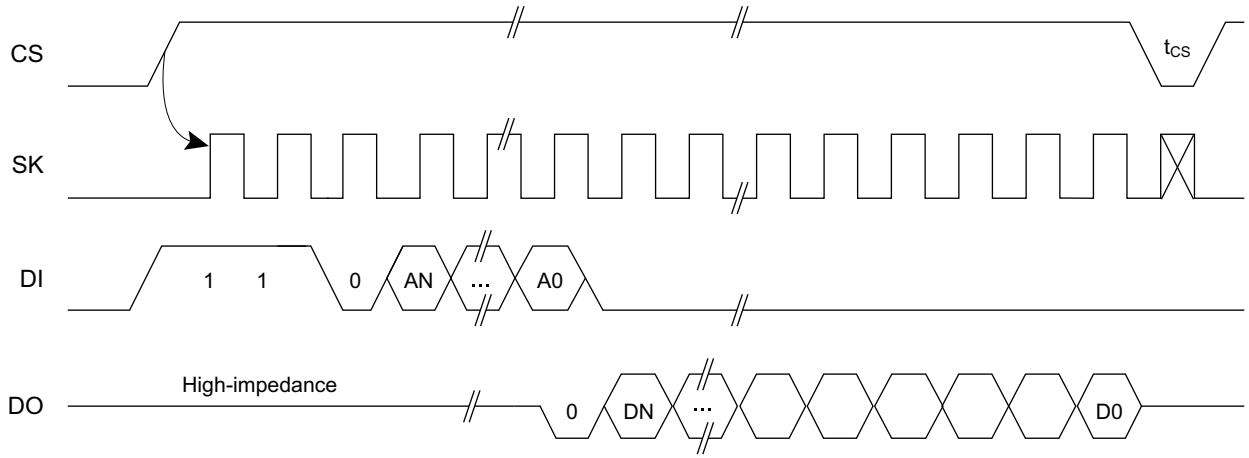
6. Functional Description

The AT93C46D is accessed via a simple and versatile 3-wire serial communication interface. The device operation is controlled by seven instructions issued by the host processor. *A valid instruction starts with a rising edge of CS* and consists of a Start bit (Logic 1) followed by the appropriate Opcode and the desired memory Address location.

READ: The READ instruction contains the address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the Serial Output (DO) pin. Output data changes are synchronized with the rising edges of Serial Clock (SK).

Note: A dummy bit (Logic 0) precedes the 8- or 16-bit data output string.

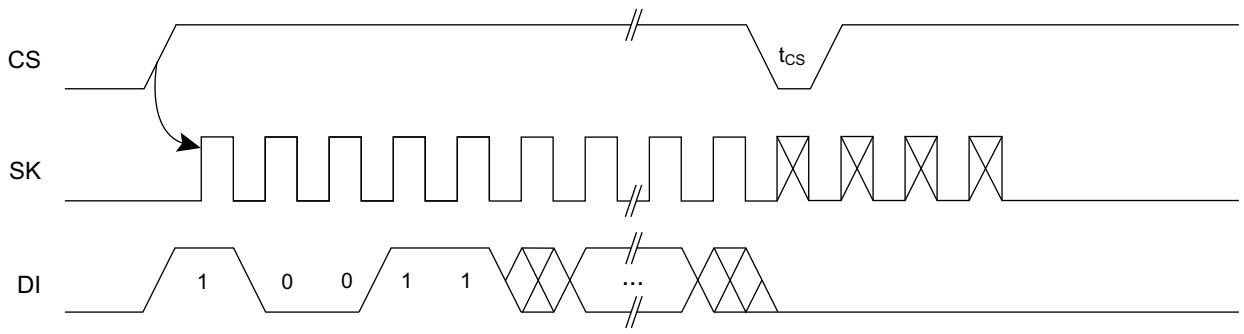
Figure 6-1. Read Timing



ERASE/WRITE (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when the power is first applied. An EWEN instruction must be executed first before any programming instructions can be carried out.

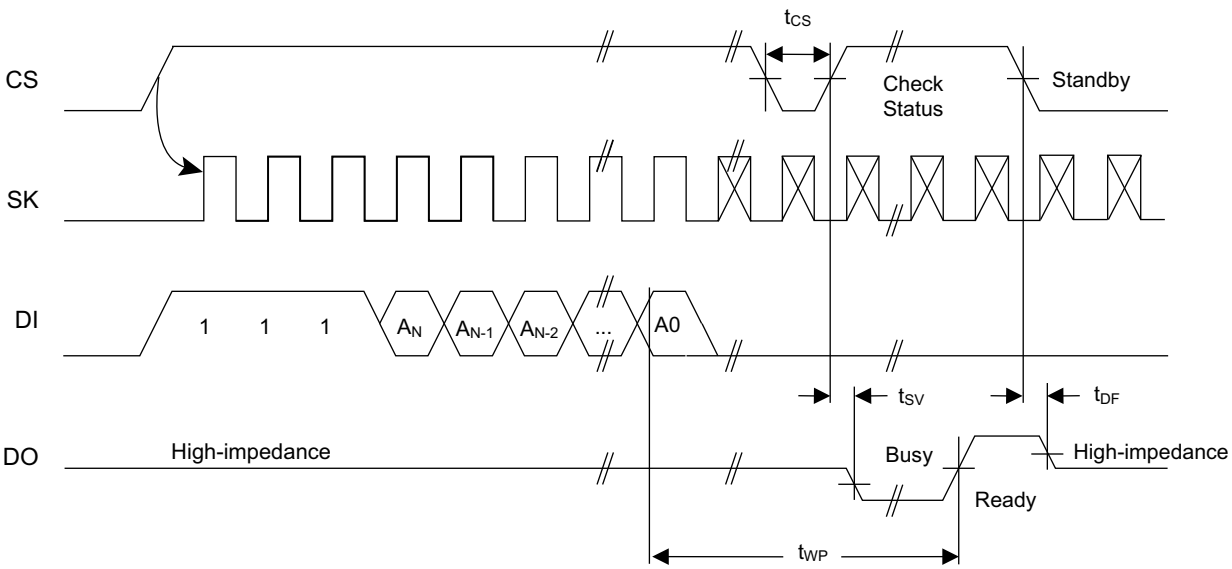
Note: Once in the EWEN state, programming remains enabled until an EWDS instruction is executed or V_{CC} power is removed from the part.

Figure 6-2. EWEN Timing



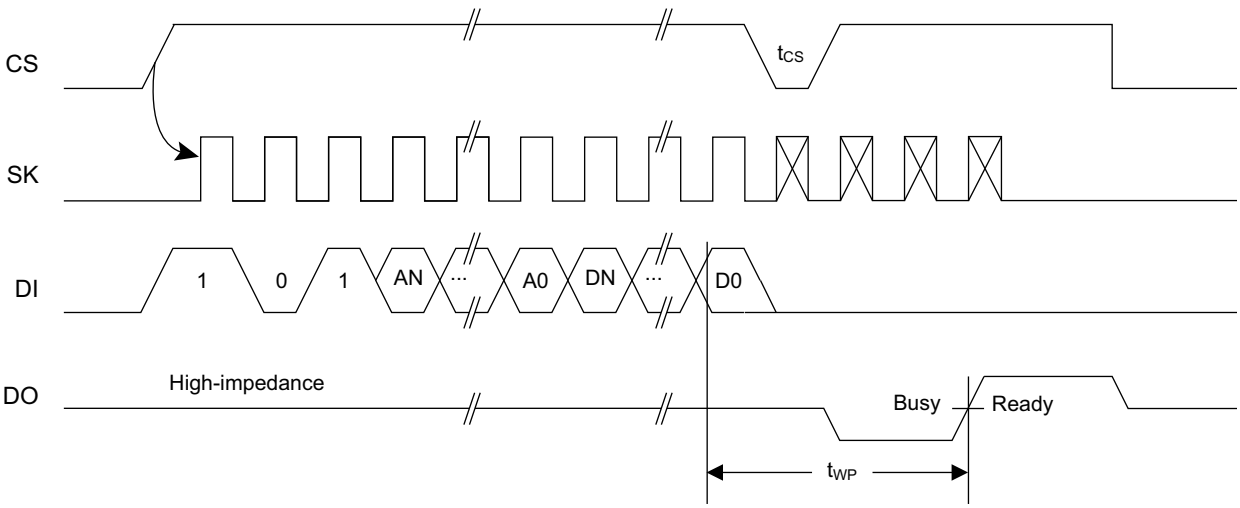
ERASE: The Erase instruction programs all of the bits in the specified memory location to the Logic 1 state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250ns (t_{CS}). A Logic 1 at the DO pin indicates that the selected memory location has been erased, and the part is ready for another instruction.

Figure 6-3. ERASE Timing



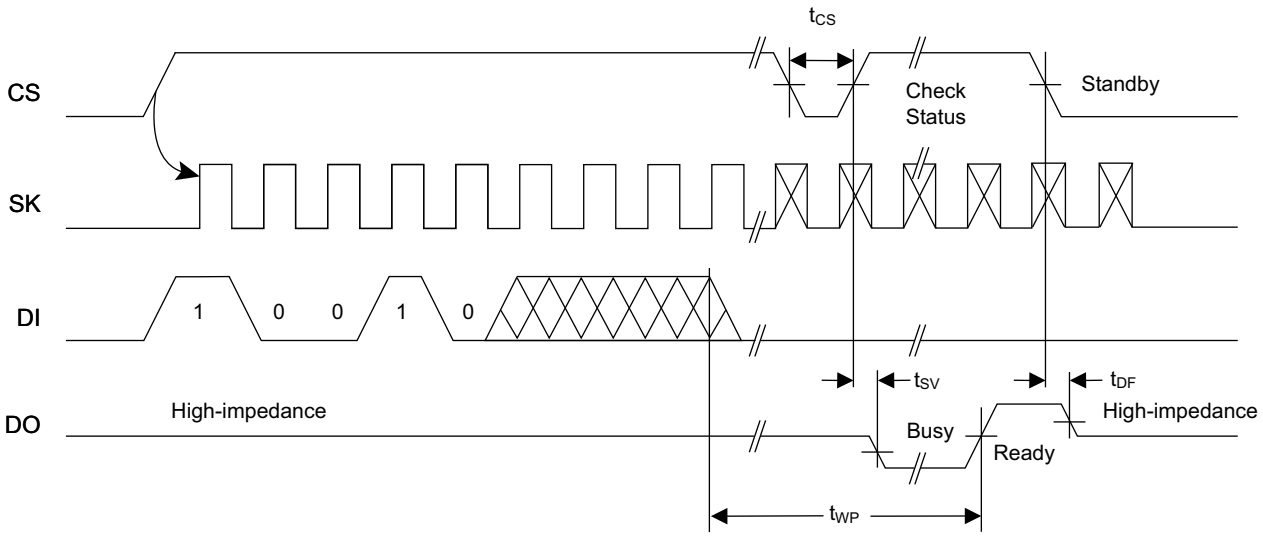
WRITE: The WRITE instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle, t_{WP}, starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250ns (t_{CS}). A Logic 0 at DO indicates that programming is still in progress. A Logic 1 indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions. *A Ready/Busy status cannot be obtained if the CS is brought high after the end of the self-timed programming cycle, t_{WP}.*

Figure 6-4. Write Timing



Erase All (ERAL): The ERAL instruction programs every bit in the memory array to the Logic 1 state and is primarily used for testing purposes. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250ns (t_{CS}). The ERAL instruction is valid only at V_{CC} = 5.0V ± 10%.

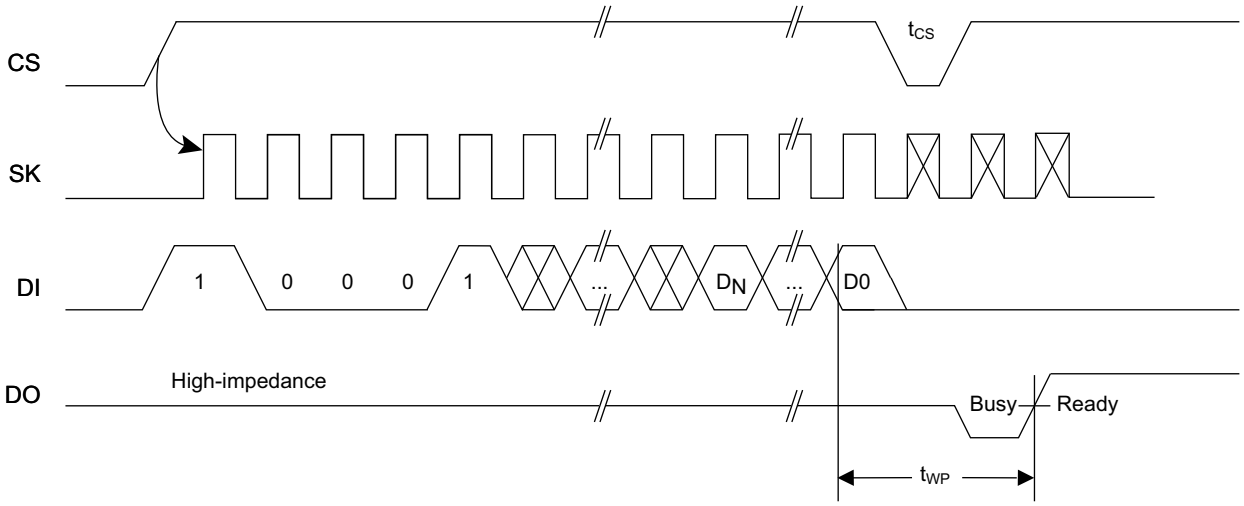
Figure 6-5. ERAL Timing[1]



Note: 1. Valid only at V_{CC} = 4.5V to 5.5V.

WRITE ALL (WRAL): The WRAL instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The WRAL instruction is valid only at V_{CC} = 5.0V ± 10%.

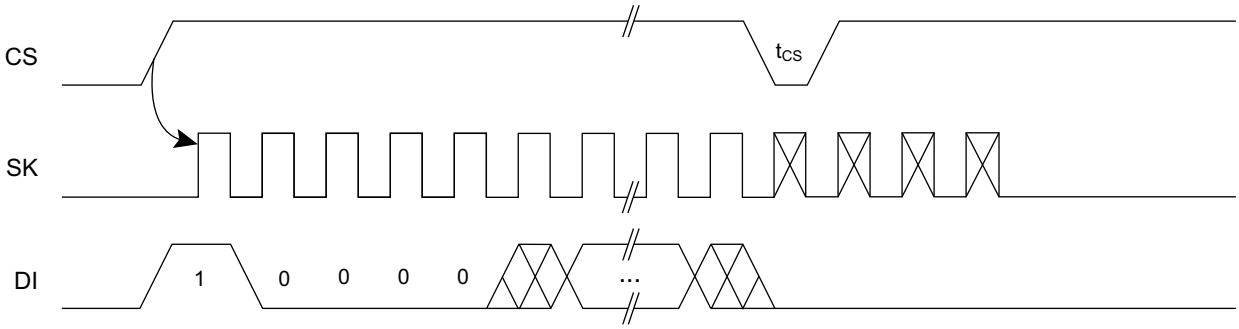
Figure 6-6. WRAL Timing[1]



Note: 1. Valid only at V_{CC} = 4.5V to 5.5V.

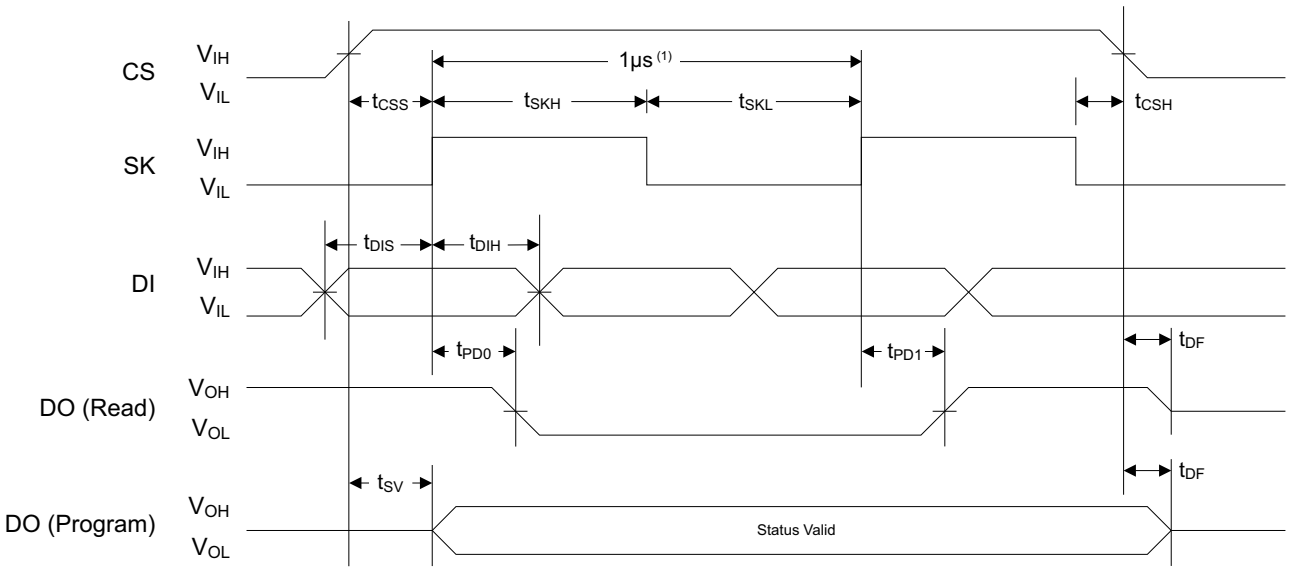
ERASE/WRITE DISABLE (EWDS): To protect against accidental data disturb, the EWDS instruction disables all the programming modes and should be executed after all programming operations. The operation of the READ instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

Figure 6-7. EWDS Timing



7. Timing Diagrams

Figure 7-1. Synchronous Data Timing

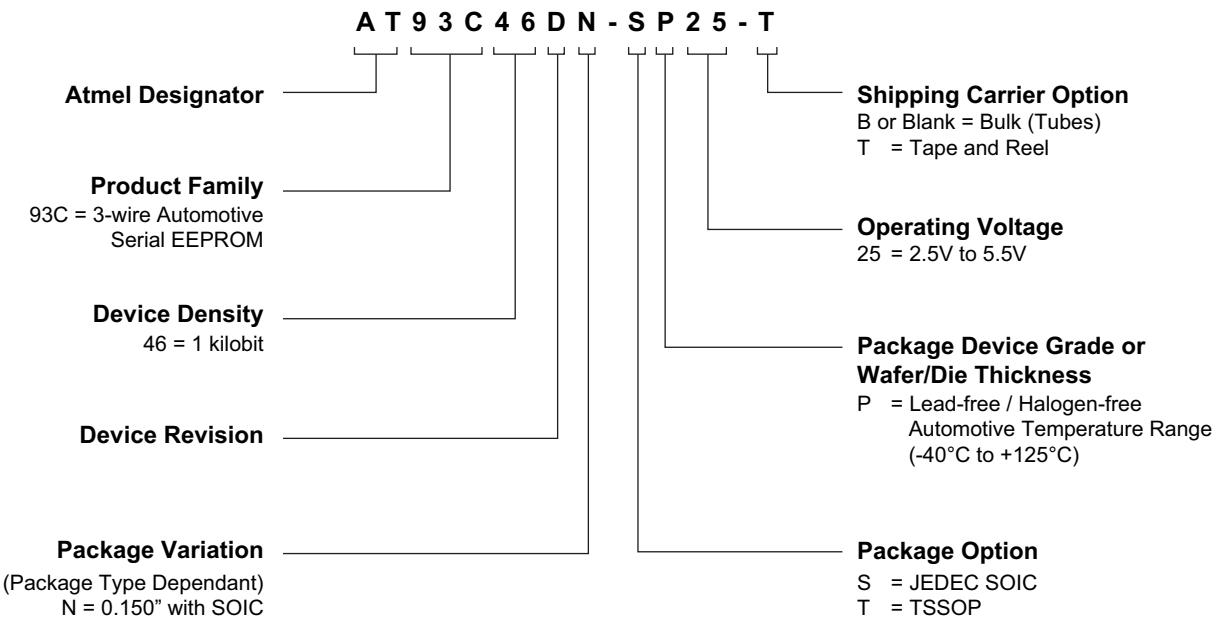


Note: 1. This is the minimum SK period.

Table 7-1. Organization Key for the Timing Diagrams

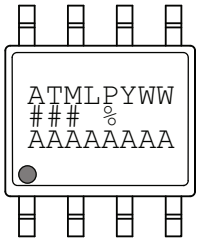
I/O	AT93C46D (1K)	
	x 8	x 16
A_N	A_6	A_5
D_N	D_7	D_{15}

8. Ordering Code Detail



9. Part Markings

AT93C46D: Automotive Package Marking Information

8-lead SOIC	8-lead TSSOP
	

Note: Lot Number and location of assembly and on the bottom side of the package.

Note 1: ● designates pin 1
Note 2: Package drawings are not to scale

Catalog Number Truncation			
AT93C46D		Truncation Code ###: 46D	
Date Codes			**Voltages**
Y = Year	M = Month	WW = Work Week of Assembly	% = Minimum Voltage
4: 2014 8: 2018 5: 2015 9: 2019 6: 2016 0: 2020 7: 2017 1: 2021	A: January B: February ... L: December	02: Week 2 04: Week 4 ... 52: Week 52	2: 2.5V min
Country of Assembly	**Lot Number**		**Grade/Lead Finish Material**
@ = Country of Assembly	AAA...A = Atmel Wafer Lot Number		P: Automotive/NiPdAu
Trace Code			**Atmel Truncation**
XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB.... YZ, ZZ			AT: Atmel ATM: Atmel ATML: Atmel

3/13/14

Atmel Package Mark Contact: DL-CSO-Assy_eng@atmel.com	**TITLE** **93C46DAM**, AT93C46D Automotive Package Marking Information	**DRAWING NO.** 93C46DAM	**REV.** A

10. Ordering Codes

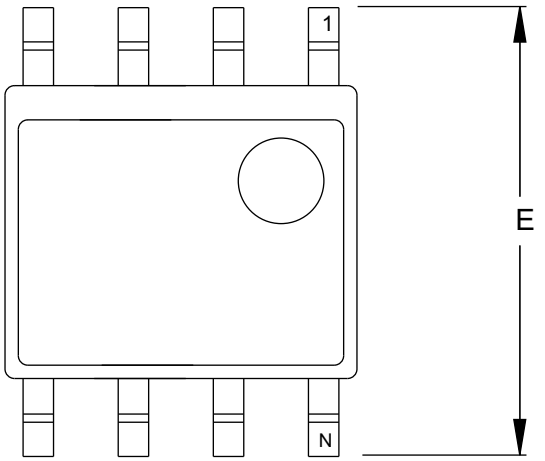
Atmel Ordering Code	Lead Finish	Package	Voltage	Operation Range
AT93C46DN-SP25-T[1]	Lead-free / Halogen-free	8S1	2.5V to 5.5V	Automotive Temperature (-40°C to 125°C)
AT93C46DN-SP25-B[2]				
AT93C46D-TP25-T[1]		8X		
AT93C46D-TP25-B[2]				

Notes:
1. Tape and reel delivery:
   - SOIC = 4,000 per reel.
   - TSSOP = 5,000 per reel.
2. Bulk delivery in tubes:
   - SOIC and TSSOP = 100 per tube.

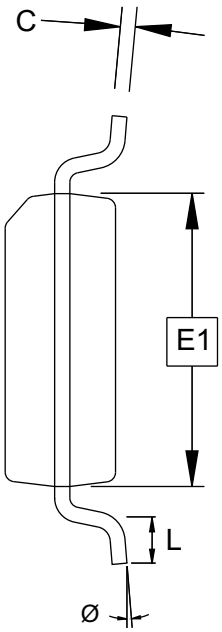
Package Type	
8S1	8-lead, 0.15" wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8X	8-lead, 4.40mm body, Plastic Thin Shrink Small Outline Package (TSSOP)

11. Packaging Information

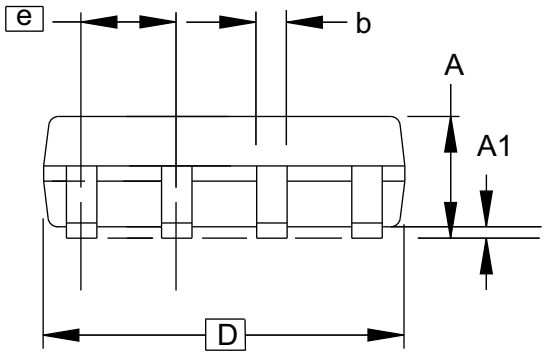
11.1 8S1 — 8-lead JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

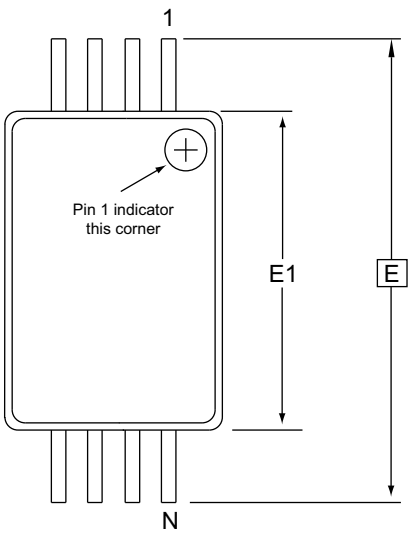
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
Ø	0°	–	8°	

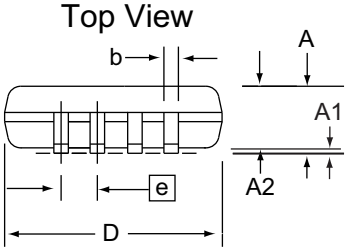
6/22/11

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8S1, 8-lead (0.150” Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	**GPC** SWB	**DRAWING NO.** 8S1	**REV.** G

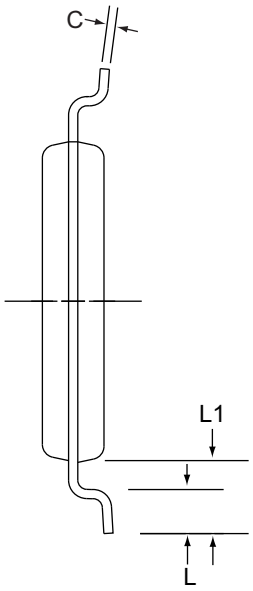
11.2 8X — 8-lead TSSOP



Top View



Side View



End View

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimension D and E1 to be determined at Datum Plane H.

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.20	
A1	0.05	-	0.15	
A2	0.80	1.00	1.05	
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
b	0.19	0.25	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		
C	0.09	-	0.20	

2/27/14

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 8X, 8-lead 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	GPC TNR	DRAWING NO. 8X	REV. E

12. Revision History

Doc. Rev.	Date	Comments
8674C	10/2014	Update the 8S1 and the 8A2 to 8X packages, template, Atmel logos, and disclaimer page. No change in functional specification.
8674B	10/2009	Updated Lit number and date and removed preliminary status.
8674A	4/2009	Initial document release.

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