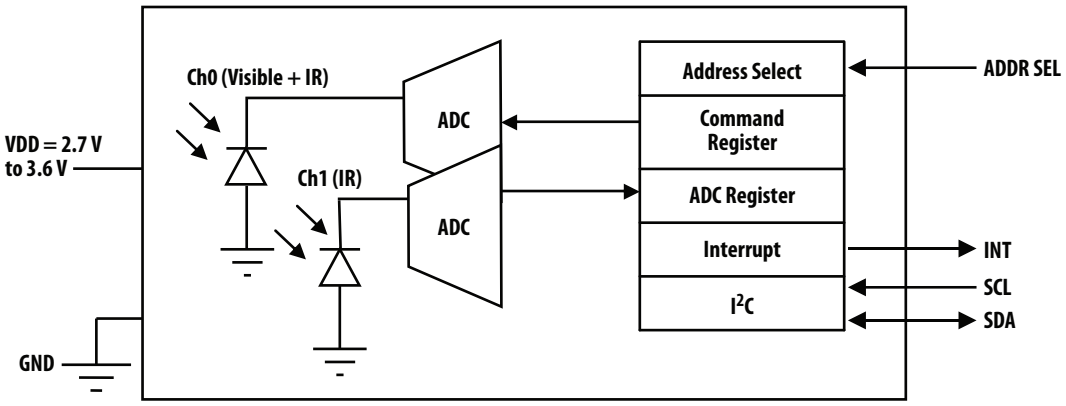
Functional Block Diagram



I/O Pins Configuration Table

Pin	Symbol	Type
1	V_{DD}	Voltage Supply
2	GND	Ground
3	ADDR SEL	Address Select
4	SCL	Serial Clock
5	SDA	Serial Data
6	INT	Interrupt

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	–	3.8	V
Digital output voltage range	VO	-0.5	3.8	V
Digital output current	IO	-1	20	mA
Storage temperature range	T_{stg}	-40	85	°C
ESD tolerance	human body model	–	2000	V

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.0	3.6	V	
Operating Temperature	T_a	-30	–	85	°C	
SCL, SDA input low voltage	V_{IL}	-0.5	–	0.8	V	
SCL, SDA input high voltage	V_{IH}	2.1	–	3.6	V	

Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Supply current	I_{DD}	–	0.24	0.6	mA	Active
		–	3.2	15	µA	Power down
INT, SDA output low voltage	V_{OL}	0	–	0.4	V	3 mA sink current
		0	–	0.6	V	6 mA sink current
Leakage current	I_{LEAK}	-5	–	5	µA	

Operating Characteristics, High Gain (16x), VDD = 3.0 V, Ta = 25°C, (unless otherwise noted) (see Notes 2, 3, 4, 5)

Parameter	Symbol	Channel	Min	Typ	Max	Unit	Conditions
Oscillator frequency	fosc		690	735	780	kHz	
Dark ADC count value		Ch0	0		4	counts	Ee = 0, Tint = 402 ms
		Ch1	0		4		
Full scale ADC count value (Note 6)		Ch0			65535	counts	Tint > 178 ms
		Ch1			65535		
		Ch0			37177		Tint = 101 ms
		Ch1			37177		
		Ch0			5047		Tint = 13.7 ms
		Ch1			5047		
ADC count value		Ch0	750	1000	1250	counts	λp = 640 nm, Tint = 101 ms
		Ch1		200			Ee = 36.3 μW/cm^2
		Ch0	700	1000	1300		λp = 940 nm, Tint = 101 ms
		Ch1		820			Ee = 119 μW/cm^2
ADC count value ratio: Ch1/Ch0			0.15	0.2	0.25		λp = 640 nm, Tint = 101 ms
			0.69	0.82	0.95		λp = 940 nm, Tint = 101 ms
Irradiance responsivity	Re	Ch0		27.5		counts/ (μW/cm^2)	λp = 640 nm, Tint = 101 ms
		Ch1		5.5			
		Ch0		8.4			λp = 940 nm, Tint = 101 ms
		Ch1		6.9			
Illuminance responsivity	Rv	Ch0		36		counts/ lux	Fluorescent light source: Tint = 402 ms
		Ch1		4			
		Ch0		144			Incandescent light source: Tint = 402 ms
		Ch1		72			
ADC count value ratio: Ch1/Ch0				0.11			Fluorescent light source: Tint = 402 ms
				0.5			Incandescent light source: Tint = 402 ms
Illuminance responsivity, low gain mode (Note 7)	Rv	Ch0		2.3		counts/ lux	Fluorescent light source: Tint = 402 ms
		Ch1		0.25			
		Ch0		9			Incandescent light source: Tint = 402 ms
		Ch1		4.5			
(Sensor Lux) /(actual Lux), high gain mode (Note 8)			0.65	1	1.35		Fluorescent light source: Tint = 402 ms
			0.60	1	1.40		Incandescent light source: Tint = 402 ms

NOTES:

2. Optical measurements are made using small–angle incident radiation from light–emitting diode optical sources. Visible 640 nm LEDs and infrared 940 nm LEDs are used for final product testing for compatibility with high–volume production.
3. The 640 nm irradiance E_e is supplied by an AlInGaP light–emitting diode with the following characteristics: peak wavelength λp = 640 nm and spectral halfwidth $\Delta\lambda\frac{1}{2}$ = 17 nm.
4. The 940 nm irradiance E_e is supplied by a GaAs light–emitting diode with the following characteristics: peak wavelength λp = 940 nm and spectral halfwidth $\Delta\lambda\frac{1}{2}$ = 40 nm.
5. Integration time T_{int}, is dependent on internal oscillator frequency (f_{osc}) and on the integration field value in the timing register as described in the *Register Set* section. For nominal f_{osc} = 735 kHz, nominal T_{int} = (number of clock cycles)/f_{osc}.
   Field value 00: T_{int} = (11 x 918)/f_{osc} = 13.7 ms
   Field value 01: T_{int} = (81 x 918)/f_{osc} = 101 ms
   Field value 10: T_{int} = (322 x 918)/f_{osc} = 402 ms
   Scaling between integration times vary proportionally as follows:
   11/322 = 0.034 (field value 00), 81/322 = 0.252 (field value 01), and 322/322 = 1 (field value 10).
6. Full scale ADC count value is limited by the fact that there is a maximum of one count per two oscillator frequency periods and also by a 2–count offset.
   Full scale ADC count value = ((number of clock cycles)/2 - 2)
   Field value 00: Full scale ADC count value = ((11 x 918)/2 - 2) = 5047
   Field value 01: Full scale ADC count value = ((81 x 918)/2 - 2) = 37177
   Field value 10: Full scale ADC count value = 65535, which is limited by 16 bit register. This full scale ADC count value is reached for 131074 clock cycles, which occurs for T_{int} = 178 ms for nominal f_{osc} = 735 kHz.
7. Low gain mode has 16x lower gain than high gain mode: (1/16 = 0.0625).
8. For sensor Lux calculation, please refer to the empirical formula below. It is based on measured Ch0 and Ch1 ADC count values for the light source specified. Actual Lux is obtained with a commercial luxmeter. The range of the (sensor Lux) / (actual Lux) ratio is estimated based on the variation of the 640 nm and 940 nm optical parameters. Devices are not 100% tested with fluorescent or incandescent light sources.

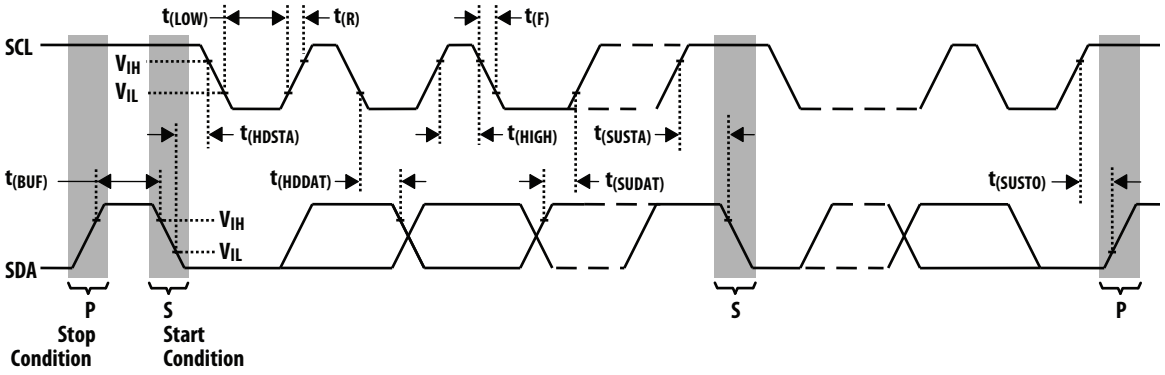
CH1/CH0	Sensor Lux Formula
0 < CH1/CH0 ≤ 0.50	Sensor Lux = (0.0304 x CH0) – (0.062 x CH0 x ((CH1/CH0)$^{1.4}$))
0.50 < CH1/CH0 ≤ 0.61	Sensor Lux = (0.0224 x CH0) – (0.031 x CH1)
0.61 < CH1/CH0 ≤ 0.80	Sensor Lux = (0.0128 x CH0) – (0.0153 x CH1)
0.80 < CH1/CH0 ≤ 1.30	Sensor Lux = (0.00146 x CH0) – (0.00112 x CH1)
CH1/CH0>1.30	Sensor Lux = 0

AC Electrical Characteristics (VDD = 3 V, Ta = 25°C)

PARAMETER†		MIN	TYP	MAX	UNIT
$t_{(CONV)}$	Conversion time	12	100	400	ms
$f_{(SCL)}$	Clock frequency	–	–	400	kHz
$t_{(BUF)}$	Bus free time between start and stop condition	1.3	–	–	µs
$t_{(HDSTA)}$	Hold time after (repeated) start condition. After this period, the first clock is generated.	0.6	–	–	µs
$t_{(SUSTA)}$	Repeated start condition setup time	0.6	–	–	µs
$t_{(SUSTO)}$	Stop condition setup time	0.6	–	–	µs
$t_{(HDDAT)}$	Data hold time	0	–	0.9	µs
$t_{(SUDAT)}$	Data setup time	100	–	–	ns
$t_{(LOW)}$	SCL clock low period	1.3	–	–	µs
$t_{(HIGH)}$	SCL clock high period	0.6	–	–	µs
t_F	Clock/data fall time	–	–	300	ns
t_R	Clock/data rise time	–	–	300	ns
C_j	Input pin capacitance	–	–	10	pF

† Specified by design and characterization; not production tested.

Parameter Measurement Information



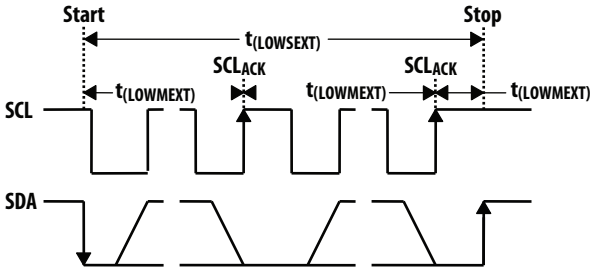


Figure 1. Timing Diagrams

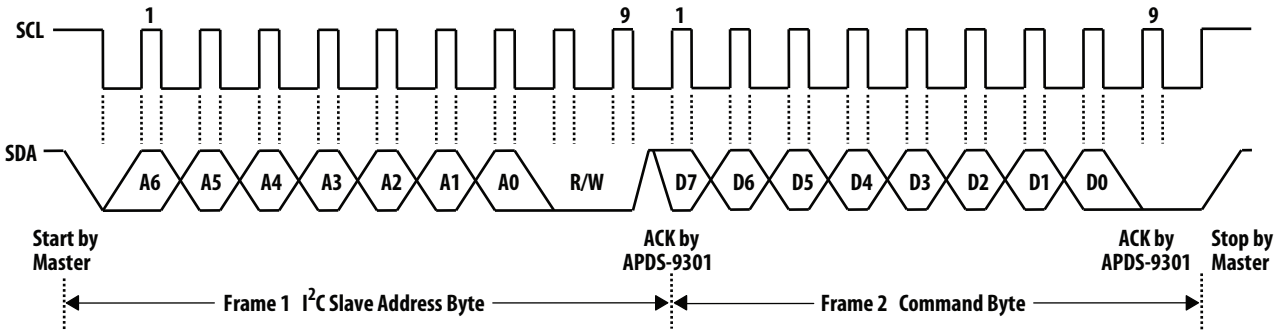


Figure 2. Example Timing Diagram for I^2C Send Byte Format

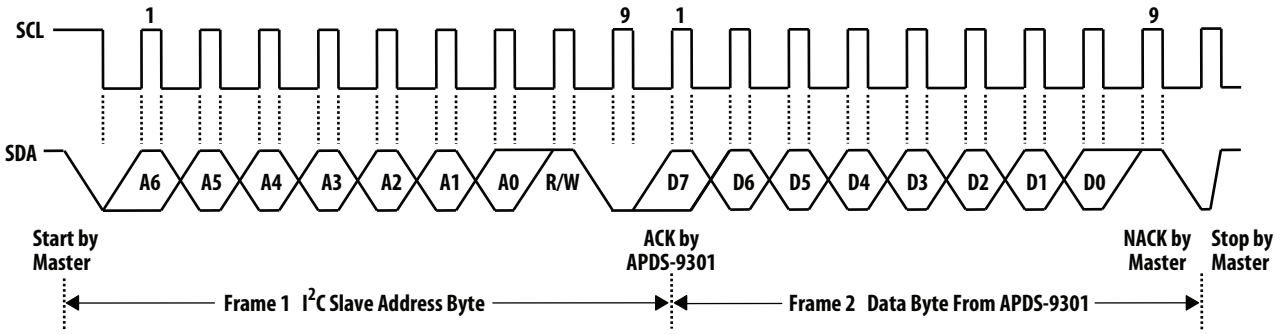


Figure 3. Example Timing Diagram for I^2C Receive Byte Format

Typical Characteristics

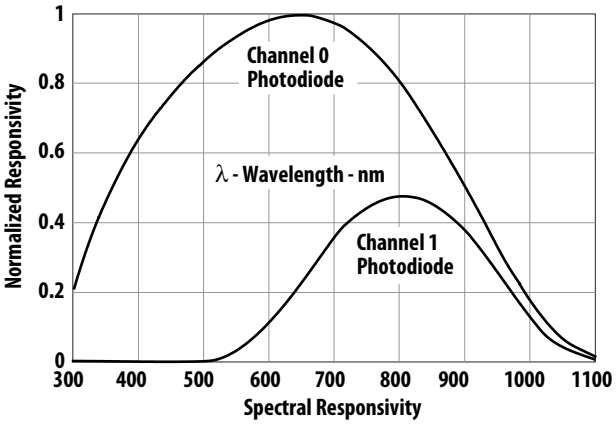


Figure 4. Normalized Responsitivity vs. Spectral Responsivity

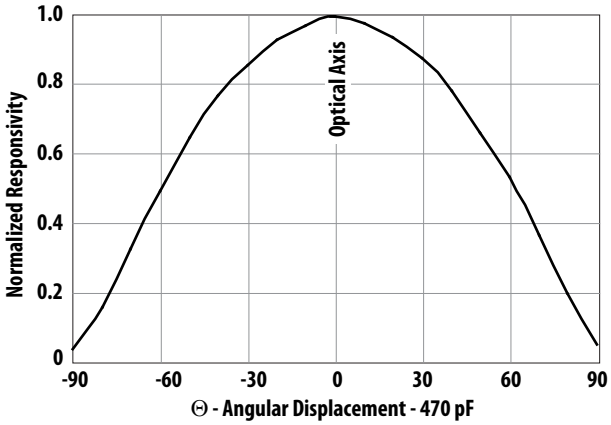


Figure 5. Normalized Responsivity vs. Angular Displacement * CL Package

PRINCIPLES OF OPERATION

Analog–to–Digital Converter

The APDS-9301 contains two integrating analog-to-digital converters (ADC) that integrate the currents from the channel 0 and channel 1 photodiodes. Integration of both channels occurs simultaneously, and upon completion of the conversion cycle the conversion result is transferred to the channel 0 and channel 1 data registers, respectively. The transfers are double buffered to ensure that invalid data is not read during the transfer. After the transfer, the device automatically begins the next integration cycle.

Digital Interface

Interface and control of the APDS-9301 is accomplished through a two–wire serial interface to a set of registers that provide access to device control functions and output data. The serial interface is compatible to I²C bus Fast–Mode. The APDS-9301 offers three slave addresses that are selectable via an external pin (ADDR SEL). The slave address options are shown in Table 1.

Table 1. Slave Address Selection

ADDR SEL TERMINAL LEVEL	SLAVE ADDRESS
GND	0101001
Float	0111001
V_{DD}	1001001

NOTE: The Slave Addresses are 7 bits and please note the I²C protocols. A read/write bit should be appended to the slave address by the master device to properly communicate with the APDS-9301 device.

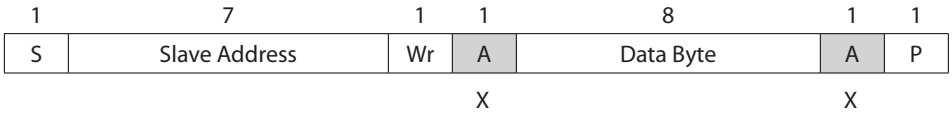
I²C Protocols

Each *Send* and *Write* protocol is, essentially, a series of bytes. A byte sent to the APDS-9301 with the most significant bit (MSB) equal to 1 will be interpreted as a COMMAND byte. The lower four bits of the COMMAND byte form the register select address (see Table 2), which is used to select the destination for the subsequent byte(s) received. The APDS-9301 responds to any Receive Byte requests with the contents of the register specified by the stored register select address.

The APDS-9301 implements the following protocols of the Philips Semiconductor I²C specification:

- I²C Write Protocol
- I²C Read Protocol

For a complete description of I²C protocol, please review the I²C Specification at http://www.semiconductors.philips.com



A Acknowledge (this bit position may be 0 for an ACK or 1 for a NACK)

P Stop Condition

Rd Read (bit value of 1)

S Start Condition

Sr Repeated Start Condition

Wr Write (bit value of 0)

X Shown under a field indicates that that field is required to have a value of X

... Continuation of protocol

Master-to-Slave

Slave-to-Master

Figure 6. I²C Packet Protocol Element Key

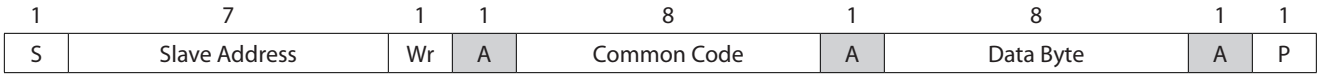


Figure 7. I²C Write Protocols

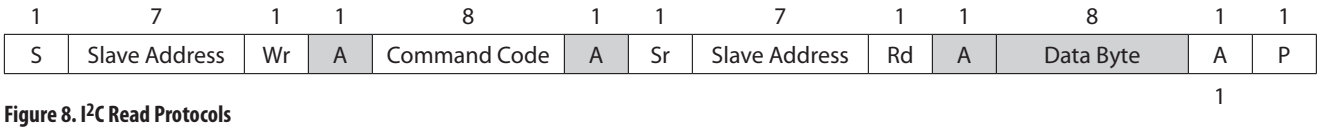


Figure 8. I²C Read Protocols

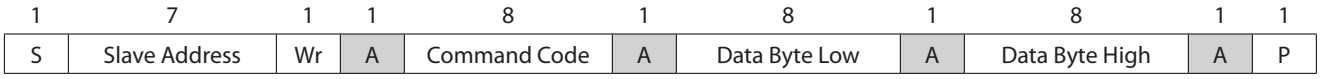


Figure 9. I²C Write Word Protocols

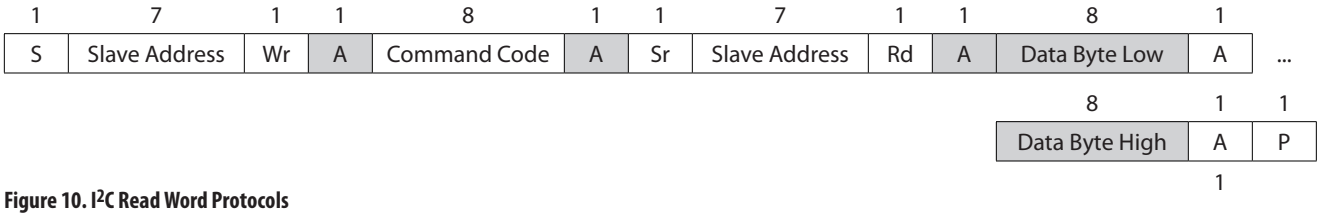


Figure 10. I²C Read Word Protocols

Register Set

The APDS-9301 is controlled and monitored by sixteen registers (three are reserved) and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The register set is summarized in Table 2.

Table 2. Register Address

ADDRESS	RESISTER NAME	REGISTER FUNCTION
--	COMMAND	Specifies register address
0h	CONTROL	Control of basic functions
1h	TIMING	Integration time/gain control
2h	THRESHLOWLOW	Low byte of low interrupt threshold
3h	THRESHLOWHIGH	High byte of low interrupt threshold
4h	THRESHHIGHLOW	Low byte of high interrupt threshold
5h	THRESHHIGHHIGH	High byte of high interrupt threshold
6h	INTERRUPT	Interrupt control
7h	--	Reserved
8h	CRC	Factory test — not a user register
9h	--	Reserved
Ah	ID	Part number/ Rev ID
Bh	--	Reserved
Ch	DATA0LOW	Low byte of ADC channel 0
Dh	DATA0HIGH	High byte of ADC channel 0
Eh	DATA1LOW	Low byte of ADC channel 1
Fh	DATA1HIGH	High byte of ADC channel 1

The mechanics of accessing a specific register depends on the specific I^2C protocol used. Refer to the section on I^2C protocols. In general, the COMMAND register is written first to specify the specific control/status register for following read/write operations.

Command Register

The command register specifies the address of the target register for subsequent read and write operations. The Send Byte protocol is used to configure the COMMAND register. The command register contains eight bits as described in Table 3. The command register defaults to 00h at power on.

Table 3. Command Register

	7	6	5	4	3	2	1	0	
	CMD	CLEAR	WORD	Resv	ADDRESS				COMMAND
Reset Value:	0	0	0	0	0	0	0	0	

FIELD	BIT	DESCRIPTION
CMD	7	Select command register. Must write as 1.
CLEAR	6	Interrupt clear. Clears any pending interrupt. This bit is a write-one-to-clear bit. It is self clearing.
WORD	5	I^2C Write/Read Word Protocol. 1 indicates that this I^2C transaction is using either the I^2C Write Word or Read Word protocol.
Resv	4	Reserved. Write as 0.
ADDRESS	3:0	Register Address. This field selects the specific control or status register for following write and read commands according to Table 2.

Control Register (0h)

The CONTROL register contains two bits and is primarily used to power the APDS-9301 device up and down as shown in Table 4.

Table 4. Control Re gister

	7	6	5	4	3	2	1	0	
Oh	Resv	Resv	Resv	Resv	Resv	Resv	POWER		CONTROL
Reset Value:	0	0	0	0	0	0	0	0	

FIELD	BIT	DESCRIPTION
Resv	7:2	Reserved. Write as 0.
POWER	1:0	Power up/power down. By writing a 03h to this register, the device is powered up. By writing a 00h to this register, the device is powered down. NOTE: If a value of 03h is written, the value returned during a read cycle will be 03h. This feature can be used to verify that the device is communicating properly.

Timing Register (1h)

The TIMING register controls both the integration time and the gain of the ADC channels. A common set of control bits is provided that controls both ADC channels. The TIMING register defaults to 02h at power on.

Table 5. Timing Register

	7	6	5	4	3	2	1	0	
1hr	Resv	Resv	Resv	GAIN	MANUAL	Resv	INTEG		TIMING
Reset Value:	0	0	0	0	0	0	1	0	

FIELD	BIT	DESCRIPTION
Resv	7-5	Reserved. Write as 0.
GAIN	4	Switches gain between low gain and high gain modes. Writing a 0 selects low gain (1x); writing a 1 selects high gain (16x).
MANUAL	3	Manual timing control. Writing a 1 begins an integration cycle. Writing a 0 stops an integration cycle. NOTE: This field only has meaning when INTEG = 11. It is ignored at all other times.
Resv	2	Reserved. Write as 0.
INTEG	1:0	Integrate time. This field selects the integration time for each conversion.

Integration time is dependent on the INTEG FIELD VALUE and the internal clock frequency. Nominal integration times and respective scaling between integration times scale proportionally as shown in Table 6. See Note 5 and Note 6 on page 5 for detailed information regarding how the scale values were obtained.

Table 6. Integration Time

INTEG FIELD VALUE	SCALE	NOMINAL INTEGRATION TIME
00	0.034	13.7 ms
01	0.252	101 ms
10	1	402 ms
11	–	N/A

The manual timing control feature is used to manually start and stop the integration time period. If a particular integration time period is required that is not listed in Table 6, then this feature can be used. For example, the manual timing control can be used to synchronize the APDS-9301 device with an external light source (e.g. LED). A start command to begin integration can be initiated by writing a 1 to this bit field. Correspondingly, the integration can be stopped by simply writing a 0 to the same bit field.

Interrupt Threshold Register (2h - 5h)

The interrupt threshold registers store the values to be used as the high and low trigger points for the comparison function for interrupt generation. If the value generated by channel 0 crosses below or is equal to the low threshold specified, an interrupt is asserted on the interrupt pin. If the value generated by channel 0 crosses above the high threshold specified, an interrupt is asserted on the interrupt pin. Registers THRESHLOWLOW and THRESHLOWHIGH provide the low byte and high byte, respectively, of the lower interrupt threshold. Registers THRESHHIGHLOW and THRESHHIGHHIGH provide the low and high bytes, respectively, of the upper interrupt threshold. The high and low bytes from each set of registers are combined to form a 16–bit threshold value. The interrupt threshold registers default to 00h on power up.

Table 7. Interrupt Threshold Register

REGISTER	ADDRESS	BITS	DESCRIPTION
THRESHLOWLOW	2h	7:0	ADC channel 0 lower byte of the low threshold
THRESHLOWHIGH	3h	7:0	ADC channel 0 upper byte of the low threshold
THRESHHIGHLOW	4h	7:0	ADC channel 0 lower byte of the high threshold
THRESHHIGHHIGH	5h	7:0	ADC channel 0 upper byte of the high threshold

NOTE: Since two 8-bit values are combined for a single 16-bit value for each of the high and low interrupt thresholds, the Send Byte protocol should not be used to write to these registers. Any values transferred by the Send Byte protocol with the MSB set would be interpreted as the COMMAND field and stored as an address for subsequent read/write operations and not as the interrupt threshold information as desired. The Write Word protocol should be used to write byte-paired registers. For example, the THRESHLOWLOW and THRESHLOWHIGH registers (as well as the THRESHHIGHLOW and THRESHHIGHHIGH registers) can be written together to set the 16–bit ADC value in a single transaction.

Interrupt Control Register (6h)

The INTERRUPT register controls the extensive interrupt capabilities of the APDS-9301. The APDS-9301 permits traditional level-style interrupts. The interrupt persist bit field (PERSIST) provides control over when interrupts occur. A value of 0 causes an interrupt to occur after every integration cycle regardless of the threshold settings. A value of 1 results in an interrupt after one integration time period outside the threshold window. A value of *N* (where *N* is 2 through 15) results in an interrupt only if the value remains outside the threshold window for *N* consecutive integration cycles. For example, if *N* is equal to 10 and the integration time is 402 ms, then the total time is approximately 4 seconds.

When a level Interrupt is selected, an interrupt is generated whenever the last conversion results in a value outside of the programmed threshold window. The interrupt is active-low and remains asserted until cleared by writing the COMMAND register with the CLEAR bit set.

NOTE: Interrupts are based on the value of Channel 0 only.

Table 8. Interrupt Control Register

	7	6	5	4	3	2	1	0	
6h	Resv	Resv	INTR		PERSIST				INTERRUPT
Reset Value:	0	0	0	0	0	0	0	0	

FIELD	BITS	DESCRIPTION
Resv	7:6	Reserved. Write as 0.
INTR	5:4	INTR Control Select. This field determines mode of interrupt logic according to Table 9, below.
PERSIST	3:0	Interrupt persistence. Controls rate of interrupts to the host processor as shown in Table 10, below.

Table 9. Interrupt Control Select

INTR FIELD VALUE	READ VALUE
00	Level Interrupt output disabled
01	Level Interrupt output enabled

Table 10. Interrupt Persistence Select

PERSIST FIELD VALUE	INTERRUPT PERSIST FUNCTION
0000	Every ADC cycle generates interrupt
0001	Any value outside of threshold range
0010	2 integration time periods out of range
0011	3 integration time periods out of range
0100	4 integration time periods out of range
0101	5 integration time periods out of range
0110	6 integration time periods out of range
0111	7 integration time periods out of range
1000	8 integration time periods out of range
1001	9 integration time periods out of range
1010	10 integration time periods out of range
1011	11 integration time periods out of range
1100	12 integration time periods out of range
1101	13 integration time periods out of range
1110	14 integration time periods out of range
1111	15 integration time periods out of range

ID Register (Ah)

The ID register provides the value for both the part number and silicon revision number for that part number. It is a read-only register, whose value never changes.

Table 11. ID Register

	7	6	5	4	3	2	1	0	
Ah	0	1	0	1	REVNO				ID
Reset Value:	–	–	–	–	–	–	–	–	

FIELD	BITS	DESCRIPTION
PARTNO	7:4	Part Number Identification
REVNO	3:0	Revision number identification

ADC Channel Data Registers (Ch - Fh)

The ADC channel data are expressed as 16-bit values spread across two registers. The ADC channel 0 data registers, DATA0LOW and DATA0HIGH provide the lower and upper bytes, respectively, of the ADC value of channel 0. Registers DATA1LOW and DATA1HIGH provide the lower and upper bytes, respectively, of the ADC value of channel 1. All channel data registers are read-only and default to 00h on power up.

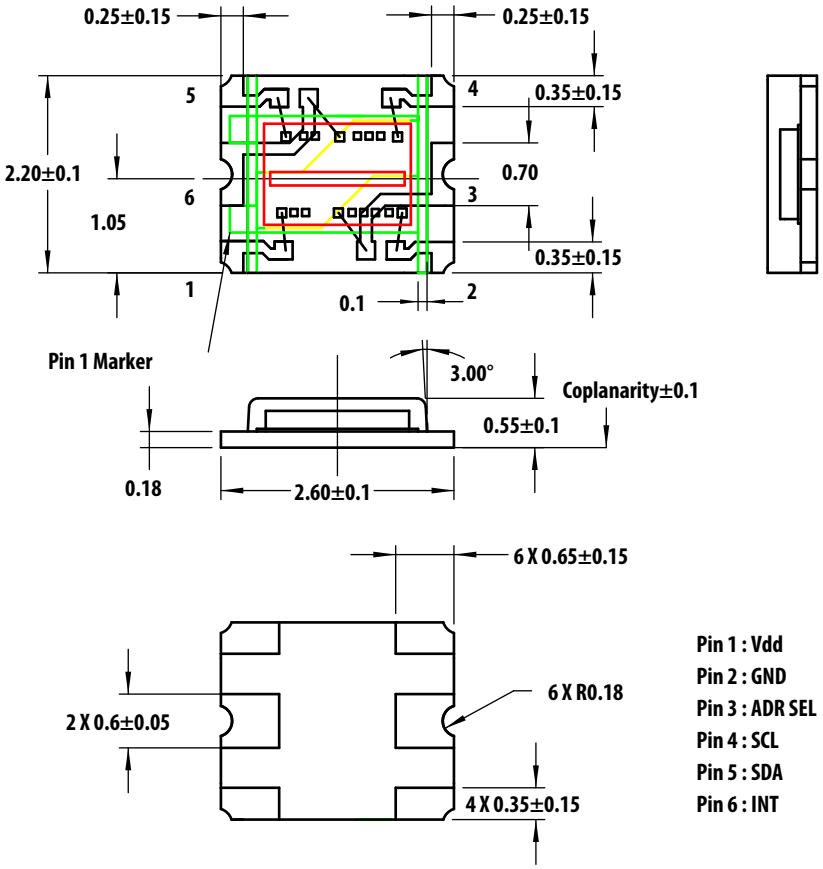
Table 12. ADC Channel Data Registers

REGISTER	ADDRESS	BITS	DESCRIPTION
DATA0LOW	Ch	7:0	ADC channel 0 lower byte
DATA0HIGH	Dh	7:0	ADC channel 0 upper byte
DATA1LOW	Eh	7:0	ADC channel 1 lower byte
DATA1HIGH	Fh	7:0	ADC channel 1 upper byte

The upper byte data registers can only be read following a read to the corresponding lower byte register. When the lower byte register is read, the upper eight bits are strobed into a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if additional ADC integration cycles end between the reading of the lower and upper registers.

NOTE: The Read Word protocol can be used to read byte-paired registers. For example, the DATA0LOW and DATA0HIGH registers (as well as the DATA1LOW and DATA1HIGH registers) may be read together to obtain the 16-bit ADC value in a single transaction

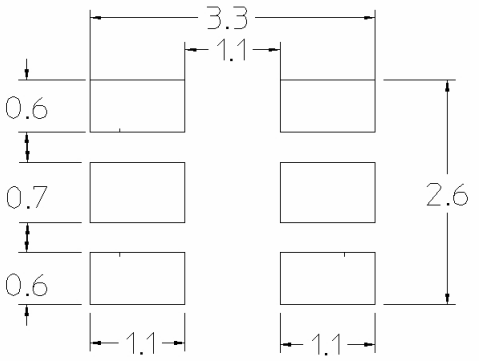
APDS-9301 Package Outline



Notes:
All dimensions are in millimeters. Dimension tolerance is ±0.2 mm unless otherwise stated

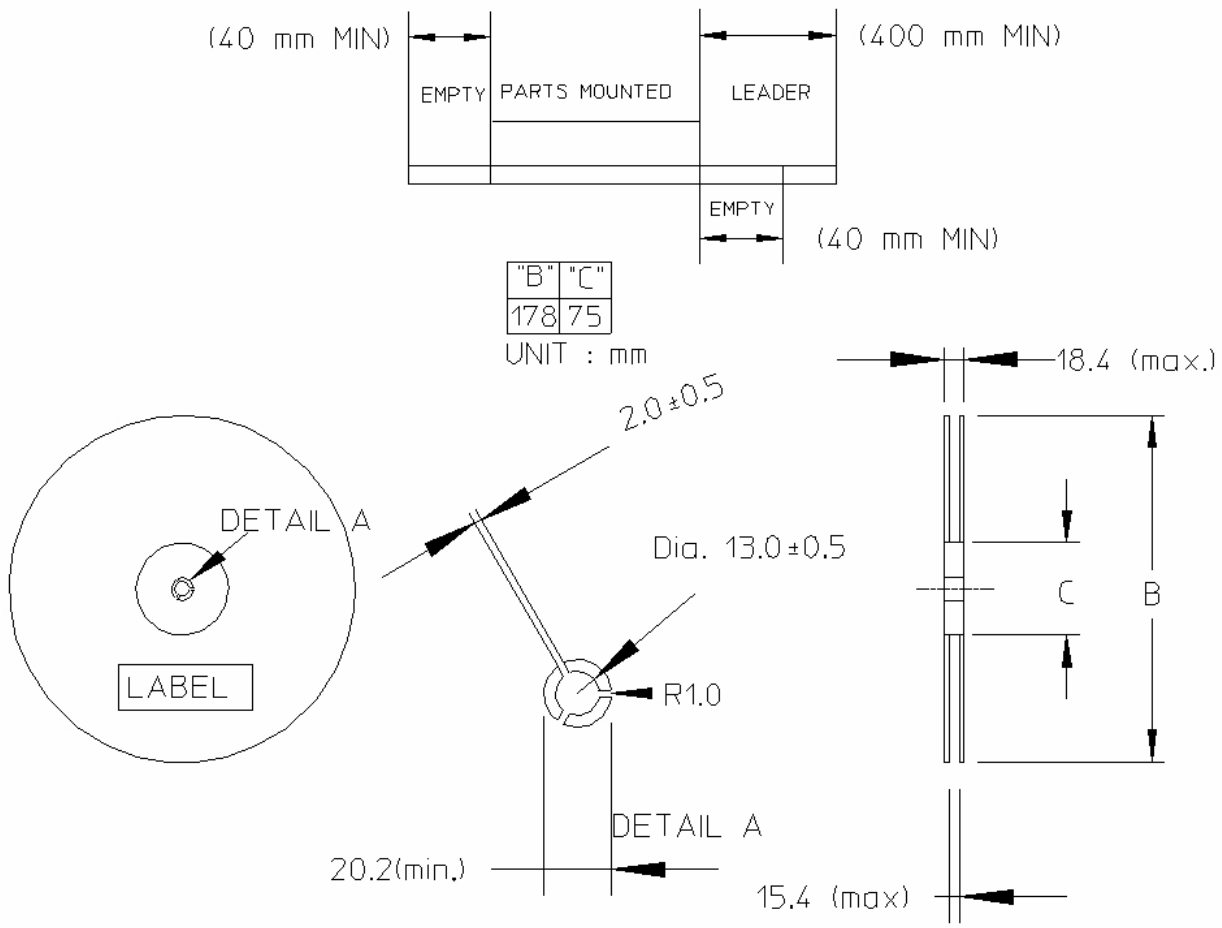
PCB Pad Layout

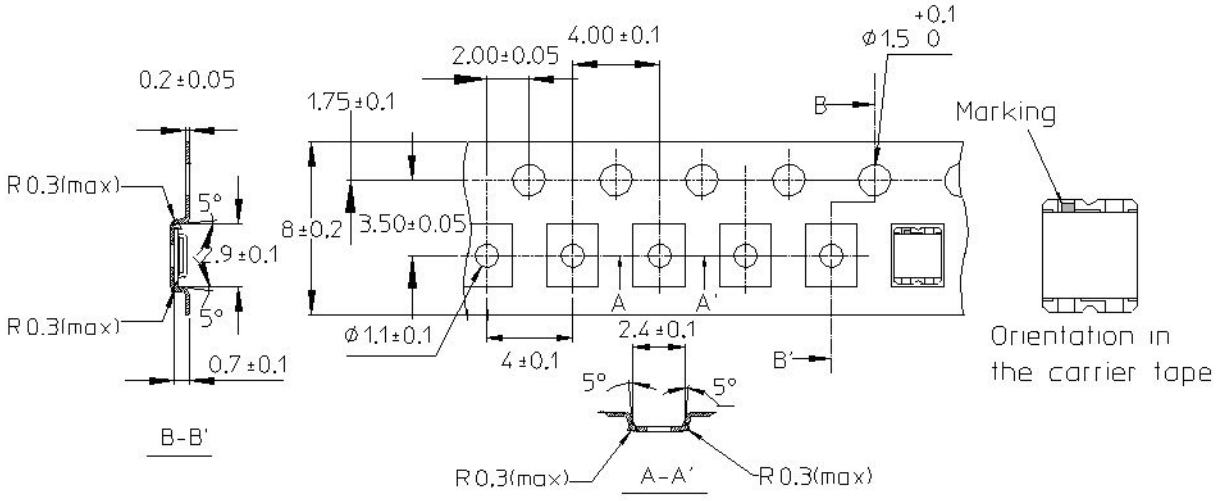
The suggested PCB layout is given below:



Notes:
All linear dimensions are in millimeters.

APDS-9301 Tape and Reel Dimensions



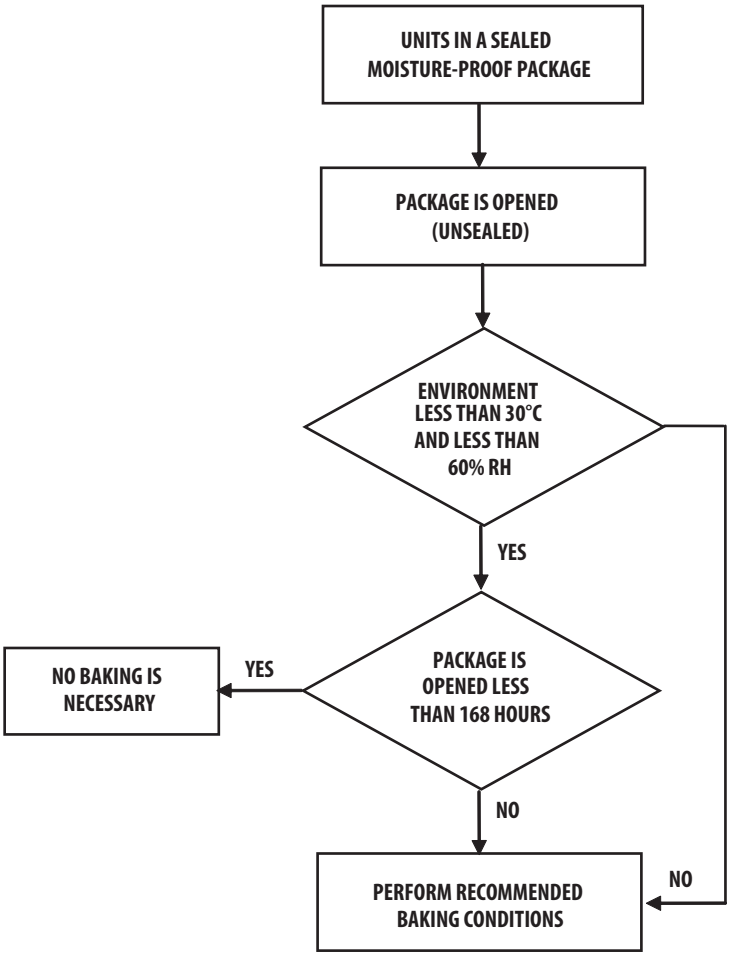


Material of Carrier Tape : Conductive Polystrene
Method of Cover : Heat Sensitive Adhesive

Moisture Proof Packaging Chart

All APDS-9301 options are shipped in moisture proof package. Once opened, moisture absorption begins.

This part is compliant to JEDEC Level 3.



BAKING CONDITIONS CHART

Recommended Storage Conditions

Storage Temperature	10°C to 30°C
Relative Humidity	Below 60% RH

Time from Unsealing to Soldering

After removal from the bag, the parts should be soldered within seven days if stored at the recommended storage conditions. When MBB (Moisture Barrier Bag) is opened and the parts are exposed to the recommended storage conditions more than seven days the parts must be baked before reflow to prevent damage to the parts.

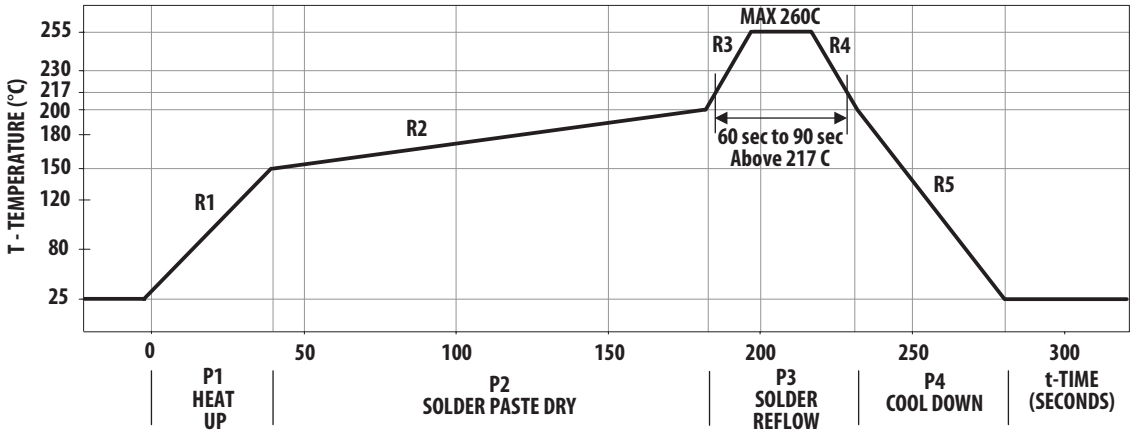
Baking Conditions

If the parts are not stored per the recommended storage conditions they must be baked before reflow to prevent damage to the parts.

Package	Temp.	Time
In Reels	60°C	48 hours
In Bulk	100°C	4 hours

Note: Baking should only be done once.

Recommended Reflow Profile



Process Zone	Symbol	ΔT	Maximum ΔT/Δtime or Duration
Heat Up	P1, R1	25°C to 150°C	3°C/s
Solder Paste Dry	P2, R2	150°C to 200°C	100s to 180s
Solder Reflow	P3, R3 P3, R4	200°C to 260°C 260°C to 200°C	3°C/s -6°C/s
Cool Down	P4, R5	200°C to 25°C	-6°C/s
Time maintained above liquidus point, 217°C		> 217°C	60s to 120s
Peak Temperature		260°C	–
Time within 5°C of actual Peak Temperature		–	20s to 40s
Time 25°C to Peak Temperature		25°C to 260°C	8mins

The reflow profile is a straight-line representation of a nominal temperature profile for a convective reflow solder process. The temperature profile is divided into four process zones, each with different ΔT/Δtime temperature change rates or duration. The ΔT/Δtime rates or duration are detailed in the above table. The temperatures are measured at the component to printed circuit board connections.

In **process zone P1**, the PC board and component pins are heated to a temperature of 150°C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 3°C per second to allow for even heating of both the PC board and component pins.

Process zone P2 should be of sufficient time duration (100 to 180 seconds) to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder.

Process zone P3 is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 260°C (500°F) for optimum results. The dwell time above the liquidus point of solder should be between 60 and 90 seconds. This is to assure proper coalescing of the solder paste into liquid solder and the formation of good solder connections. Beyond the recommended dwell time the intermetallic growth within the solder connections becomes excessive, resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder to allow the solder within the connections to freeze solid.

Process zone P4 is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25°C (77°F) should not exceed 6°C per second maximum. This limitation is necessary to allow the PC board and component pins to change dimensions evenly, putting minimal stresses on the component.

It is recommended to perform reflow soldering no more than twice.

Appendix A: Window Design Guide

A1: Optical Window Dimensions

To ensure that the performance of the APDS-9301 will not be affected by improper window design, there are some criteria requested on the dimensions and design of the window. There is a constraint on the minimum size of the window, which is placed in front of the photo light sensor, so that it will not affect the angular response of the APDS-9301. This minimum dimension that is recommended will ensure at least a ±35° light reception cone.

If a smaller window is required, a light pipe or light guide can be used. A light pipe or light guide is a cylindrical piece of transparent plastic, which makes use of total internal reflection to focus the light.

The thickness of the window should be kept as minimum as possible because there is a loss of power in every optical window of about 8% due to reflection (4% on each side) and an additional loss of energy in the plastic material.

Figure A1 illustrates the two types of window that we have recommended which could either be a flat window or a flat window with light pipe.

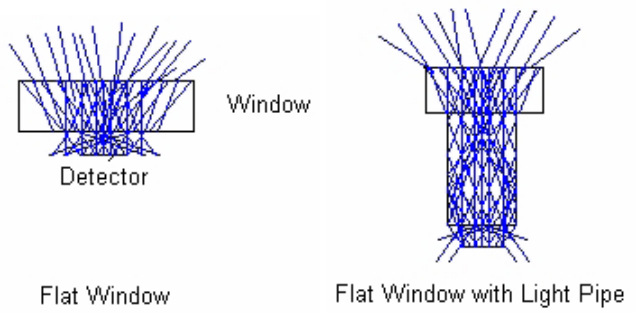


Figure A1. Recommended Window Design

Table A1 and Figure A2 show the recommended dimensions of the window. These dimension values are based on a window thickness of 1.0mm with a refractive index 1.585.

The window should be placed directly on top of the light sensitive area of APDS-9301 (see Figure A3) to achieve better performance. If a flat window with a light pipe is used, dimension D2 should be 1.55mm to optimize the performance of APDS-9301.

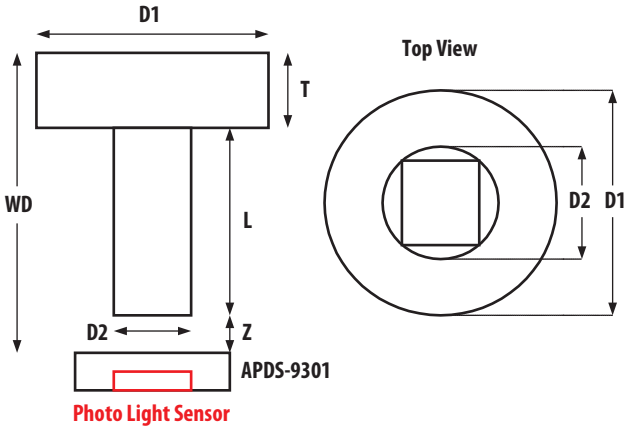


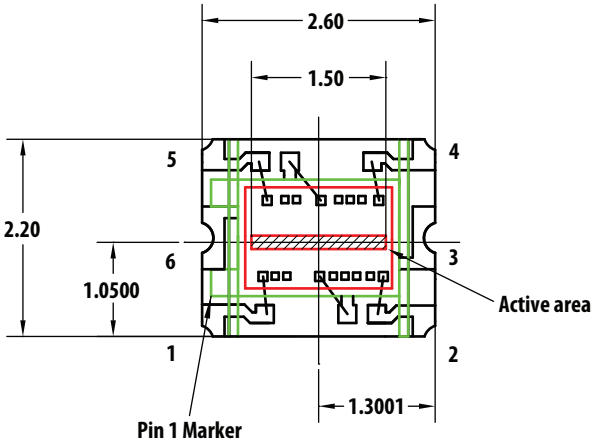
Figure A2. Recommended Window Dimensions

WD: Working Distance between window front panel & APDS-9301
D1: Window Diameter
T: Thickness
L: Length of Light Pipe
D2: Light Pipe Diameter
Z: Distance between window rear panel and APDS-9301

All dimensions are in mm

Table A1. Recommended dimension for optical window

WD (T+L+Z)	Flat Window (L = 0.0 mm, T = 1.0 mm)		Flat window with Light Pipe (D2 = 1.55mm, Z = 0.5mm, T = 1.0mm)	
	Z	D1	D1	L
1.5	0.5	2.25	–	–
2.0	1.0	3.25	–	–
2.5	1.5	4.25	–	–
3.0	2.0	5.00	2.5	1.5
6.0	5.0	8.50	2.5	4.5



Notes:
1. All dimensions are in millimeters
2. All package dimension tolerance in ± 0.2mm unless otherwise specified

Figure A3. APDS-9301 Light Sensitive Area

A2: Optical Window Material

The material of the window is recommended to be polycarbonate. The surface finish of the plastic should be smooth, without any texture.

The recommended plastic material for use as a window is available from Bayer AG and Bayer Antwerp N. V. (Europe), Bayer Corp. (USA) and Bayer Polymers Co., Ltd. (Thailand), as shown in Table A2.

Table A2. Recommended Plastic Materials

Material number	Visible light transmission	Refractive index
Makrolon LQ2647	87%	1.587
Makrolon LQ3147	87%	1.587
Makrolon LQ3187	85%	1.587

Appendix B: Application Circuit

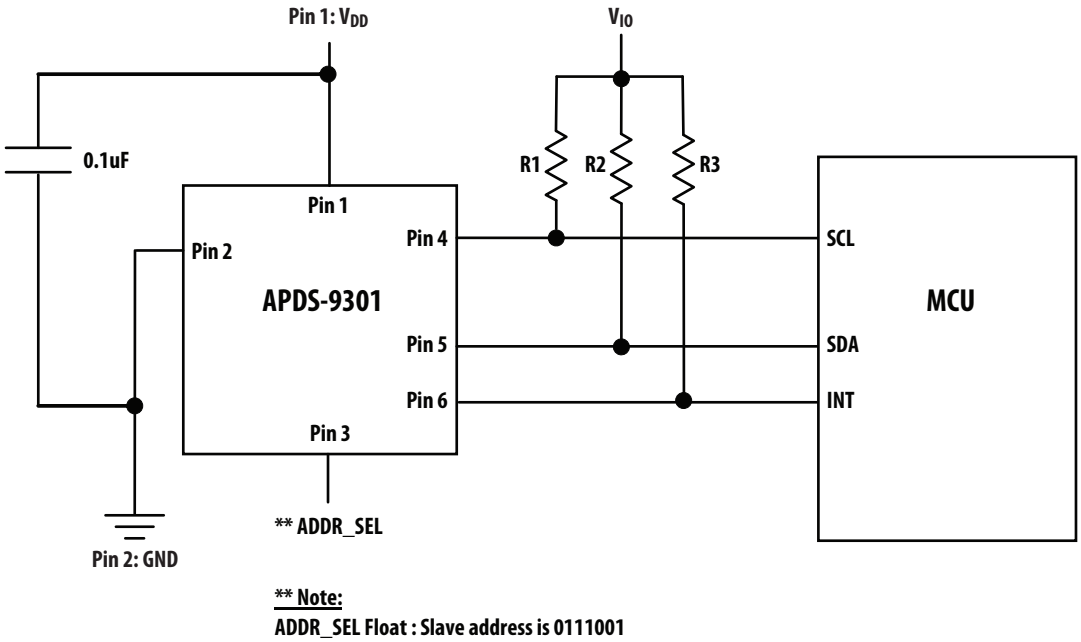


Figure B1. Application circuit for APDS-9301

The power supply lines must be decoupled with a 0.1 uF capacitor placed as close to the device package as possible, as shown in Figure B1. The bypass capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents caused by internal logic switching.

Pull-up resistors, R1 and R2, maintain the SDA and SCL lines at a high level when the bus is free and ensure the signals are pulled up from a low to a high level within the required rise time. For a complete description of I^2C maximum and minimum R1 and R2 values, please review the I^2C Specification at http://www.semiconductors.philips.com.

A pull-up resistor, R3, is also required for the interrupt (INT), which functions as a wired-AND signal in a similar fashion to the SCL and SDA lines. A typical impedance value between 10 kΩ and 100 kΩ can be used.

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