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8/15—Rev. A to Rev. B

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Added Figure 10, Figure 12, Figure 13, and Figure 14; Renumbered Sequentially ... 7
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9/14—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = 1.2 V, V_{SYS} = V_{BAT} = 3 V, T_J = −40°C to 125°C for minimum/maximum specifications and T_A = 25°C for typical specifications, unless otherwise noted. External components and inductor (L) = 22 µH, C_{IN} = 4.7 µF, C_{SYS} = 4.7 µF.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
COLD-START CIRCUIT						
Minimum Input Voltage for Cold-Start	V_{IN_COLD}	V_{SYS} = 0 V, 0°C < T_A < 85°C		380	440	mV
Minimum Input Power for Cold-Start	P_{IN_COLD}			16		µW
End of Cold-Start Operation Threshold	V_{SYS_TH}		1.8	1.93	2.03	V
End of Cold-Start Operation Hysteresis	V_{SYS_HYS}			125		mV
BOOST REGULATOR						
Input Voltage Operation Range	V_{IN}	Cold-start completed	0.1		3.3	V
Input Power Operation Range	P_{IN}	Cold-start completed, V_{IN} = 0.5 V	0.01		200	mW
Input Peak Current	I_{IN_PEAK}	Factory trim, 1 bit (Option 0)		100	135	mA
		Factory trim, 1 bit (Option 1)		195	250	mA
Low-Side Switch on Resistance	$R_{LS\_DS\_ON}$			1.25	1.71	Ω
High-Side Switch on Resistance	$R_{HS\_DS\_ON}$			1.38	1.88	Ω
SYS Switch on Resistance	$R_{SYS\_DS\_ON}$			0.48	0.70	Ω
DIS_SW High Voltage	DIS_SW_{HIGH}		1			V
DIS_SW Low Voltage	DIS_SW_{LOW}				0.5	V
DIS_SW Delay	t_{DIS_DELAY}			1		µs
VIN CONTROL AND REGULATION						
VIN Open Circuit Voltage Sampling Cycle	T_{VOC_CYCLE}			19		s
VIN Open Circuit Voltage Sampling Time	T_{VOC_SAMPL}			296		ms
MINOP Bias Current	I_{MINOP}		1.45	2	2.55	µA
MINOP Operation Voltage Range	V_{MINOP}				1	V
ENERGY STORAGE MANAGEMENT						
Operating Quiescent Current of SYS Pin	I_{Q_SYS}	V_{IN} > V_{CBP} ≥ V_{MINOP}, V_{SYS} > V_{BAT_SD}		320	580	nA
Sleeping Quiescent Current of SYS Pin	$I_{IQ\_SLEEP\_SYS}$	V_{CBP} < V_{MINOP}, V_{SYS} > V_{BAT_SD}		260	480	nA
Internal Reference Voltage	V_{REF}		1.14	1.21	1.28	V
Battery Stop Discharging Threshold	V_{BAT_SD}		2		V_{BAT_TERM}	V
Battery Stop Discharging Hysteresis Resistor	$R_{BAT\_SD\_HYS}$		65	103.5	150	kΩ
Battery Terminal Charging Threshold	V_{BAT_TERM}		2.2		5.2	V
Battery Terminal Charging Hysteresis	$V_{BAT\_TERM\_HYS}$			3	3.7	%
PGOOD Falling Threshold at SYS Pin	V_{SYS_PG}		V_{BAT_SD}		V_{BAT_TERM}	V
PGOOD Hysteresis Resistor at SYS Pin	$R_{SYS\_PG\_HYS}$		65	103.5	150	kΩ
PGOOD Pull-Up Resistor				11.8	17	kΩ
PGOOD Pull-Down Resistor				11.8	17	kΩ
Battery Switch on Resistance	$R_{BAT\_SW\_ON}$			0.55	0.73	Ω
Battery Current Capability	I_{BAT}				800	mA
Leakage Current at BAT Pin	I_{BAT_LEAK}	V_{BAT} = 2 V, V_{BAT_SD} = 2.2 V, V_{SYS} = 2 V		15	50	nA
		V_{BAT} = 3.3 V, V_{BAT_SD} = 2.2 V, V_{SYS} = 0 V		0.5	20	nA
BACK_UP POWER PATH						
BACK_UP Switches on Resistance	$R_{BKP\_SW\_ON}$	V_{SYS} = V_{BACK_UP} = 3 V		1.18	1.60	Ω
BACK_UP and BAT Comparator Offset	V_{BKP_OFFSET}	V_{SYS} ≥ V_{SYS_TH}	135	185	250	mV
BACK_UP and BAT Comparator Hysteresis	V_{BAT_HYS}	V_{SYS} ≥ V_{SYS_TH}	55	75	100	mV
BACK_UP Current Capability	I_{BKP}	V_{SYS} ≥ V_{SYS_TH}		400	520	mA
		Plug in the backup battery first		250		µA
Leakage Current at BACK_UP Pin	I_{BKP_LEAK}	V_{BACK_UP} = V_{SYS} = V_{BAT} = 3 V		6	18	nA
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	T_{SHDN}	V_{SYS} ≥ V_{SYS_TH}		125		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VIN, MPPT, CBP, MINOP	−0.3 V to +3.6 V
DIS_SW, TERM, SETPG, SETSD, PGOOD, REF to AGND	−0.3 V to +6.0 V
SW, SYS, BAT, BACK_UP to PGND	−2.0 V to +6.0 V
PGND to GND	−0.3 V to +0.3 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3.

Package Type	θ_{JA}	θ_{JC}	Unit
16-Lead LFCSP	53.1	4.55	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

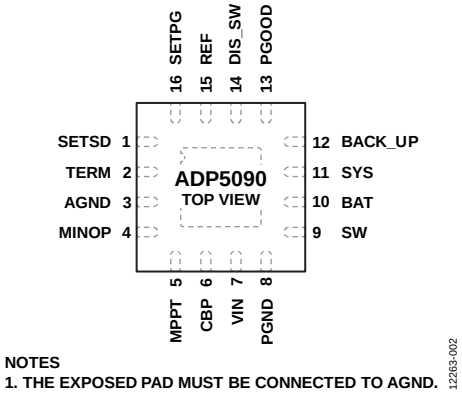

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SETSD	Shutdown Setting. This pin sets the shutdown discharging voltage based on the BAT node voltage level.
2	TERM	Termination Charging Voltage. This pin sets the terminal charging voltage based on the BAT node voltage level.
3	AGND	Analog Ground. Connect the exposed pad to the analog ground on the board.
4	MINOP	Minimum Operating Power. Place a resistor on this pin to set the minimum operation input voltage level. The boost regulator starts switching after the CBP voltage exceeds the MINOP voltage. Connect this pin to AGND to disable MINOP function.
5	MPPT	Maximum Power Point Tracking. This pin sets the maximum power point tracking level for different energy harvesters. To disable MPPT, float this pin.
6	CBP	Capacitor Bypass. Samples and holds the maximum power point level. Connect a 10 nF capacitor from this pin to AGND. When MPPT is disabled, tie CBP to an external reference that is lower than VIN.
7	VIN	Input Supply from Energy Harvester Source. Connect at least a 4.7 µF capacitor as close as possible between this pin and PGND.
8	PGND	Power Ground.
9	SW	Switching Node for the Inductive Boost Regulator with a Connection to the External Inductor. Connect a 22 µH inductor between this pin and VIN.
10	BAT	Places Rechargeable Battery or Super Capacitor as a Storage for SYS Output Supply.
11	SYS	Output Supply to System Load. Connect at least a 4.7 µF capacitor as close as possible between this pin and PGND.
12	BACK_UP	Optional Input Supply from the Backup Primary Battery Cell.
13	PGOOD	Output Supply. Maintain a logic high signal when SYS voltage is higher than the SETPG threshold.
14	DIS_SW	Control Signal from the MCU or RF Transceiver. Stop the main boost switching by pulling this pin high. Enable the main boost switching by pulling this pin low.
15	REF	Provides Bias Voltage for the SETSD, TERM, and SETPG Pins. Connect the high side of the resistor divider networks to this bias voltage.
16	SETPG	Sets Power Good Voltage Based on the SYS Node Voltage Level.
	EPAD	Exposed Pad. The exposed pad must be connected to AGND.

TYPICAL PERFORMANCE CHARACTERISTICS

I_{VIN} = 5 mA, V_{BAT_TERM} = 3.5 V, V_{SYS_PG} = 3.0 V, V_{BAT_SD} = 2.4 V, MPPT ratio (OCV) = 80%, L = 22 µH, C_{IN} = C_{SYS} = 4.7 µF, C_{CBP}= 10 nF.

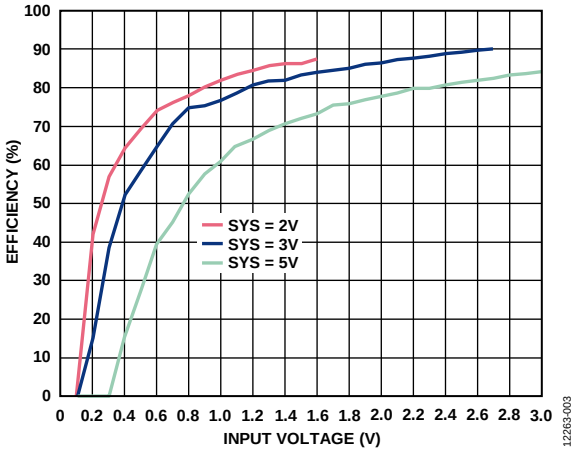

Figure 3. Efficiency vs. Input Voltage, I_{IN} = 10 µA

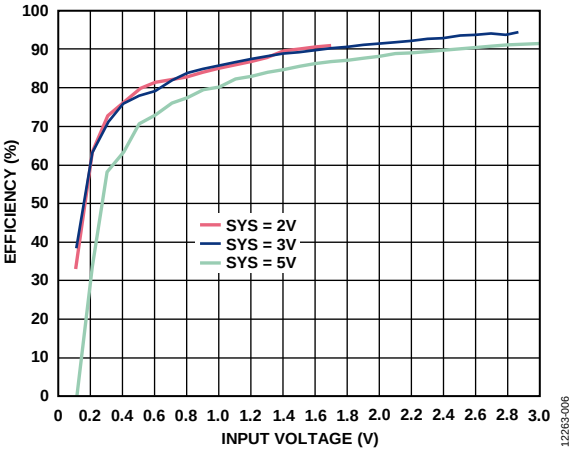

Figure 6. Efficiency vs. Input Voltage, I_{IN} = 100 µA

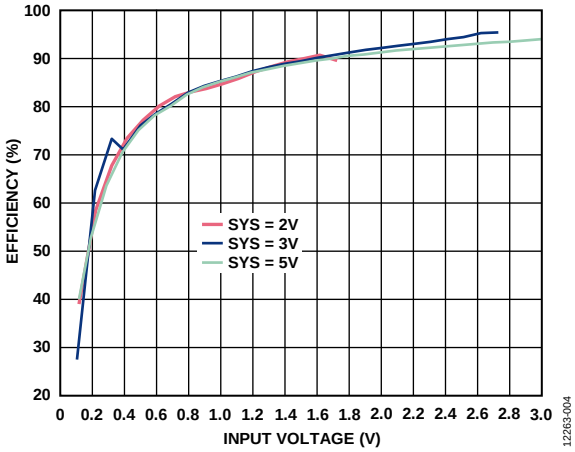

Figure 4. Efficiency vs. Input Voltage, I_{IN} = 10 mA

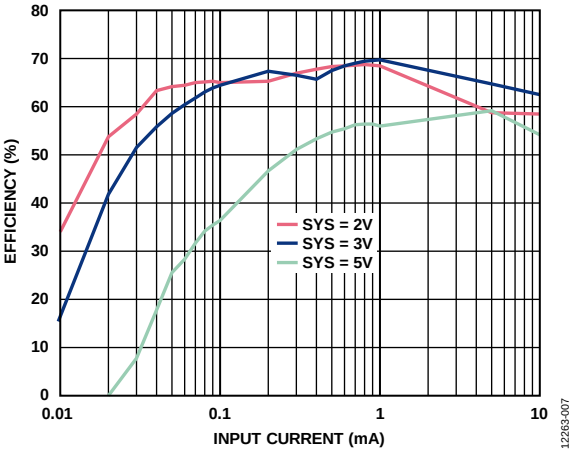

Figure 7. Efficiency vs. Input Current, V_{IN} = 0.2 V

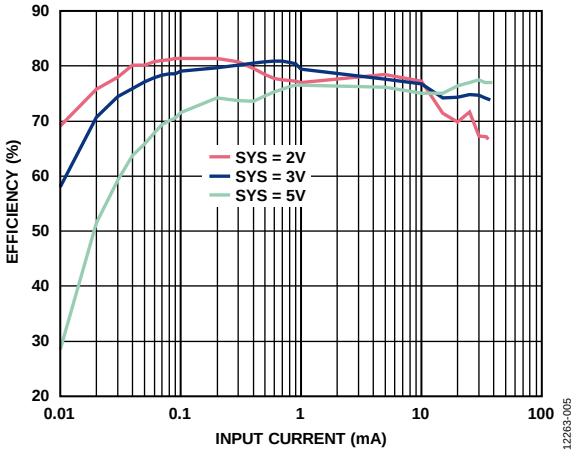

Figure 5. Efficiency vs. Input Current, V_{IN} = 0.5 V

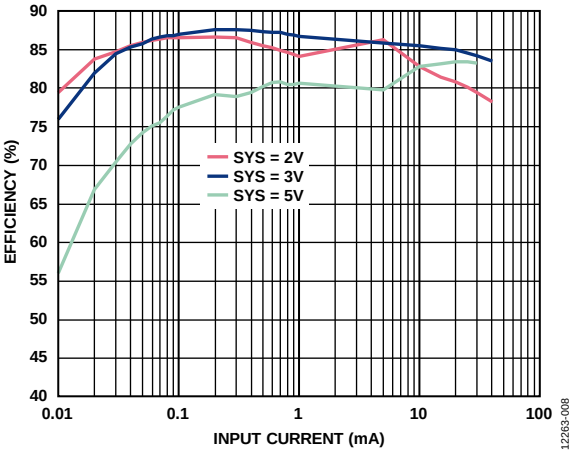

Figure 8. Efficiency vs. Input Current, V_{IN} = 1 V

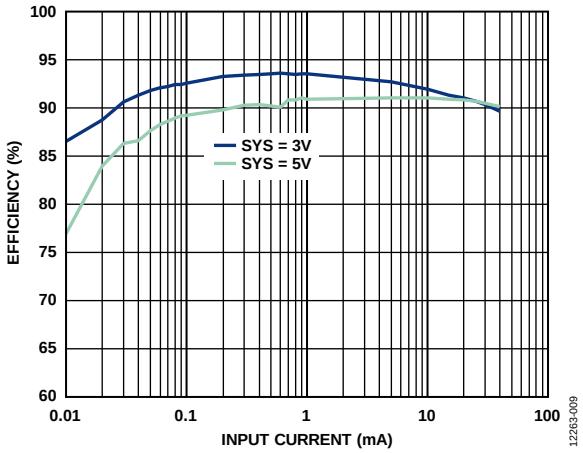

Figure 9. Efficiency vs. Input Current, V_{IN} = 2 V

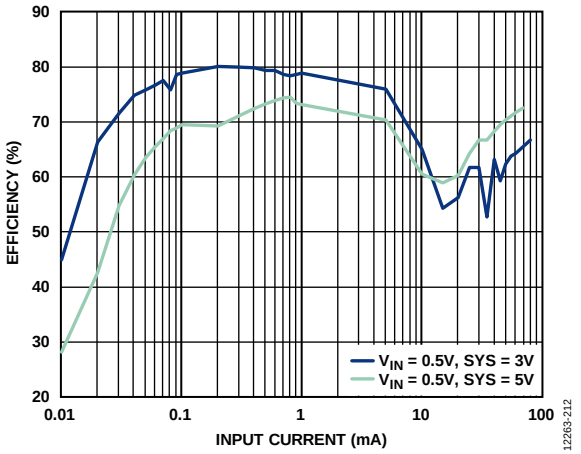

Figure 12. ADP5090ACPZ-2-R7 Efficiency vs. Input Current, V_{IN} = 0.5 V

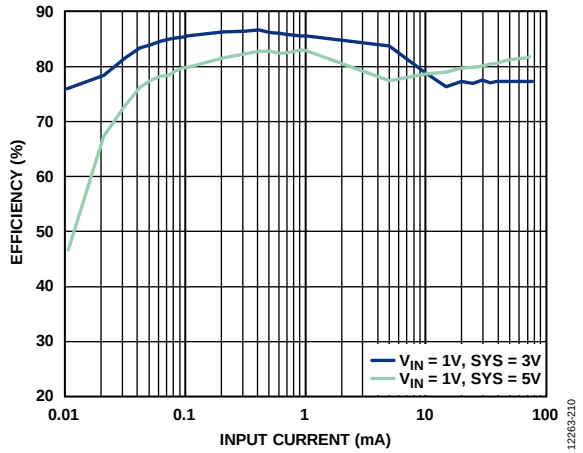

Figure 10. ADP5090ACPZ-2-R7 Efficiency vs. Input Current, V_{IN} = 1 V

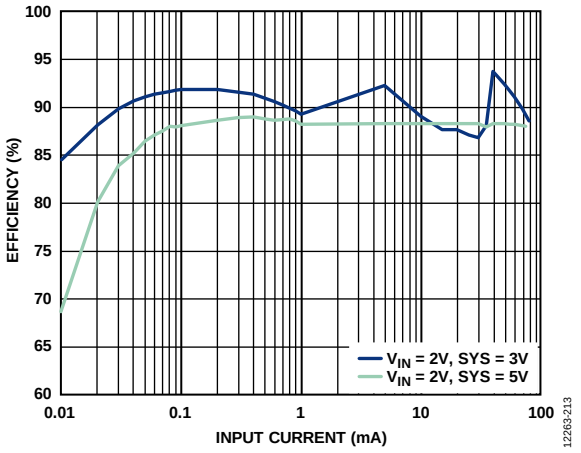

Figure 13. ADP5090ACPZ-2-R7 Efficiency vs. Input Current, V_{IN} = 2 V

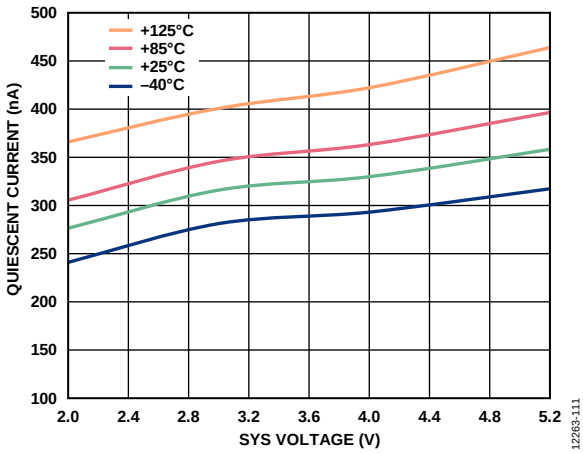

Figure 11. Quiescent Current vs. SYS Voltage ($V_{MPPT} \geq V_{MINOP}$)

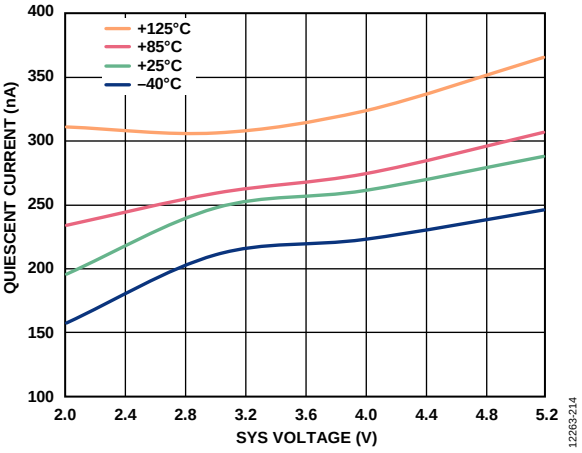

Figure 14. Quiescent Current vs. SYS Voltage ($V_{MPPT} < V_{MINOP}$)

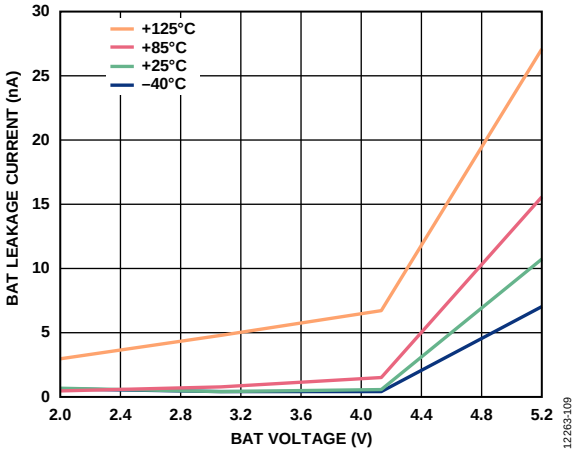

Figure 15. BAT Leakage Current vs. BAT Voltage

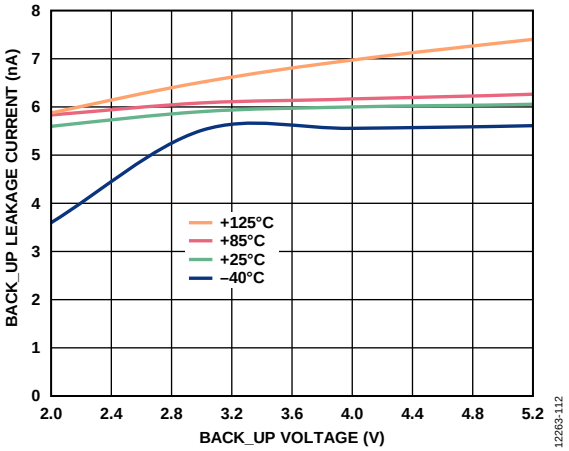

Figure 18. BACK_UP Leakage Current vs. BACK_UP Voltage

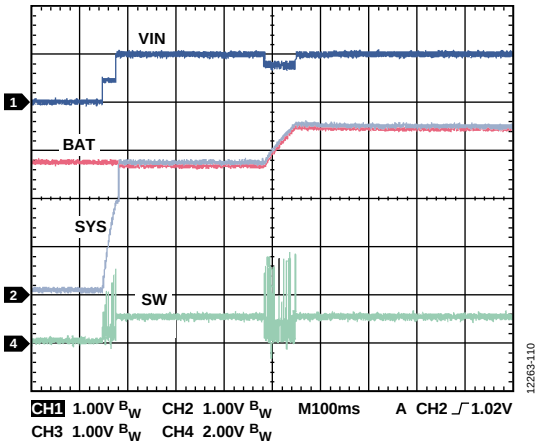

Figure 16. Startup with 100 µF Battery, $V_{BAT} > V_{BAT\_SD}$

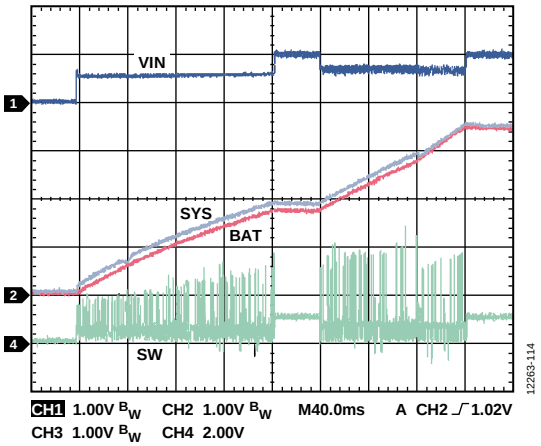

Figure 19. Startup with Empty 100 µF Battery

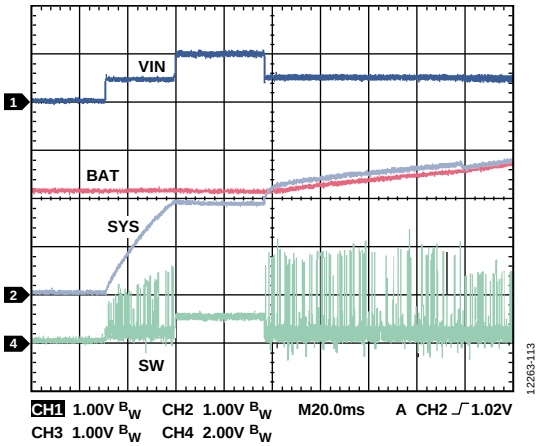

Figure 17. Startup with 100 µF Battery, $V_{BAT} < V_{BAT\_SD}$

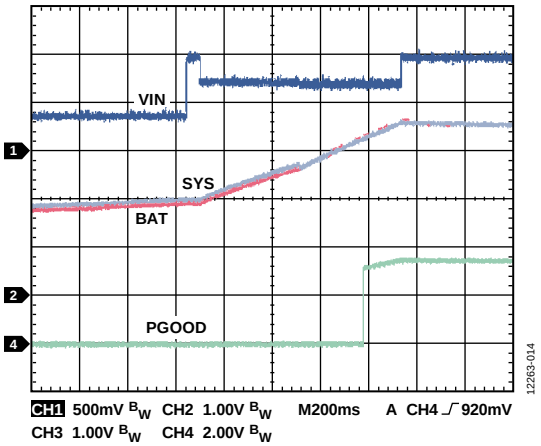

Figure 20. PGOOD Function Waveform

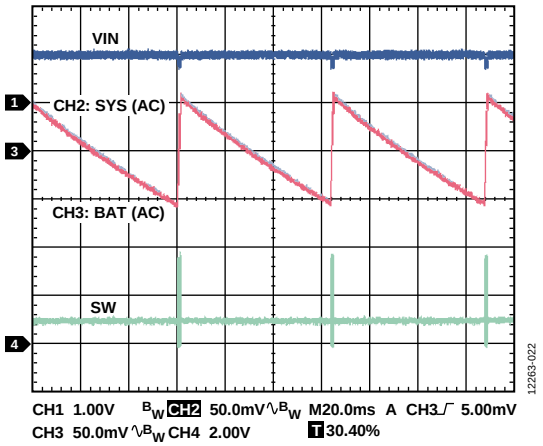

Figure 21. Output Ripple of TERM Function with 100 µA Load

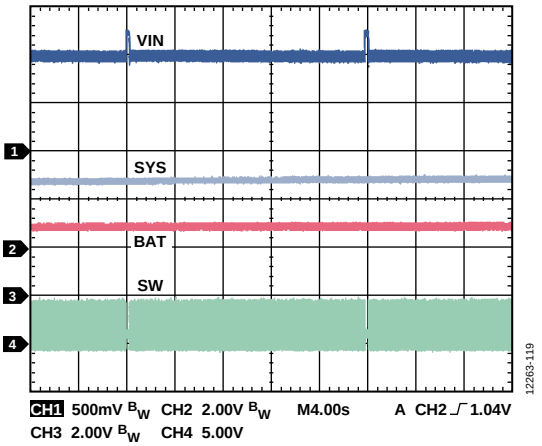

Figure 24. MPPT Sampling Cycle Waveform

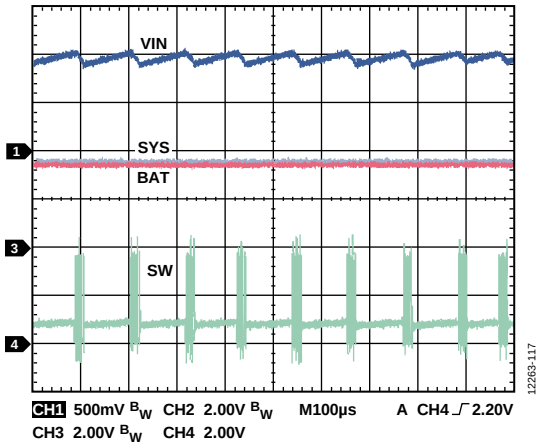

Figure 22. Main Boost PFM Waveform with 200 µA Load

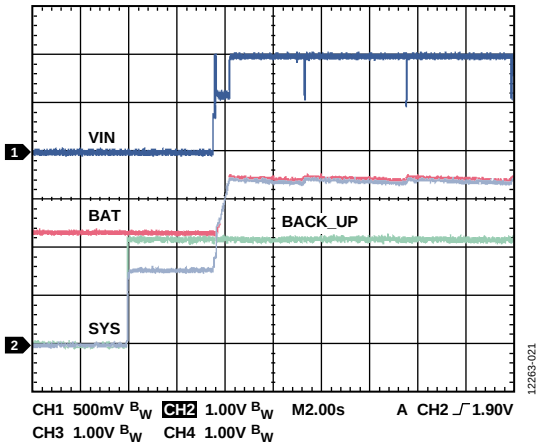

Figure 25. Backup Function, $V_{BACK\_UP} < V_{BAT}$

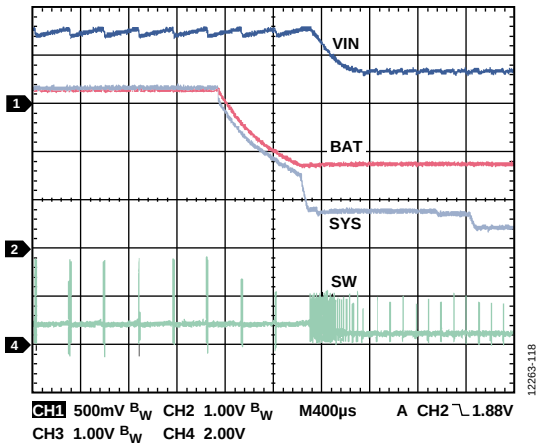

Figure 23. Battery Protection Function Waveform

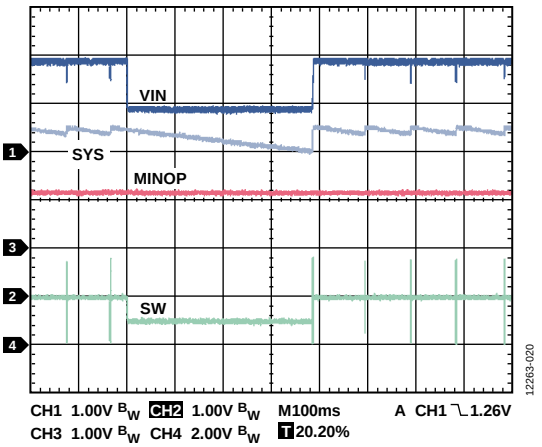

Figure 26. MINOP Function Waveform

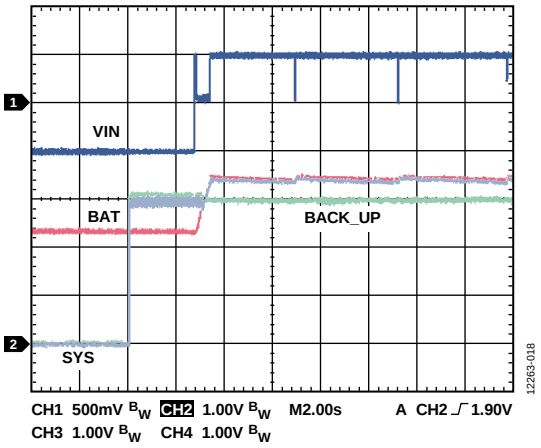

Figure 27. Backup Function, $V_{BACK\_UP} > V_{BAT}$

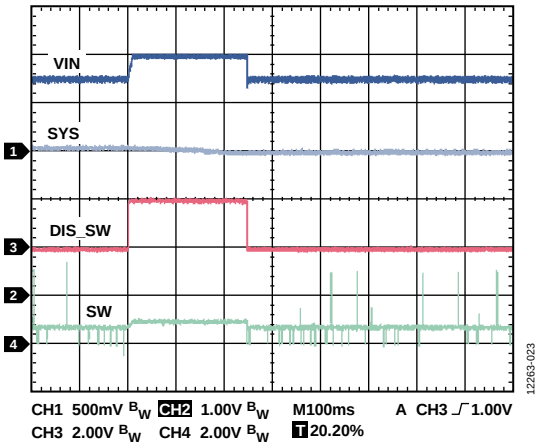

Figure 28. DIS_SW Function Waveform

DETAILED FUNCTIONAL BLOCK DIAGRAM

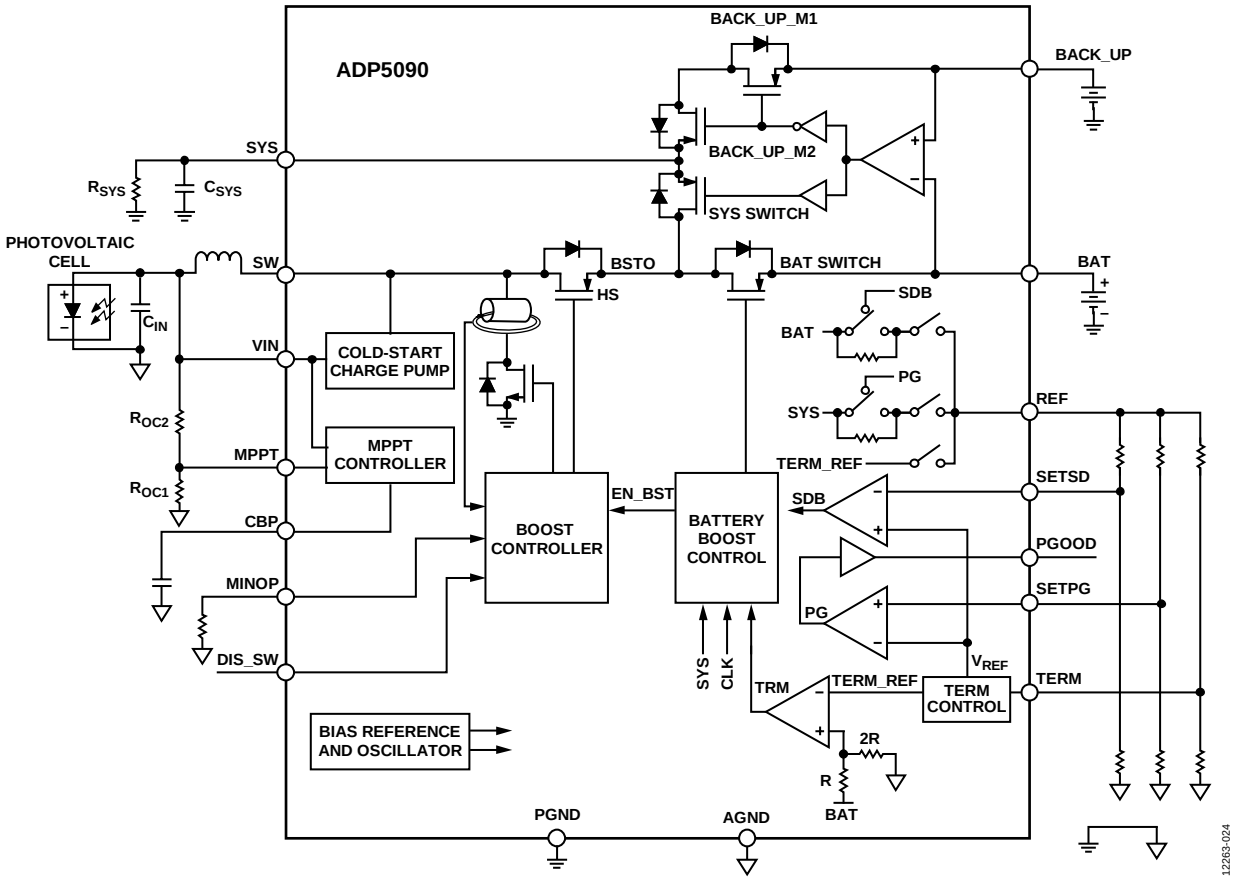

Figure 29. Detailed Functional Block Diagram

THEORY OF OPERATION

The ADP5090 combines a nano powered boost regulator with a storage elements management controller. It converts power from low voltage, high impedance dc sources such as PV cells, TEGs, and piezoelectric modules. The device stores power in the rechargeable battery or capacitor with storage protection, and provides power to the load. It can also control an additional power path from a primary battery cell to the system.

The ADP5090 includes a cold start up circuit, a synchronous boost controller with integrated MOSFETs, a charge controller with an integrated switch, and switches for the backup power path. The boost can be stopped temporarily by an external signal to prevent interference with RF transmission.

COLD STARTUP ($V_{SYS} < V_{SYS\_TH}$, $V_{IN} > V_{IN\_COLD}$)

The cold startup circuit is required when the VIN pin is above V_{IN_COLD}, and the energy storage voltage at the SYS pin is below V_{SYS_TH}, above which the boost regulator and energy storage controller start working. The charge-pump cold startup circuit extracts the energy available at the VIN pin and charges the capacitors at the SYS pin and the BAT pin up to V_{SYS_TH}. The energy harvester must supply sufficient power to complete cold startup (see the Energy Harvester Selection section for more information). The cold start circuit, with lower efficiency compared to the boost regulator, can achieve a short startup time, creating a low shutdown current system load enabled by the PGOOD signal. To bypass the cold startup, place a primary battery at the BACK_UP pin (see the Backup Storage Path section for more information).

BOOST REGULATOR ($V_{BAT\_TERM} > V_{SYS} \geq V_{SYS\_TH}$)

The switching mode synchronous boost regulator, with an external inductor connected between the VIN and SW pins, operates in pulse frequency mode (PFM), transferring energy stored in the input capacitor to the system load (SYS) and energy storage connected to the BAT pin. The boost control loop regulates the VIN voltage at the level sampled at the MPPT pin and stored at the capacitor connected to the CBP pin. To maintain the high efficiency of the regulator across a wide input power range, the current sense circuitry employs the internal dither peak current limit to control the inductor current.

The boost regulator operation turns off the SYS and BAT switches as an asynchronous mode via the energy storage controller when the BAT pin voltage is below the battery discharging protection threshold programmed at the SETSD pin, or stops switching when the BAT pin voltage is above the battery overcharging threshold programmed at the TERM pin. The boost regulator is disabled when the voltage of the CBP pin decreases to the threshold set by the resistor at the MINOP pin. In addition, the boost is periodically stopped by the open voltage sampling circuit, and can be temporary disabled by driving the DIS_SW pin high.

VIN OPEN CIRCUIT AND MPPT

The boost regulation reference is the VIN pin open circuit voltage scaled to a ratio programmed by the resistor divider at the MPPT pin. This voltage is periodically sampled and stored in the capacitor connected to the CBP pin. This storage keeps the VIN voltage operating at the level of maximum power points available from the energy harvester at the input of the ADP5090. The reference voltage refreshes every 19 sec by periodically disabling the boost regulator for 296 ms and sampling the open circuit voltage. The reference voltage is set by the following equation:

$$V_{MPPT} = V_{IN}\left(Open\ Circuit\right)\left(\frac{R_{OC1}}{R_{OC1} + R_{OC2}}\right) \quad (1)$$

The typical MPPT ratio depends on the type of harvester. For example, it is around 0.8 for PV cells, and 0.5 for TEGs. The MPPT can be disabled and left floating. Set the CBP pin to an external voltage reference lower than the VIN voltage. If the input source is an ideal voltage source, connect the MPPT and CBP pins to ground.

ENERGY STORAGE CHARGE MANAGEMENT

Energy storage is connected to the BAT pin. The storage can be a rechargeable battery, super capacitor, or 100 µF or larger capacitor. The energy storage controller manages the charging and discharging operations, monitors the SYS pin voltage, and asserts the PGOOD signal high when it is above the threshold programmed at the SETPG pin.

When the BAT pin voltage exceeds the charging protection threshold programmed at the TERM pin, the boost operation terminates to prevent battery overcharging. The overcharging protection threshold is programmable from 2.2 V to 5.2 V. When the BAT voltage drops below the discharging protection threshold level programmed at SETSD pin, the switches between the BAT pin and SYS pin are opened to prevent a deep, destructive battery discharge, and the boost reaches asynchronous mode. Although there is no current limit at the SYS and BAT pins, it is recommended to limit the system load current to lower than 800 mA. The large system load current generates a droop between the SYS pin and the rechargeable battery at the BAT pin, with consideration given to the resistance of the SYS switch, the BAT switch, and the rechargeable battery internal resistance.

When no input source is attached, discharge the SYS pin to ground before attaching a storage element to the BAT pin. After hot plugging a charged storage element, release the SYS pin because the SYS voltage below V_{SYS_TH} results in the BAT switch remaining off to protect the storage element until the SYS voltage reaches V_{SYS_TH}. This can be described as store mode, a state with the lowest leakage (0.5 nA, typical) that allows a long store period without discharging the storage element on BAT.

BACKUP STORAGE PATH

The ADP5090 provides an optional backup storage energy path, an integrated backup controller, and two back to back power switches between the BACK_UP pin and the SYS pin. When the system operates at a condition where the harvested and stored energy is periodically insufficient, a backup energy storage element can be attached to the BACK_UP pin. The backup controller enables when the SYS voltage is above 1.5 V (typical). When the BACK_UP pin voltage is higher than the BAT pin voltage, it turns on the internal power switches between the BACK_UP pin and the SYS pin. When the BACK_UP pin voltage is lower than the BAT pin voltage, the internal power switches are turned off. The 185 mV (typical) comparator input offset of the BAT pin prevents the input source and BAT pin charging the BACK_UP pin (see Figure 32).

In addition, the backup storage element can bypass the cold startup with inrush current protection circuitry. When the system current exceeds the internal current limit of 400 mA (typical), the BACK_UP switches turn off. Nevertheless, the current capability is only 250 µA (typical) when plugging in the backup battery for the first time. Restricting the system load current from the SYS pin ensures that the power path can enter normal operation status. Table 6 explains the power path working state. For long-term store mode, remove the backup storage element and then discharge SYS to ground.

MINOP FUNCTION

When the energy generated by the harvester cannot sustain the steady working state, the MINOP function can disable the boost regulator to prevent discharging the storage element. The MINOP function disables the MPPT function to achieve the lowest quiescent current of 260 nA (typical). When the voltage of the CBP pin decreases to the threshold set by the resistor at the MINOP pin, the boost regulator stops switching. Disable this function by connecting MINOP to AGND. The typical MINOP bias current is 2 µA.

DISABLING BOOST

For noise or EMI sensitive applications, the boost switcher can be stopped temporarily by pulling the DIS_SW pin high to prevent interference with RF circuits. The boost switching resumes when the DIS_SW pin is pulled low. The transition delay is less than 1 µs (typical).

BATTERY OVERCHARGING PROTECTION

To prevent rechargeable batteries from being overcharged and damaged, the battery terminal voltage (V_{BAT_TERM}) must be set by using external resistors. Figure 30 shows the V_{BAT_TERM} rising threshold voltage given by Equation 2.

$$V_{BAT\_TERM} = \frac{3}{2} V_{REF}\left(1 + \frac{R_{TERM1}}{R_{TERM2}}\right) \quad (2)$$

Considering the quiescent current consumption, the sum of the resistors must be more than 6 MΩ, that is,

$$R_{TERM1} + R_{TERM2} \geq 6\ M\Omega$$

The overvoltage falling threshold is given by $V_{BAT\_TERM\_HYS}$, which is internally set to the overvoltage threshold minus an internal hysteresis voltage denoted by $V_{BAT\_TERM\_HYS}$. When the voltage at the battery exceeds the V_{BAT_TERM} threshold, the main boost regulator is disabled. The main boost starts again when the battery voltage falls below the $V_{BAT\_TERM\_HYS}$ level. When the input energy is excessive, the VBAT pin voltage ripples between the V_{BAT_TERM} and the $V_{BAT\_TERM\_HYS}$ levels.

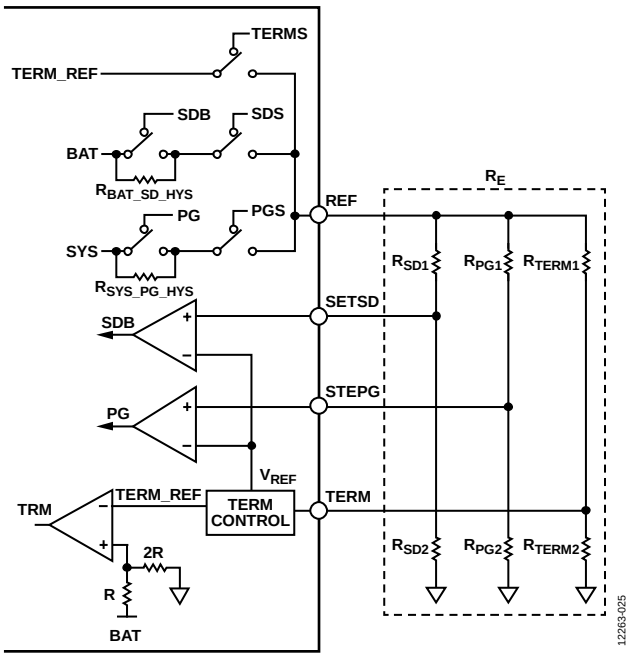

Figure 30. The ADP5090 Program Paramater Setting

BATTERY DISCHARGING PROTECTION

To prevent rechargeable batteries from being deeply discharged and damaged, the battery discharge shutdown voltage (V_{BAT_SD}) must be set by using external resistors. Figure 30 shows the V_{BAT_SD} falling threshold voltage given by Equation 3.

$$V_{BAT\_SD} = V_{REF}\left(1 + \frac{R_{SD1}}{R_{SD2}}\right) \quad (3)$$

The ADP5090 has an internal resistor, $R_{BAT\_SD\_HYS}$ = 103.5 kΩ (typical), to program the hysteresis, given by Equation 4.

$$V_{BAT\_SD\_HYS} = V_{BAT\_SD} \times \frac{R_{BAT\_SD\_HYS}}{R_E} \quad (4)$$

where $V_{BAT\_SD\_HYS}$ contains an internal resistor to program the hysteresis.

Considering the quiescent current consumption, the sum of the resistors that comprise the resistor divider ($R_{BAT\_SD\_HYS}$, R_{SD1}, and R_{SD2}) must be more than 6 MΩ, that is,

$$R_{BAT\_SD\_HYS} + R_{SD1} + R_{SD2} \geq 6\ M\Omega$$

The equivalent resistor of the three external configuration resistor dividers, R_E, is equivalent to the paralleling value of the three resistor dividers.

POWER GOOD (PGOOD)

The ADP5090 allows users to set a programmable PGOOD voltage (V_{PGOOD}) threshold, which indicates the SYS voltage is at an acceptable level. It must be set using external resistors. Figure 30 shows the V_{PGOOD} falling threshold voltage given by Equation 5.

$$V_{SYS\_PGOOD} = V_{REF}\left(1 + \frac{R_{PG1}}{R_{PG2}}\right) \quad (5)$$

The ADP5090 has an internal resistor to program the hysteresis, $R_{SYS\_PG\_HYS}$ = 103.5 kΩ (typical), given by Equation 6.

$$V_{SYS\_PGOOD\_HYS} = V_{SYS\_PGOOD} \times \frac{R_{SYS\_PG\_HYS}}{R_E} \quad (6)$$

where $V_{SYS\_PGOOD\_HYS}$ is the PGOOD hysteresis voltage.

The equivalent resistor of the three external configuration resistor dividers, R_E, is recommended to be comprised of the same three resistor dividers for easy resistor selection. Considering the quiescent current consumption, the sum of the resistors that comprise the power good resistor divider ($R_{SYS\_PG\_HYS}$, R_{PG1}, and R_{PG2}) must be more than 6 MΩ, that is,

$$R_{SYS\_PG\_HYS} + R_{PG1} + R_{PG2} \geq 6\ \text{MΩ} \quad (7)$$

The logic high level on PGOOD is equal to the SYS voltage and the logic low level is ground. The logic high level has approximately 11.8 kΩ (typical) internally in series to limit the available current. The V_{PGOOD} threshold must be greater than or equal to the V_{BAT_SD} threshold.

For the best operation of the system, set up PGOOD to drive an external PFET between SYS and the system load via an inverter in order to determine when the load can be connected or removed to optimize the storage element capacity (see Figure 36). It is necessary to complete the cold start-up if the system load cannot be disabled.

Table 5 shows programming threshold resistor examples corresponding to various voltages with a 10 MΩ resistor divider. Figure 31 shows states of various threshold voltages.

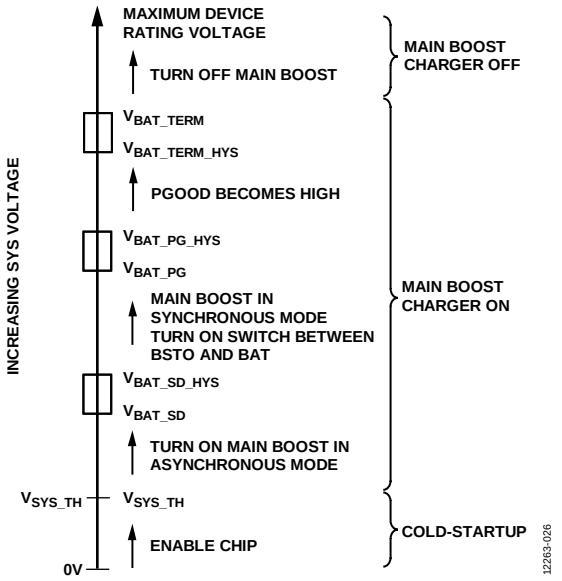

Figure 31. States of Various Threshold Voltages

Table 5. Programming Threshold Resistors

Voltage Threshold (V)	R_{SD1} and R_{PG1} (MΩ)	R_{SD2} and R_{PG2} (MΩ)	R_{TERM1} (MΩ)	R_{TERM2} (MΩ)
2	3.92	6.04	Not applicable	Not applicable
2.1	4.22	5.76	Not applicable	Not applicable
2.2	4.53	5.49	1.74	8.25
2.3	4.75	5.23	2.1	7.87
2.4	4.99	5	2.43	7.5
2.5	5.11	4.87	2.74	7.32
2.6	5.36	4.64	3.01	6.98
2.7	5.49	4.53	3.3	6.65
2.8	5.62	4.32	3.48	6.49
2.9	5.76	4.22	3.74	6.2
3	5.9	4.02	3.92	6.04
3.1	6.04	3.9	4.12	5.9
3.2	6.2	3.74	4.32	5.62
3.3	6.34	3.65	4.53	5.49
3.4	6.49	3.57	4.64	5.36
3.5	6.49	3.48	4.87	5.23
3.6	6.65	3.4	4.99	5
3.7	6.8	3.3	5.1	4.87
3.8	6.81	3.2	5.23	4.75
3.9	6.98	3.09	5.36	4.64

Voltage Threshold (V)	R_{SD1} and R_{PG1} (MΩ)	R_{SD2} and R_{PG2} (MΩ)	R_{TERM1} (MΩ)	R_{TERM2} (MΩ)
4	6.98	3.01	5.49	4.53
4.1	6.98	2.94	5.6	4.42
4.2	7.15	2.87	5.62	4.32
4.3	7.15	2.8	5.76	4.22
4.4	7.32	2.74	5.9	4.12
4.5	7.32	2.7	5.9	4.02
4.6	7.32	2.61	6.04	3.92
4.7	7.5	2.55	6.19	3.83
4.8	7.5	2.5	6.2	3.74
4.9	7.5	2.49	6.34	3.74
5	7.5	2.43	6.34	3.65
5.1	7.68	2.37	6.49	3.57
5.2	7.68	2.32	6.49	3.48

Table 6. Power Path Working State

Power Path	Power Condition	Main Boost	BAT Switch	SYS Switch	BACK_UP_M1	BACK_UP_M2
Without Backup Battery	$V_{SYS} > V_{SYS\_TH}$, $V_{BAT\_SD} > V_{BAT}$	Asynchronous	Off	Off	Off	Off
	$V_{BAT\_TERM} > V_{BAT} = V_{SYS} > V_{BAT\_SD}$	Synchronous	On	On	Off	Off
	$V_{SYS} > V_{SYS\_TH}$, $V_{BAT} > V_{BAT\_TERM}$	Disabled	On	On	Off	Off
With Backup Battery	$V_{SYS} > V_{SYS\_TH}$, $V_{BACK\_UP} > V_{BAT} > V_{BAT\_SD}$	Synchronous	On	Off	On	On
	$V_{SYS} > V_{SYS\_TH}$, $V_{BACK\_UP} > V_{BAT\_SD} > V_{BAT}$	Asynchronous	Off	Off	On	On
	$1.5\ V < V_{SYS} < V_{SYS\_TH}$, $V_{SYS} < V_{BACK\_UP}$	Disabled	Off	Off	On	On
	$V_{SYS} < 1.5\ V$	Disabled	Off	Off	Off	Off

POWER PATH WORKING FLOW

Figure 32 shows the power switches structure when the backup primary battery is implemented. When the BACK_UP voltage is higher than the BAT voltage, the SYS switch prevents the BACK_UP primary battery from charging the BAT pin. Meanwhile, the BAT offset avoids input source charging BACK_UP primary battery. Table 6 shows the power path working state.

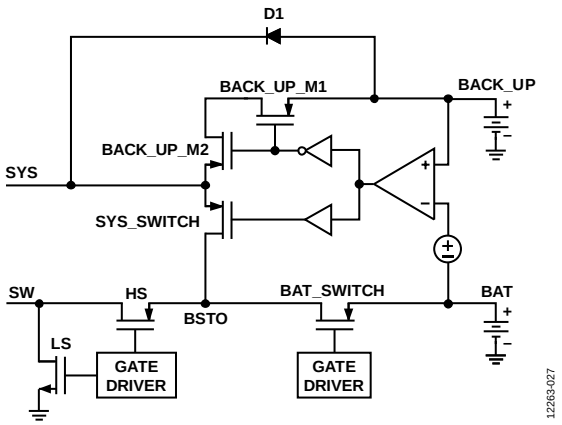

Figure 32. Power Switches Structure

CURRENT-LIMIT AND SHORT-CIRCUIT PROTECTION

The boost regulator in the ADP5090 includes current-limit protection circuitry to limit the amount of positive current flowing through the low-side boost switch. It is a cycle-by-cycle, three level peak current-limit protection with a third level of 100 mA (typical).

Although there is no current limit at the SYS and BAT pins, it is recommended to limit the system load current to lower than 800 mA. The total resistance of the SYS switch and the BAT switch (1.03 Ω, typical), generates a voltage drop when the system load sinks a large current from BAT. It is necessary to consider the internal resistance of the storage elements connected to the BAT pin.

The BACK_UP power path current limit of 400 mA (typical) protects the primary battery sinking large current. When the current from the BACK_UP pin is higher than the current limit, the BACK_UP switches turn off.

THERMAL SHUTDOWN

In the event that the ADP5090 junction temperature rises above 125°C, the thermal shutdown (TSD) circuit turns off the switch between the BAT pin and the SYS pin to prevent the damage of energy storage at a high ambient temperature. The boost operation is also terminated. A 15°C hysteresis is included, allowing the ADP5090 to return to operation when the on-chip temperature drops below 110°C. When coming out of TSD, the boost regulator and the energy storage controller resume the functions.

APPLICATIONS INFORMATION

The ADP5090 extracts the energy from the VIN pin to charge the SYS and BAT pins. This occurs in three stages: cold start, asynchronous boost, and synchronous boost. This section describes the procedures for selecting the external components to maintain the energy transmission system with the layout and assembly consideration.

ENERGY HARVESTER SELECTION

The energy harvester input source must provide a minimum level of power for cold start, asynchronous boost, and synchronous boost. The minimum input power required to complete cold start can be estimated using the following equation:

$$V_{IN} \times I_{IN} \times \eta_{COLD} > V_{SYS\_TH} \times (I_{STR\_LEAK} + I_{SYS\_LOAD})$$

where:

V_{IN} is clamped to V_{IN_COLD} = 380 mV (typical), which indicates cold start real input power.

I_{IN} is the input current.

η_{COLD} is the cold start efficiency, which is about 5% to 7%.

V_{SYS_TH} is the current with the bias voltage, and an estimation of worst case.

I_{STR_LEAK} is the storage element leakage current at the BAT pin.

I_{SYS_LOAD} is the system load current of the SYS pin. Minimizing the system load accelerates the cold start. Programming the PGOOD threshold to enable the system load current is recommended.

After the ADP5090 completes the cold start, the MPPT function enables. To meet the average system load current, the input source must provide the boost regulator with enough power to charge the storage element fully while the system is in low power or sleep mode. The power required by the system can be estimated using the following equation:

$$V_{IN} \times I_{IN} \times \eta_{BOOST} > V_{BAT\_TERM} \times (I_{STR\_LEAK} + I_{SYS\_LOAD})$$

where:

V_{IN} is regulated to the CBP pin voltage (MPPT ratio × OCV).

I_{IN} is the input current.

η_{BOOST} is the boost regulator efficiency. See the efficiency figures in the Typical Performance Characteristics section for more information.

V_{BAT_TERM} is the current with the bias voltage, and an estimation of worst case.

I_{STR_LEAK} is the storage element leakage current at the BAT pin.

I_{SYS_LOAD} is the average system load current of the SYS pin.

ENERGY STORAGE ELEMENT SELECTION

In order to protect the storage element from overcharging or overdischarging, the storage element must be connected to the BAT pin and the system load tied to the SYS pin. The ADP5090 supports many types of storage elements, such as rechargeable batteries, super capacitors, and conventional capacitors. A storage element with a 100 µF equivalent capacitance is required to filter the pulse currents of the PFM switching converter. The storage element capacity must provide the entire system load when the input source is no longer generating power.

If there is high pulse current or the storage element has significant impedance, it may be necessary to increase the SYS capacitor from the 4.7 µF minimum, or add additional capacitance to the BAT pin in order to prevent a droop in the SYS voltage. Note that increasing the SYS capacitor causes the boost regulator to operate in the less efficient cold start stage for a longer period at startup. If the application cannot accept the longer cold start time, place the additional capacitor parallel to the storage element. See the Capacitor Selection section for more information.

INDUCTOR SELECTION

The boost regulator needs an appropriate inductor for proper operation. The inductor saturation current must be at least 30% higher than the expected peak inductor currents, as well as a low series resistance (DCR) to maintain high efficiency. The boost regulator internal control circuitry is designed to optimize the efficiency and control the switching behavior with a nominal inductance of 22 µH ± 20%. Table 7 lists some recommended inductors.

Table 7. Recommended Inductors

Vendor	Device No.	L (µH)	ISAT (A)	IRMS (A)	DCR (mΩ)
Würth Elektronik	74437324220	22	2	1	470
	744042220	22	0.6	0.88	255
Coilcraft	LPS4018-223M	22	0.8	0.65	360

CAPACITOR SELECTION

Low leakage capacitors are required for ultralow power applications that are sensitive to the leakage current. Any leakage from the capacitors reduces efficiency, increases the quiescent current, and degrades the MPPT effectiveness.

Input Capacitor

A capacitor C_{IN} connected to the VIN pin and the PGND pin stores energy from the input source. For the energy harvester, the source impedance is dominated by capacitive behavior. Scale the input capacitor according to the value of the output capacitance of the energy harvester; a minimum of 4.7 µF is recommended.

For the primary battery as an input source application, a larger capacitance helps to reduce the input voltage ripple and keep the source current stable in order to extend the battery life.

SYS Capacitor

The ADP5090 requires two capacitors to be connected between the SYS pin and the PGND pin. Connect a low ESR ceramic capacitor of at least 4.7 µF parallel to a high frequency bypass capacitor of 0.1 µF. Connect the bypass capacitor as close as possible between SYS and PGND.

CBP Capacitor

The operation of the MPPT pin depends on the sampled value of the OCV. The VIN pin is regulated to the voltage stored on the CBP capacitor. This capacitor is sensitive to leakage because the holding period is around 19 sec. As the capacitor voltage drops due to leakage, the VIN regulation voltage also drops and influences the effectiveness of MPPT. When the IC junction temperature exceeds 85°C, the leakage current of the CBP pin significantly increases so that a larger capacitance is beneficial to the effectiveness of the MPPT. It is recommended to keep the same RC time constant of the MPPT resistors and CBP capacitor (up to 220 nF) as the typical application circuit in Figure 33. Considering the time constant of the MPPT resistor divider and the CBP capacitor, a low leakage X7R or C0G 10 nF ceramic capacitor is recommended.

LAYOUT AND ASSEMBLY CONSIDERATIONS

Carefully consider the printed circuit board (PCB) layout during the design of the switching power supply, especially at high peak currents and high switching frequency. Therefore, it is recommended to use wide and short traces for the main power path and the power ground paths. Place the input capacitors, output capacitors, inductor, and storage elements as close as possible to the IC. It is most important for the boost regulator to minimize the power path from output to ground. Therefore, place the output capacitor as close as possible between the SYS pin and the PGND pin. Keep a minimum power path from the input capacitor to the inductor from the VIN pin to the PGND pin. Place the input capacitor as close as possible between the VIN pin and the PGND pin, and place the inductor close to the VIN pin and the SW pin. It is best to use vias and bottom traces for connecting the inductors to their respective pins. To minimize noise pickup by the high impedance threshold setting nodes (REF, TERM, SETSD, and SETPG), place the external resistors close to the IC with short traces.

The CBP capacitor must hold the MPPT voltage for 19 sec, as any leakage can degrade the MPPT effectiveness. During board assembly and cleaning, contaminants such as solder flux and residue may form parasitic resistance to ground, especially in humid environments with fast airflow. This can significantly degrade the voltage regulation and change threshold levels set by the external resistors. Therefore, it is recommended that no ground planes be poured near the CBP capacitor or the threshold setting resistors. In addition, the boards must be carefully cleaned. If possible, clean ionic contamination with deionized water for the CBP capacitor and the threshold setting resistors.

TYPICAL APPLICATION CIRCUITS

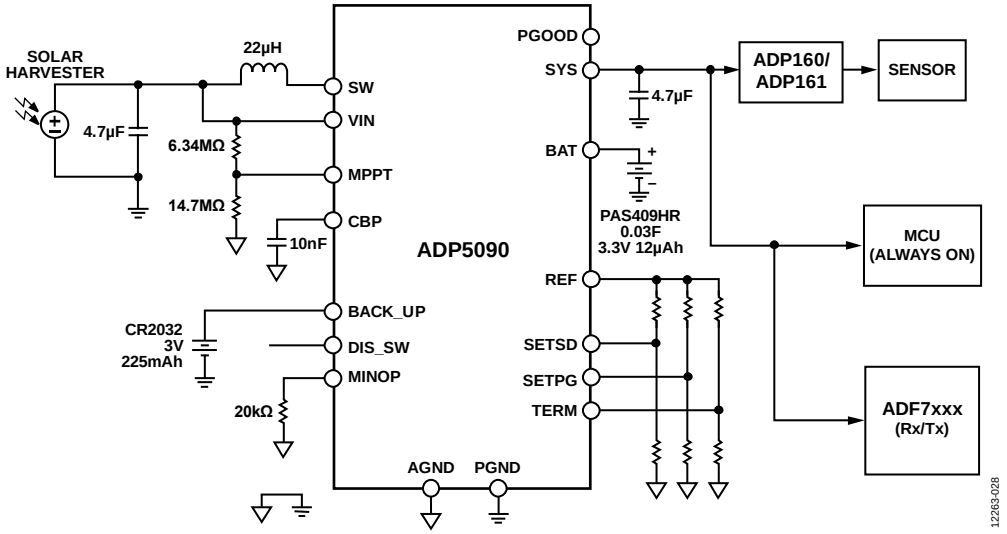

Figure 33. ADP5090 Based Energy Harvester Wireless Sensor Application with PV Cell as the Harvesting Energy Source (Trony 0.7 V, 60 µA, Alta Devices 0.72 V, 42 µA, Gcell 1.1 V, 100 µA), Shoei Electronics Polyacene Coin Type Capacitor PAS409HR as the Harvested Energy Storage, and Panasonic Primary Li-Ion Coin Cell CR2032 as the Backup Battery

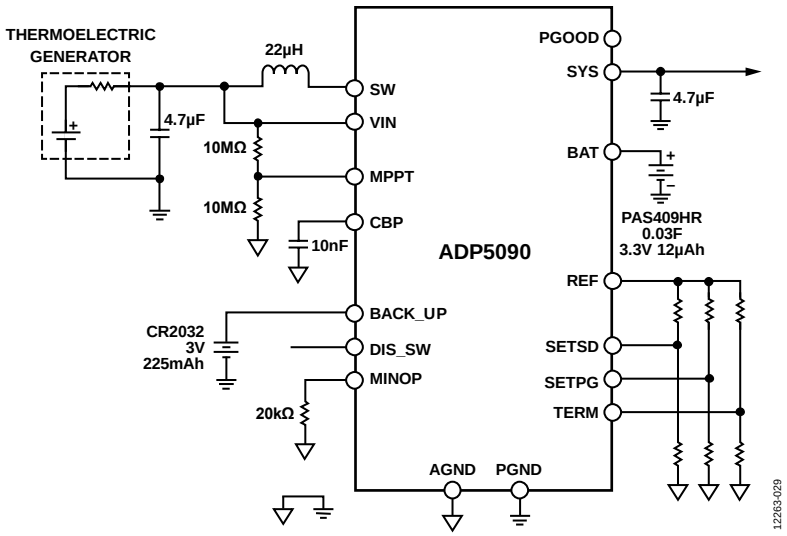

Figure 34. ADP5090 Based Energy Harvester Circuit with a Thermoelectric Generator as the Harvesting Energy Source, Shoei Electronics Polyacene Coin Type Capacitor PAS409HR as the Harvested Energy Storage, and Panasonic Primary Li-Ion Coin Cell CR2032 as the Backup Battery

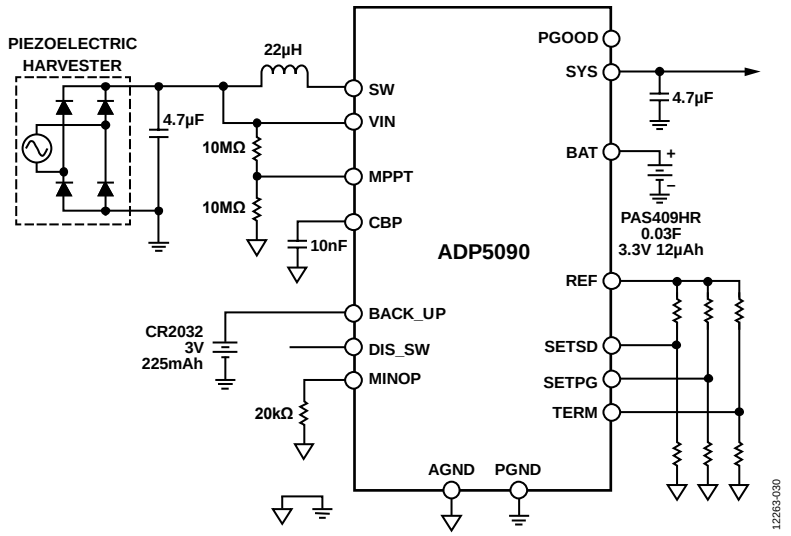

Figure 35. ADP5090 Based Energy Harvester Circuit with a Piezoelectric Generator as the Harvesting Energy Source, Shoei Electronics Polyacene Coin Type Capacitor PAS409HR as the Harvested Energy Storage, and Panasonic Primary Li-Ion Coin Cell CR2032 as the Backup Battery

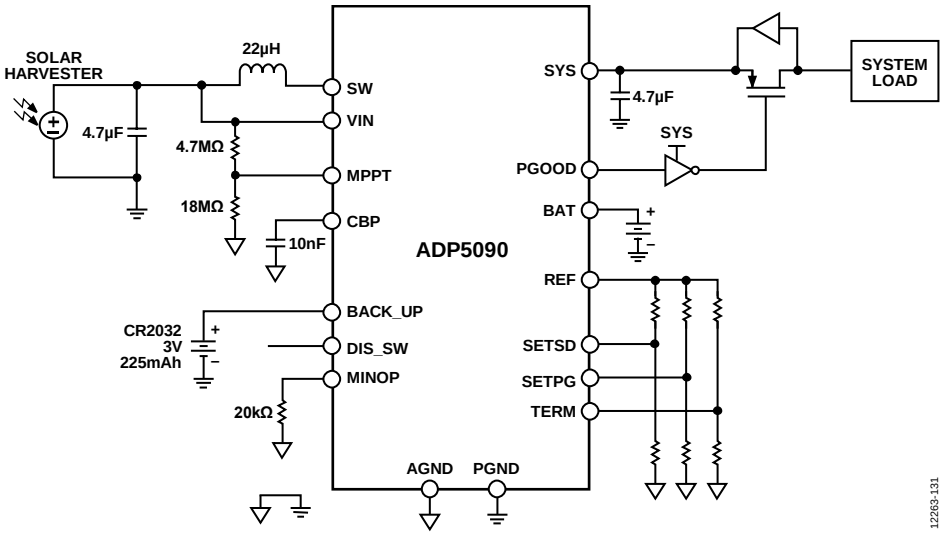

Figure 36. ADP5090 PGOOD Function Determines the Time to Enable the System Load

FACTORY PROGRAMMABLE OPTIONS

To order a device with options other than the default options, contact your local Analog Devices sales or distribution representative.

Table 8. Input Peak Current

Option	Description
Option 0	100 mA (default)
Option 1	195 mA

OUTLINE DIMENSIONS

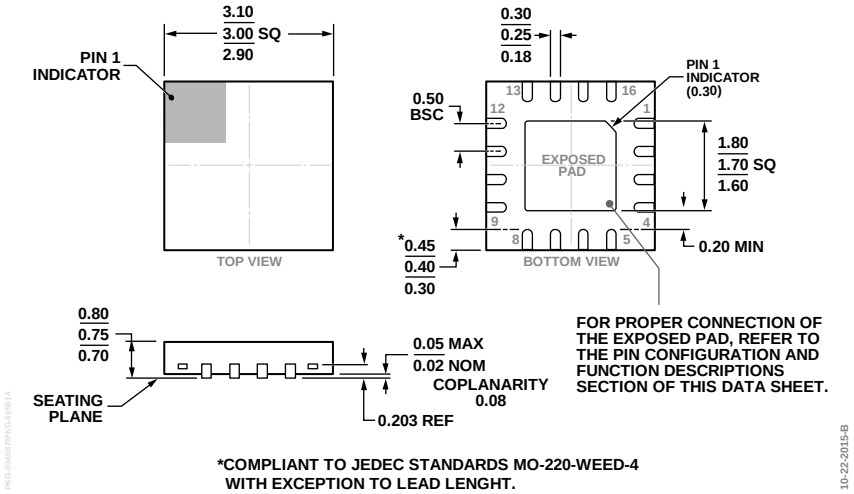

Figure 37. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
3 mm × 3 mm Body, Very Very Thin Quad
(CP-16-33)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADP5090ACPZ-1-R7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ], 100 mA Current Limit	CP-16-33	LPN
ADP5090ACPZ-2-R7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ], 195 mA Current Limit	CP-16-33	LT3
ADP5090-1-EVALZ		Evaluation Board		
ADP5090-2-EVALZ		Evaluation Board with Solar Harvester		

[1] Z = RoHS Compliant Part.