ADM709–SPECIFICATIONS (V_{CC} = Full Operating Range, $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
V_{CC} Operating Voltage Range	1.0		5.5	V	T_A = 0°C to +70°C
	1.2		5.5	V	T_A = –40°C to +85°C
Supply Current		35	85	µA	V_{CC} < 3.6 V, T_A = 0°C to +70°C
		35	110	µA	V_{CC} < 3.6 V, T_A = –40°C to +85°C
		65	150	µA	V_{CC} < 5.5 V, T_A = 0°C to +70°C
		65	200	µA	V_{CC} < 5.5 V, T_A = –40°C to +85°C
Reset Threshold	4.5	4.65	4.75	V	ADM709L
	4.25	4.40	4.50	V	ADM709M
	3.00	3.08	3.15	V	ADM709T
	2.85	2.93	3.00	V	ADM709S
	2.55	2.63	2.70	V	ADM709R
V_{CC} to $\overline{RESET}$ Delay		20		µs	V_{CC} = Reset Threshold max–min
$\overline{RESET}$ Active Time-Out Period	140	280	380	ms	V_{CC} = Reset Threshold max, V_{CC} Rising
$\overline{RESET}$ Output Voltage			0.3	V	ADM709R/S/T, I_{SINK} = 1.2 mA. V_{CC} = Reset Threshold min
			0.4	V	ADM709L/M, I_{SINK} = 3.2 mA. V_{CC} = Reset Threshold min
			0.3	V	I_{SINK} = 50 µA. $V_{CC} \geq$ 1.0 V
			0.4	V	I_{SINK} = 100 µA. $V_{CC} \geq$ 1.2 V
	0.8 × V_{CC}			V	ADM709R/S/T, I_{SOURCE} = 500 µA, $V_{CC} \geq$ Reset Threshold max
	V_{CC}–1.5 V			V	ADM709L/M, I_{SOURCE} = 800 µA, $V_{CC} \geq$ Reset Threshold max

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

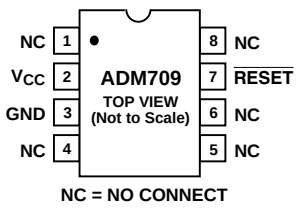
V_{CC} . . . . . –0.3 V to +6 V
$\overline{RESET}$ Output . . . . . –0.3 V to V_{CC} + 0.3 V
V_{CC} Input Current . . . . . 20 mA
$\overline{RESET}$ Output Current . . . . . 20 mA
Power Dissipation, N-8 DIP . . . . . 727 mW
θ_{JA} Thermal Impedance . . . . . 135°C/W
Power Dissipation, SO-8 SOIC . . . . . 470 mW
θ_{JA} Thermal Impedance . . . . . 110°C/W
Operating Temperature Range
Industrial (A Version) . . . . . –40°C to +85°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Vapor Phase (60 secs) . . . . . +215°C
Infrared (15 secs) . . . . . +220°C
Storage Temperature Range . . . . . –65°C to +150°C
ESD Rating . . . . . >5 kV

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

PIN FUNCTION DESCRIPTION

Mnemonic	Pin No.	Function
NC	1, 4, 5, 6, 8	No Connect Pins.
V_{CC}	2	+5 V, +3.3 V, +3 V Power Supply Input.
$\overline{RESET}$	7	Logic Output. It remains low while V_{CC} is below the reset threshold voltage and for 280 ms (typ) after V_{CC} rises above the threshold.
GND	3	Ground, 0 V.

PIN CONFIGURATION



NC = NO CONNECT

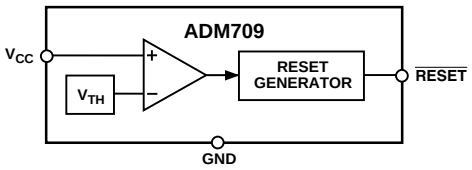


Figure 1. Functional Block Diagram

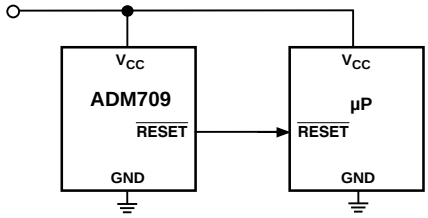


Figure 2. Typical Operating Circuit

CIRCUIT INFORMATION

RESET Output

RESET is an active low output which provides a reset signal to the microprocessor whenever the V_{CC} supply voltage is below the reset threshold. An internal timer holds RESET low for 140 ms after the voltage on V_{CC} rises above the threshold. This is intended as a power-on reset signal for the processor. It allows time for the power supply and microprocessor to stabilize after power up. Similarly a power supply brownout will initiate a processor reset. On power-down, the RESET output remains low with V_{CC} as low as 1 V. This ensures that the microprocessor is held in a stable shutdown condition as the power supply drops.

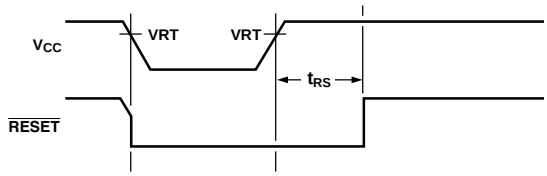


Figure 3. Power Off/On RESET Timing

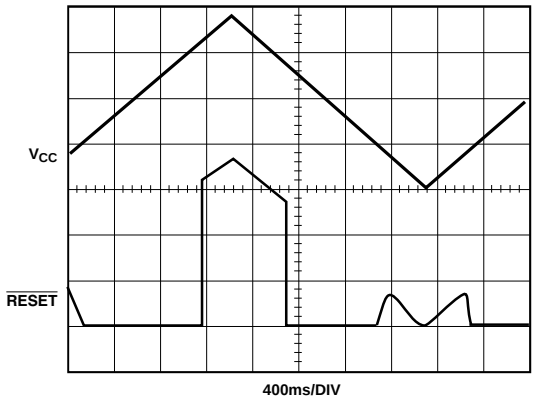


Figure 4. RESET Output vs. V_{CC}

RESET at Voltages < 1 V

The ADM709 RESET output is guaranteed to operate with supply voltages as low as 1 V. If it is desired that the RESET output remains low below 1 V, then a pull-down resistor should be connected between the RESET output and GND. A resistor of 100 kΩ is suitable. This is illustrated in Figure 5.

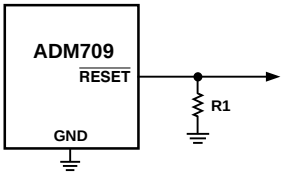


Figure 5. RESET Valid @ V_{CC} < 1 V

Glitch Immunity

The ADM709 is immune to short transient which may occur on the V_{CC} line. This is important so that spurious resets are not generated as a result of minor glitches on the power supply.

Additional glitch immunity may be obtained by connecting a capacitor (0.1 µF or greater) as close as possible to the V_{CC} pin on the device.

Microprocessors with Bidirectional I-O

Some microprocessors or microcontrollers such as the MC68HC11 have bidirectional reset lines. In order to avoid signal contention, a resistor of 4.7 kΩ should be connected between the ADM709 RESET output and the microcontroller RESET line. This arrangement is shown in Figure 6.

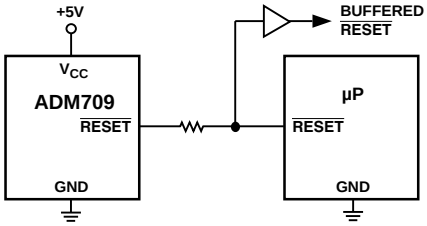
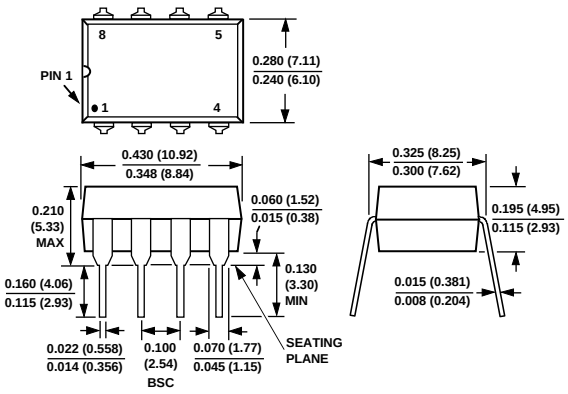


Figure 6. Interfacing to Microprocessors with Bidirectional RESET

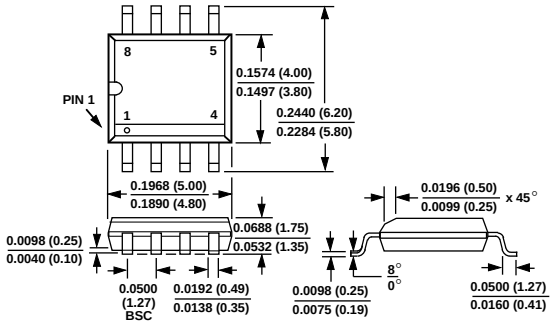
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Plastic DIP
(N-8)



8-Lead SOIC
(SO-8)



C2022–18–4/95

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