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REVISION HISTORY

10/2017—Rev. 0 to Rev. A

Changed CP-24-2 to CP-24-14 ... Throughout
Change to General Description ... 1
Change to Figure 2 and Table 3 ... 5
Updated Outline Dimensions ... 15
Changes to Ordering Guide ... 15

5/2009—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V; T_A = 25°C; M/A-COM ETC1-1-13 1:1 balun at input and output for single-ended 50 Ω match.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
GENERAL					
Usable Frequency Range		0.001		1.2	GHz
Nominal Input Impedance			50		Ω
Nominal Output Impedance			20		Ω
FREQUENCY INPUT = 100 MHz					
Gain Control Span	±3 dB gain law conformance		30		dB
Minimum Gain	V_{GAIN} = 0.1 V		−14		dB
Maximum Gain	V_{GAIN} = 1.4 V		17		dB
Gain Flatness vs. Frequency	±30 MHz around center frequency, V_{GAIN} = 1.0 V (differential output)		0.09		dB
Gain Control Slope			40		mV/dB
Gain Control Intercept	Gain = 0 dB, gain = slope (V_{GAIN} − intercept)		700		mV
Output IP3	V_{GAIN} = 1.4 V, input −13 dBm per tone, two tone measurement		47		dBm
Output Noise Floor	V_{GAIN} = 1.4 V		−149		dBm/Hz
Noise Figure	V_{GAIN} = 1.4 V		9		dB
FREQUENCY INPUT = 400 MHz					
Gain Control Span	±3 dB gain law conformance		30		dB
Minimum Gain	V_{GAIN} = 0.1 V		−15		dB
Maximum Gain	V_{GAIN} = 1.4 V		15		dB
Gain Flatness vs. Frequency	±30 MHz around center frequency, V_{GAIN} = 1.0 V (differential output)		0.09		dB
Gain Control Slope			39.5		mV/dB
Gain Control Intercept	Gain = 0 dB, gain = slope (V_{GAIN} − intercept)		730		mV
Output IP3	V_{GAIN} = 1.4 V, input −13 dBm per tone, two tone measurement		39		dBm
Output Noise Floor	20 MHz carrier offset, V_{GAIN} = 1.4 V		−150		dBm/Hz
Noise Figure	V_{GAIN} = 1.4 V		9		dB
FREQUENCY INPUT = 900 MHz					
Gain Control Span	±3 dB gain law conformance		35		dB
Minimum Gain	V_{GAIN} = 0.1 V		−18		dB
Maximum Gain	V_{GAIN} = 1.4 V		15		dB
Gain Flatness vs. Frequency	±30 MHz around center frequency, V_{GAIN} = 1.0 V (differential output)		0.09		dB
Gain Control Slope			37		mV/dB
Gain Control Intercept	Gain = 0 dB, gain = slope (V_{GAIN} − intercept)		800		mV
Third-Order Harmonic	−8 dBm output at 900 MHz fundamental		−75		dBc
Output IP3	V_{GAIN} = 1.4 V, input −13 dBm per tone, two tone measurement		32		dBm
Output Noise Floor	20 MHz carrier offset, V_{GAIN} = 1.4 V		−150		dBm/Hz
Noise Figure	V_{GAIN} = 1.4 V		9		dB
GAIN CONTROL INPUT	Pin GAIN				
Gain Control Voltage Range[1]		0.1		1.4	V
Incremental Input Resistance	Pin GAIN to Pin COM1		1		MΩ
Response Time	Full scale, to within 1 dB of final gain		380		ns
	3 dB gain step, P_{OUT} to within 1 dB of final gain		20		ns
POWER SUPPLIES	Pin VPS1, Pin VPS2, Pin COM1, Pin COM2, Pin ENBL				
Voltage		4.75	5	5.25	V
Current, Nominal Active			240		mA
ENBL, Logic 1, Device Enabled		2.3			V
ENBL, Logic 0, Device Disabled				0.8	V
Current, Disabled	ENBL = Logic 0		250		µA

[1] Minimum gain voltage varies with frequency (see Figure 3, Figure 4, and Figure 5).

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage VPS1	5.5 V
Supply Voltage VPS2	5.5 V
VPS2 to VPS1	±200 mV
RF Input Power	5 dBm at 50 Ω
OPHI, OPLO	5.5 V
ENBL	VPS1
GAIN	VPS1
Internal Power Dissipation	1.2 W
θ_{JA} (with Pad Soldered to Board)	56.1°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

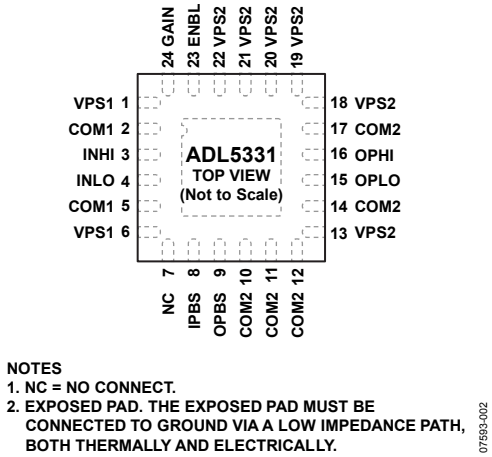


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 6	VPS1	Positive Supply. Nominally equal to 5 V.
2, 5	COM1	Common for the Input Stage.
3, 4	INHI, INLO	Differential Inputs, AC-Coupled.
7	NC	No Connect.
8	IPBS	Input Bias. Normally ac-coupled to VPS1. A 10 nF capacitor is recommended.
9	OPBS	Output Bias. Internally compensated, do not connect externally.
10 to 12, 14, 17	COM2	Common for the Output Stage.
13, 18 to 22	VPS2	Positive Supply. Nominally equal to 5 V.
15, 16	OPLO, OPHI	Differential Outputs. Bias to VPOS with RF chokes.
23	ENBL	Device Enable. Apply logic high for normal operation.
24	GAIN	Gain Control Voltage Input. Nominal range is 0 V to 1.4 V.
	EPAD	Exposed Pad. Exposed pad must be connected to via a low impedance path, both thermally and electrically.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V; T_A = 25°C; M/A-COM ETC1-1-13 1:1 balun at input and output for single-ended 50 Ω match.

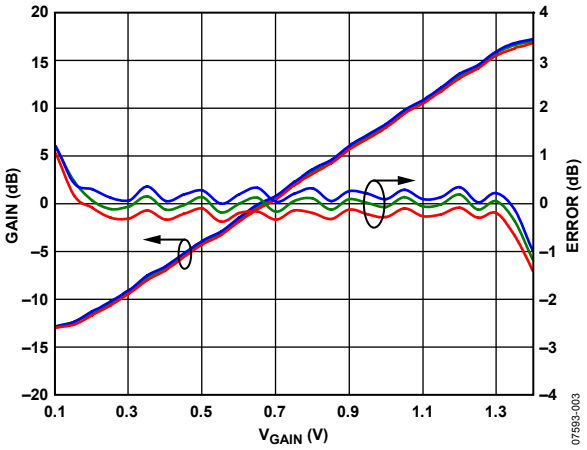


Figure 3. Gain and Gain Law Conformance vs. V_{GAIN} over Temperature at 100 MHz

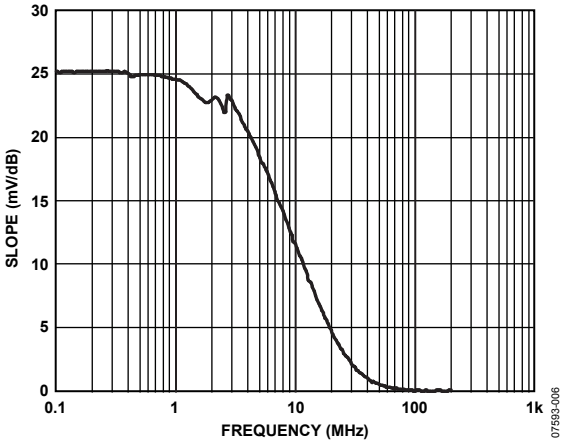


Figure 6. Gain Slope vs. Frequency, RFIN = −20 dBm @ 500 MHz, V_{GAIN} = 1 V

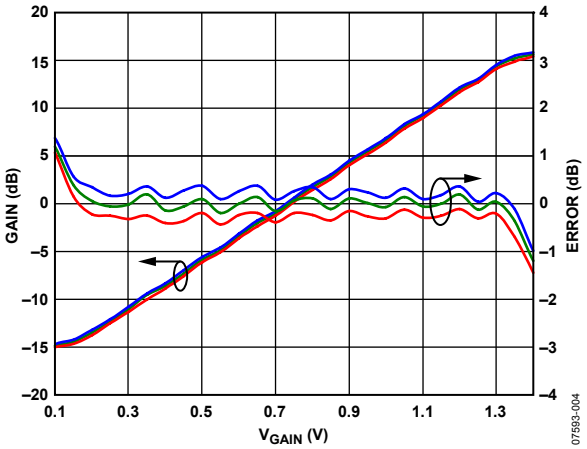


Figure 4. Gain and Gain Law Conformance vs. V_{GAIN} over Temperature at 400 MHz

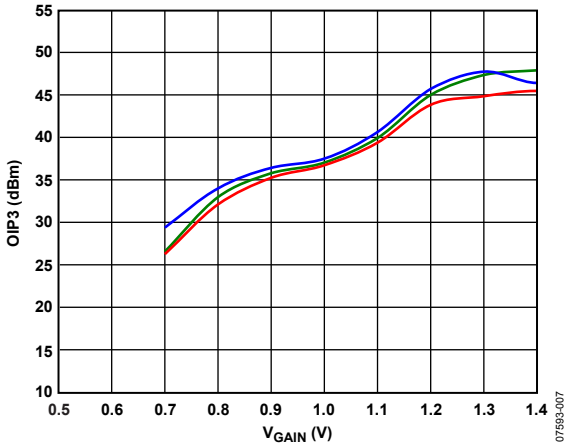


Figure 7. Output IP3 vs. V_{GAIN} at 100 MHz

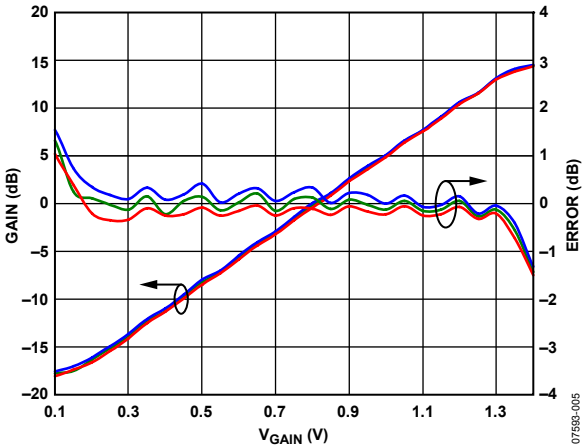


Figure 5. Gain and Gain Law Conformance vs. V_{GAIN} over Temperature at 900 MHz

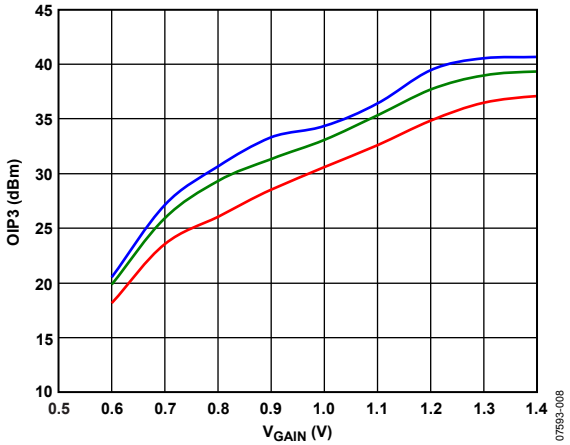


Figure 8. Output IP3 vs. V_{GAIN} at 400 MHz

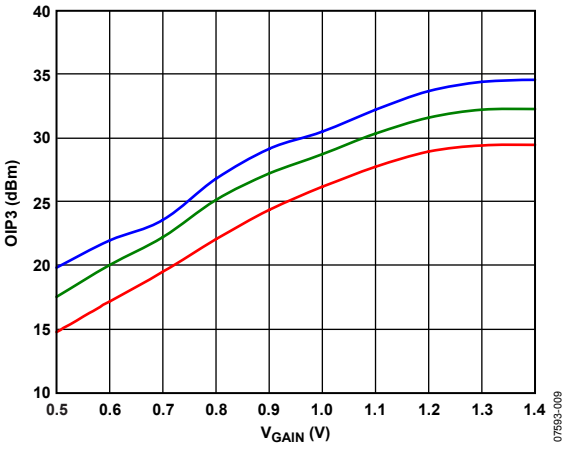


Figure 9. Output IP3 vs. V_{GAIN} at 900 MHz

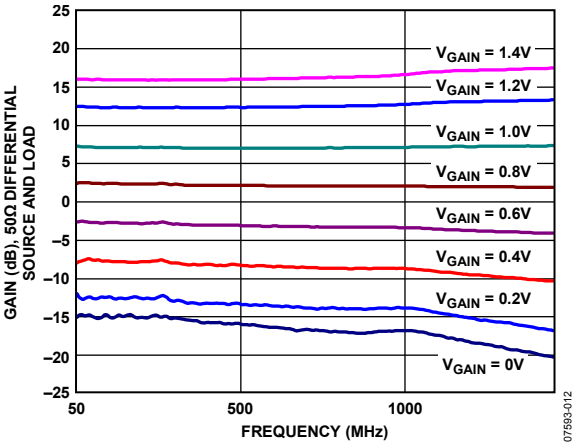


Figure 12. Gain vs. Frequency (Differential 100 Ω Output Load)

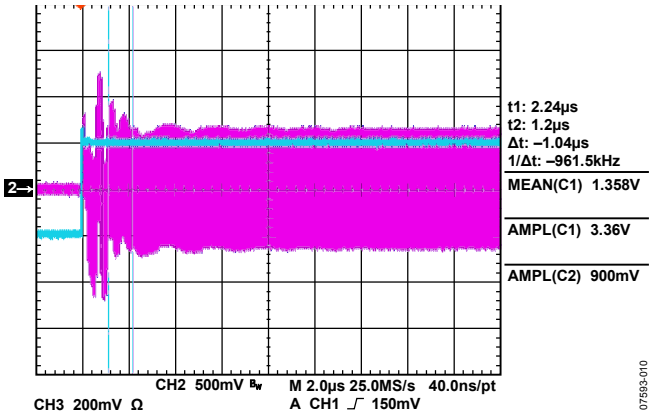


Figure 10. Step Response of Gain Control Input

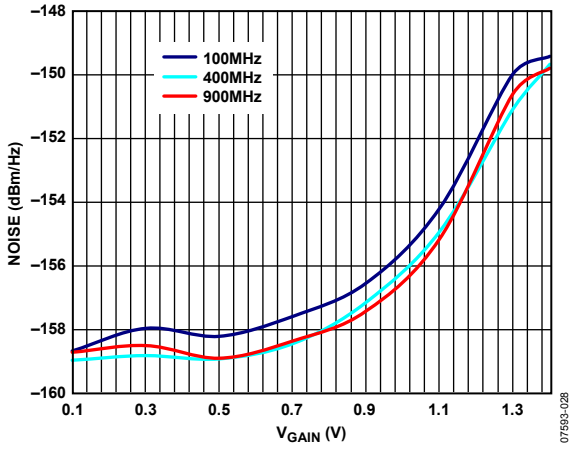


Figure 13. Output Noise Spectral Density vs. V_{GAIN}

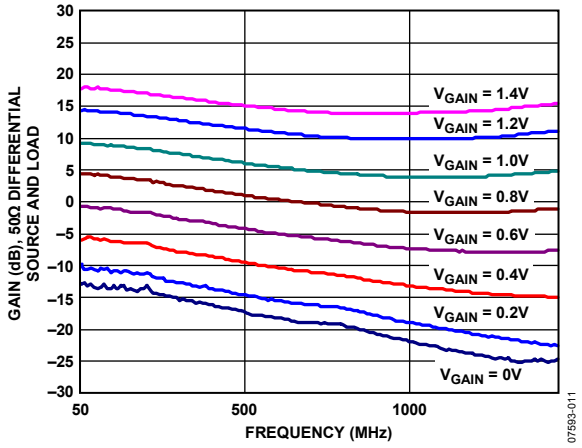


Figure 11. Gain vs. Frequency (Differential 50 Ω Output Load)

THEORY OF OPERATION

The ADL5331 is a high performance, voltage-controlled variable gain amplifier/attenuator for use in applications with frequencies up to 1.2 GHz. This device is intended to serve as an output variable gain amplifier (OVGA) for applications where a reasonably constant input level is available and the output level adjusts over a wide range. One aspect of an OVGA is that the output metrics, OIP3 and OP1dB, decrease with decreasing gain.

The signal path is fully differential throughout the device to provide the usual benefits of differential signaling, including reduced radiation, reduced parasitic feedthrough, and reduced susceptibility to common-mode interference with other circuits. Figure 14 provides a simplified schematic of the ADL5331.

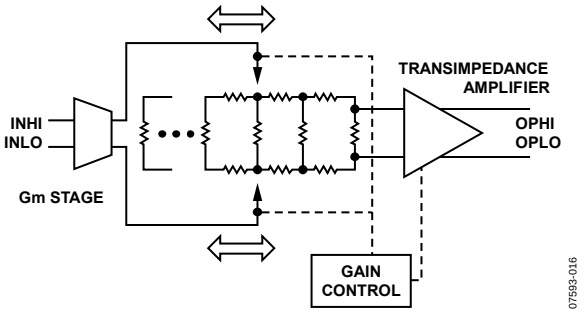


Figure 14. Simplified Schematic

A controlled input impedance of 50 Ω is achieved through a combination of passive and active (feedback-derived) termination techniques in an input Gm stage.

Note that the inputs of the Gm stage are internally biased to a dc level and dc blocking capacitors are generally needed on the inputs to avoid upsetting the operation of the device.

The currents from the Gm stage are then injected into a balanced ladder attenuator at a deliberately diffused location along the ladder, wherein the location of the centroid of the injection region is dependent on the applied gain control voltage. The steering of the current injection into the ladder is accomplished by proprietary means to achieve linear-in-dB gain control and low distortion.

Linear-in-dB gain control is accomplished by the application of a voltage in the range of 0 V dc to 1.4 V dc to the gain control pin, with maximum gain occurring at the highest voltage.

The output of the ladder attenuator is passed into a fixed-gain transimpedance amplifier (TZA) to provide gain and to buffer the ladder terminating impedance from load variations. The TZA uses feedback to improve linearity and to provide controlled 50 Ω differential output impedance. The quiescent current of the output amplifier is adaptive; it is controlled by an output level detector, which biases the output stage for signal levels above a threshold.

The outputs of the ADL5331 require external dc bias to the positive supply voltage. This bias is typically supplied through external inductors. The outputs are best taken differentially to avoid any common-mode noise that is present, but, if necessary, can be taken single-ended from either output.

The output impedance is 20 Ω differential and can drive a range of impedances from <20 Ω to >75 Ω. Back series terminations can be used to pad the output impedance to a desired level.

If only a single output is used, it is still necessary to provide a bias to the unused output pin and it is advisable to arrange a reasonably equivalent ac load on the unused output. Differential output can be taken via a 1:1 balun into a 50 Ω environment. In virtually all cases, it is necessary to use dc blocking in the output signal path.

At high gain settings, the noise floor is set by the input stage, in which case the noise figure (NF) of the device is essentially independent of the gain setting. Below a certain gain setting, however, the input stage noise that reaches the output of the attenuator falls below the input-equivalent noise of the output stage. In such a case, the output noise is dominated by the output stage itself; therefore, the overall NF of the device gets worse on a dB-per-dB basis as the gain is lowered, because the gain is reduced below the critical value. Figure 7 through Figure 9 provide details of this behavior.

APPLICATIONS INFORMATION

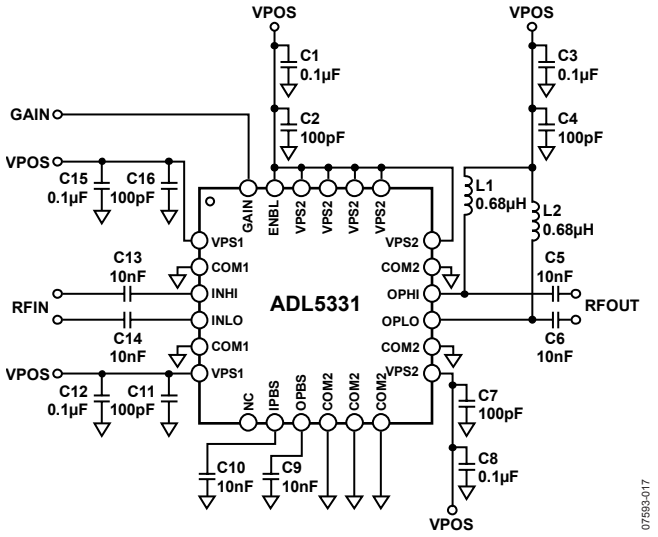


Figure 15. Basic Connections

BASIC CONNECTIONS

Figure 15 shows the basic connections for operating the ADL5331. There are two positive supplies, VPS1 and VPS2, which must be connected to the same potential. Connect COM1 and COM2 (common pins) to a low impedance ground plane.

Apply a power supply voltage between 4.75 V and 5.25 V to VPS1 and VPS2. Connect decoupling capacitors with 100 pF and 0.1 µF power supplies close to each power supply pin. The VPS2 pins (Pins 13 and Pin 18 through Pin 22) can share a pair of decoupling capacitors because of their proximity to each other.

The outputs of the ADL5331, OPHI and OPLO, are open collectors that need to be pulled up to the positive supply with 120 nH RF chokes. The ac-coupling capacitors and the RF chokes are the principle limitations for operation at low frequencies. For example, to operate down to 1 MHz, use 0.1 µF ac coupling capacitors and 1.5 µH RF chokes. Note that in some circumstances, the use of substantially larger inductor values results in oscillations.

Because the differential outputs are biased to the positive supply, ac-coupling capacitors (preferably 100 pF) are needed between the ADL5331 outputs and the next stage in the system. Similarly, the INHI and INLO input pins are at bias voltages of about 3.3 V above ground.

The nominal input and output impedance looking into each individual RF input/output pin is 25 Ω. Consequently, the differential impedance is 50 Ω.

To enable the ADL5331, the ENBL pin must be pulled high. Taking ENBL low puts the ADL5331 in sleep mode, reducing current consumption to 250 µA at an ambient temperature. The voltage on ENBL must be greater than 1.7 V to enable the device. When enabled, the device draws 100 mA at low gain to 215 mA at maximum gain.

The ADL5331 is primarily designed for differential signals; however, there are several configurations that can be implemented to interface the ADL5331 to single-ended applications. Figure 16 and Figure 17 show options for differential-to-single-ended interfaces. Both configurations use ac-coupling capacitors at the input/output and RF chokes at the output.

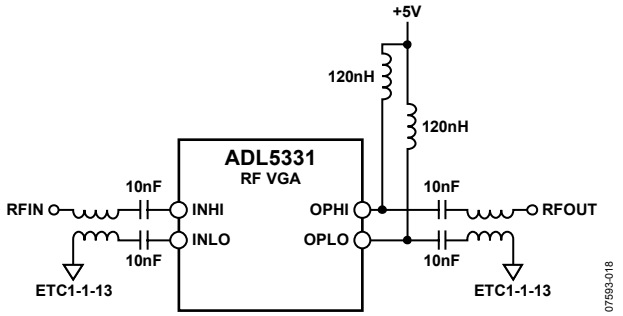


Figure 16. Differential Operation with Balun Transformers

Figure 16 illustrates differential balance at the input and output using a transformer balun. Input and output baluns are recommended for optimal performance. Much of the characterization for the ADL5331 was completed using 1:1 baluns at the input and output for a single-ended 50 Ω match. Operation using M/A-COM ETC1-1-13 transmission line transformer baluns is recommended for a broadband interface; however, narrowband baluns can be used for applications requiring lower insertion loss over smaller bandwidths.

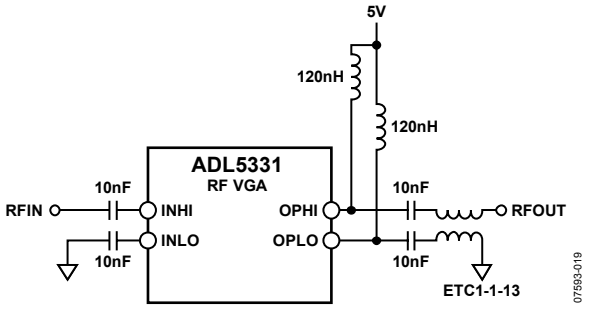


Figure 17. Single-Ended Drive with Balanced Output

The device can be driven single-ended with similar performance, as shown in Figure 17. The single-ended input interface can be implemented by driving one of the input terminals and terminating the unused input to ground. To achieve the optimal performance, the output must remain balanced. In the case of Figure 17, a transformer balun is used at the output.

GAIN CONTROL INPUT

When the VGA is enabled, the voltage applied to the GAIN pin sets the gain. The input impedance of the GAIN pin is 1 MΩ.

The gain control voltage range is between 0.1 V and 1.4 V, which corresponds to a typical gain range between −15 dB and +15 dB.

The 1 dB input compression point remains constant at 3 dBm through the majority of the gain control range, as shown in Figure 7 through Figure 9. The output compression point increases decibel for decibel with increasing gain setting. The noise floor is constant up to V_{GAIN} = 1 V where it begins to rise.

The bandwidth on the gain control pin is approximately 3 MHz. Figure 10 shows the response time of a pulse on the V_{GAIN} pin.

Although the ADL5331 provides accurate gain control, precise regulation of output power can be achieved with an automatic gain control (AGC) loop. Figure 18 shows the ADL5331 in an AGC loop. The addition of a log amp or a TruPwr™ detector (such as the AD8362) allows the AGC to have improved temperature stability over a wide output power control range.

Note that the ADL5331, because of its positive gain slope, in an AGC application requires a detector with a negative V_{OUT}/RF_{IN} slope. As an example, the AD8319 in the example in Figure 19 has a negative slope. The AD8362 rms detector, however, has a positive slope. Extra circuitry is necessary to compensate for this.

To operate the ADL5331 in an AGC loop, a sample of the output RF must be fed back to the detector (typically using a directional coupler and additional attenuation). A setpoint voltage is applied to the VSET input of the detector while VOUT is connected to the GAIN pin of the ADL5331. Based on the detector's defined linear-in-dB relationship between VOUT and the RFIN signal, the detector adjusts the voltage on the GAIN pin (the detector's VOUT pin is an error amplifier output) until the level at the RF input corresponds to the applied setpoint voltage. The V_{GAIN} setting settles to a value that results in the correct balance between the input signal level at the detector and the setpoint voltage.

The detector's error amplifier uses CLPF, a ground-referenced capacitor pin, to integrate the error signal (in the form of a current). A capacitor must be connected to CLPF to set the loop bandwidth and to ensure loop stability.

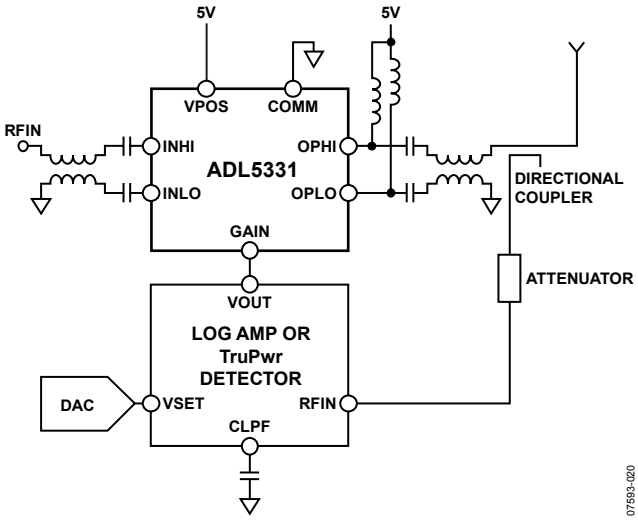


Figure 18. ADL5331 in AGC Loop

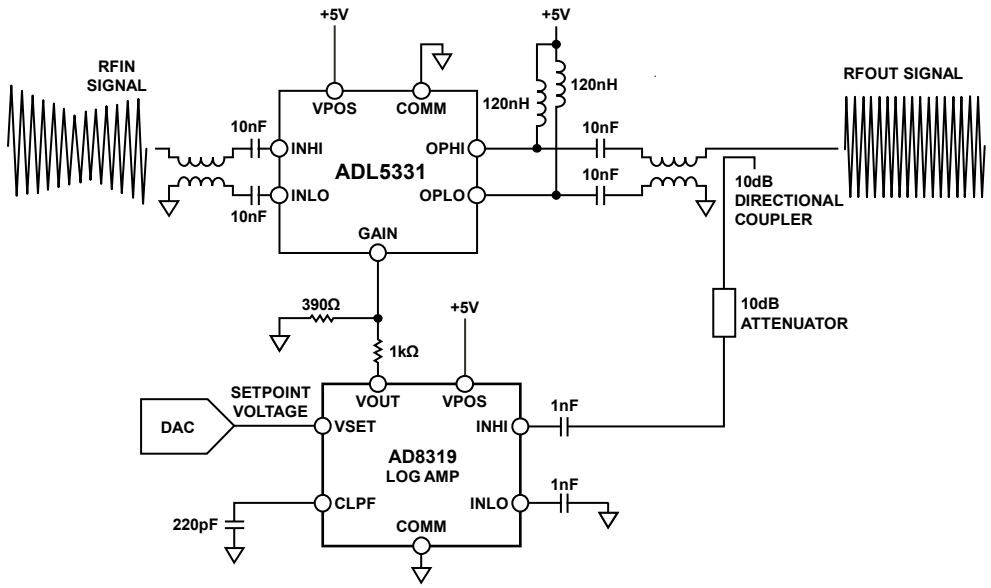


Figure 19. AD8319 Operating in Controller Mode to Provide Automatic Gain Control Functionality in Combination with the ADL5331

Figure 19 shows the basic connections for operating the AD8319 log detector in an automatic gain control (AGC) loop with the ADL5331.

The gain of the ADL5331 is controlled by the output pin of the AD8319. The voltage, V_{OUT}, has a range of 0 V to near V_{POS}. To avoid overdrive recovery issues, the AD8319 output voltage can be scaled down using a resistive divider to interface with the 0.1 V to 1.4 V gain control range of the ADL5331.

A coupler/attenuation of 21 dB is used to match the desired maximum output power from the VGA to the top end of the linear operating range of the AD8319 (approximately −5 dBm at 900 MHz).

Figure 20 shows the transfer function of the output power vs. the V_{SET} voltage over temperature for a 100 MHz sine wave with an input power of −1.5 dBm. Note that the power control of the AD8319 has a negative sense. Decreasing V_{SET}, which corresponds to demanding a higher signal from the ADL5331, increases gain.

This AGC loop is capable of controlling signals of ~30 dB, which is the gain range limitation on the ADL5331. Across the top 25 dB range of output power, the linear conformance error is within ±0.5 dB over temperature.

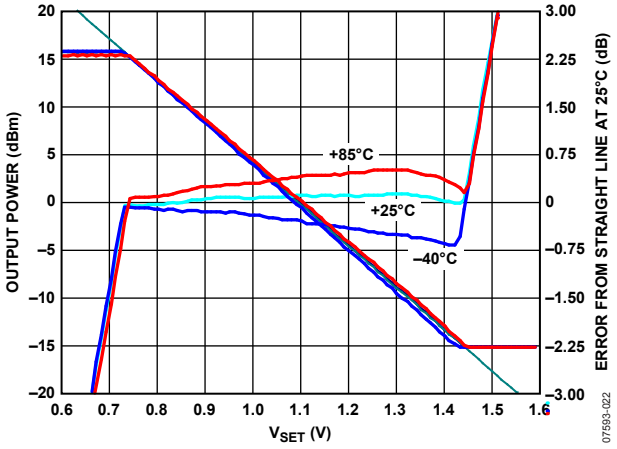


Figure 20. ADL5331 Output Power vs. AD8319 Setpoint Voltage, P_{IN} = 0 dBm at 100 MHz

For the AGC loop to remain in equilibrium, the AD8319 must track the envelope of the output signal of the ADL5331 and provide the necessary voltage levels to the gain control input of the ADL5331. Figure 21 shows an oscilloscope of the AGC loop depicted in Figure 19. A 100 MHz sine wave with 50% AM modulation is applied to the ADL5331. The output signal from the VGA is a constant envelope sine wave with amplitude corresponding to a setpoint voltage at the AD8319 of 1.3 V. The gain control response of the AD8319 to the changing input envelope is also shown in Figure 21.

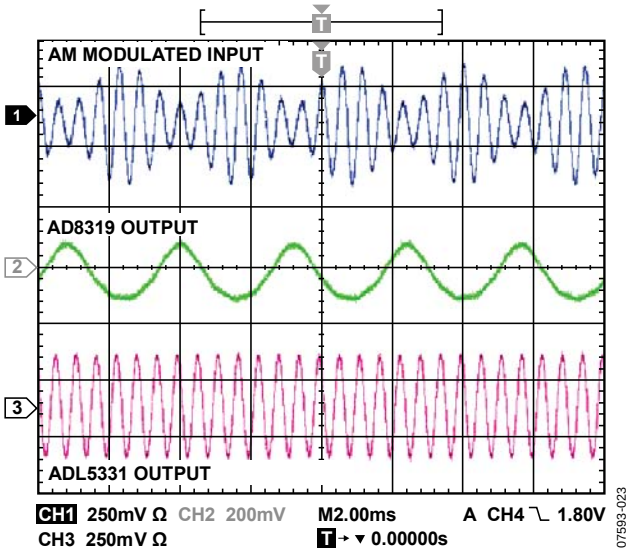


Figure 21. Oscilloscope Showing an AM Modulated Input Signal and the Response from the AD8319

Figure 22 shows the response of the AGC RF output to a pulse on VSET. As VSET decreases from 1.5 V to 0.4 V, the AGC loop responds with an RF burst. In this configuration, the input signal to the ADL5331 is a 1 GHz sine wave at a power level of −15 dBm.

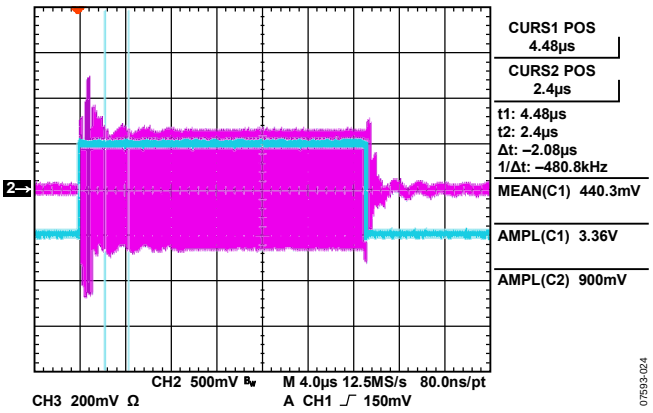


Figure 22. Oscilloscope Showing theResponse Time of the AGC Loop

Response time and the amount of signal integration are controlled by CLPF. This functionality is analogous to the feedback capacitor around an integrating amplifier. While it is possible to use large capacitors for CLPF, in most applications, values under 1 nF provide sufficient filtering.

More information on the use of AD8319 in an AGC application can be found in the AD8319 data sheet.

CMTS TRANSMIT APPLICATION

Interfacing to AD9789

Because of its broadband operating range, the ADL5331 VGA can also be used in direct-launch cable modem termination systems (CMTS) applications in the 50 MHz to 860 MHz cable band. The ADL5331 makes an excellent choice as a post-DAC VGA in a CMTS application when used with the Analog Devices AD9789 wideband DAC. The AD9789 also contains digital signal processing specifically designed to process DOCSIS type CMTS signals. A typical AD9789-to-ADL5331 interface is shown in Figure 23.

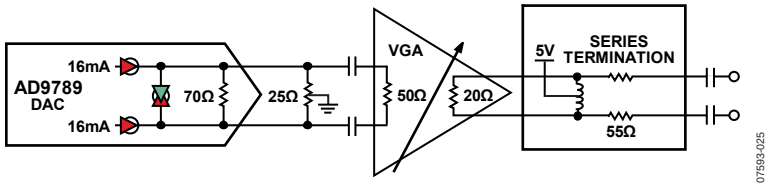


Figure 23. Block Diagram of AD9789 interface to ADL5331 in a DOCSIS Type Application

INTERFACING TO AN IQ MODULATOR

The basic connections for interfacing the ADL5331 with the ADL5385 are shown in Figure 24. The ADL5385 is an RF quadrature modulator with an output frequency range of 50 MHz to 2.2 GHz. It offers excellent phase accuracy and amplitude balance, enabling high performance direct RF modulation for communication systems.

The output of the ADL5385 is designed to drive 50 Ω loads and easily interfaces with the ADL5331. The input to the ADL5331 can be driven single-ended, as shown in Figure 17. Similar configurations are possible with the ADL537x family of quadrature modulators. These modulators can provide outputs from 500 MHz to 4 GHz.

SOLDERING INFORMATION

On the underside of the chip scale package, there is an exposed compressed paddle. This paddle is internally connected to the chip's ground. Solder the paddle to the low impedance ground plane on the printed circuit board to ensure specified electrical performance and to provide thermal relief. It is also recommended that the ground planes on all layers under the paddle be stitched together with vias to reduce thermal impedance.

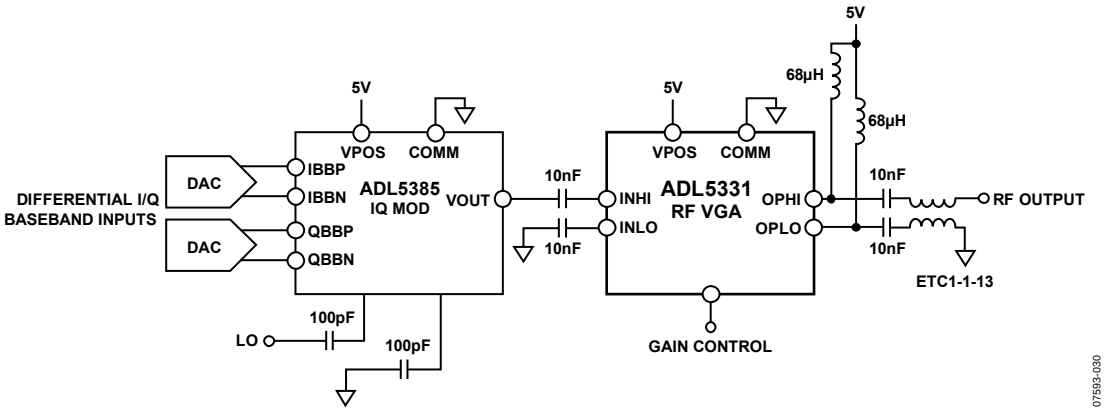


Figure 24. ADL5385 Quadrature Modulator and ADL5331 Interface

EVALUATION BOARD SCHEMATIC

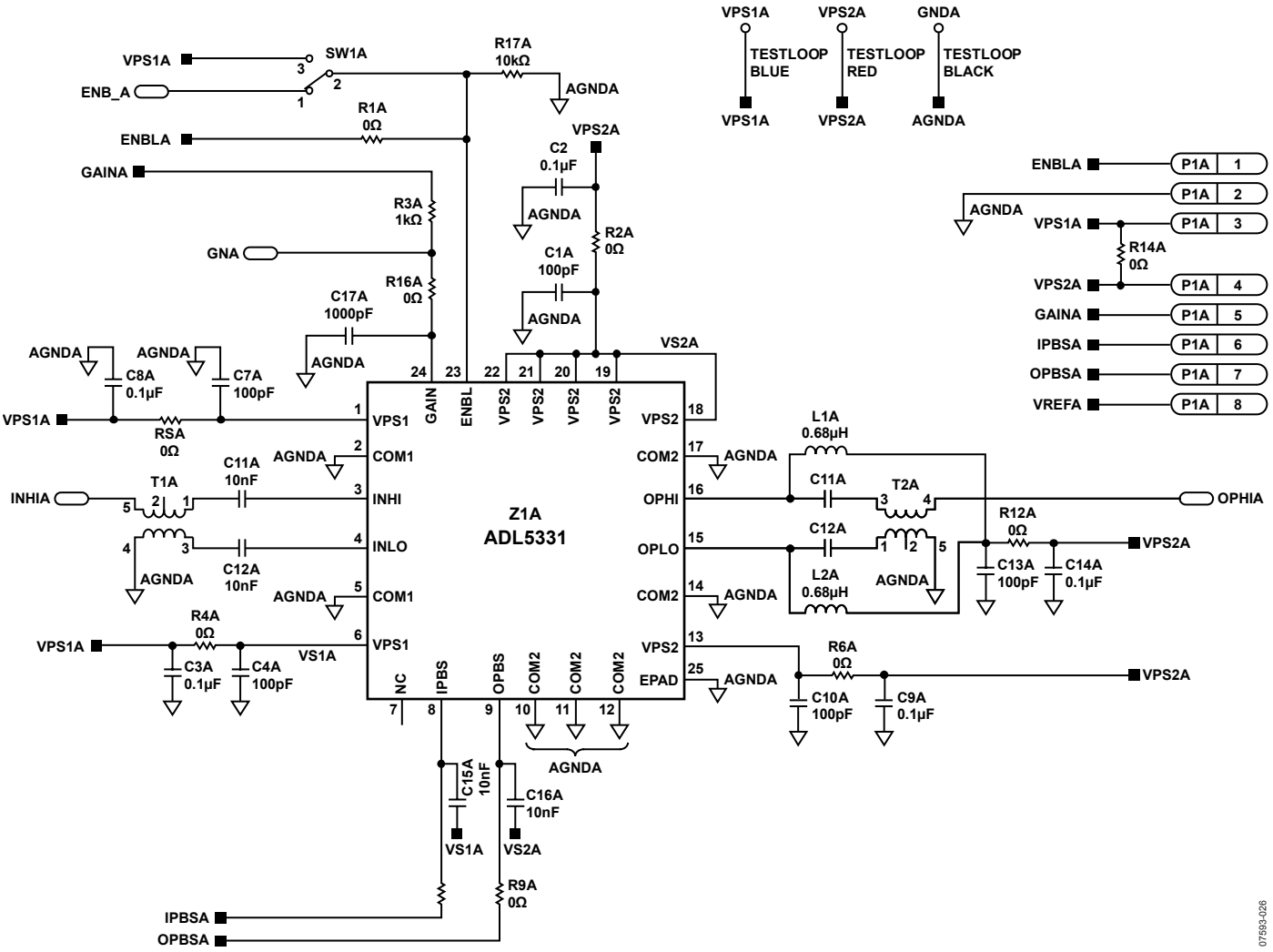
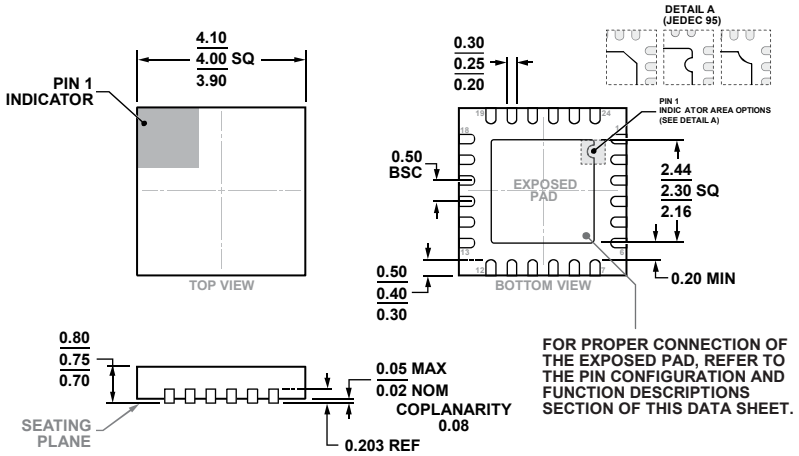


Figure 25. ADL5331 Single-Ended Input/Output Evaluation Board

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-8

Figure 26. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-24-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
ADL5331ACPZ-R7	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-14	1,500
ADL5331-EVALZ		ADL5331 Evaluation Board		

[1] Z = RoHS Compliant Part.

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