

TABLE OF CONTENTS

Features	1	ESD Caution.....	6
Applications.....	1	Pin Configurations.....	7
General Description	1	Typical Performance Characteristics	8
Revision History	2	Shutdown Operation.....	16
Specifications.....	3	Input Pin Characteristics.....	16
Electrical Characteristics—2.7 V Operation	3	Input Threshold.....	16
Electrical Characteristics—5 V Operation.....	4	Outline Dimensions	17
Absolute Maximum Ratings.....	6	Ordering Guide	19
Thermal Resistance	6		

REVISION HISTORY

12/2019—Rev. D to Rev. E

Changes to Table 1	1
Changes to Table 2.....	3
Changes to Table 3.....	5
Updated Outline Dimensions	17
Changes to Ordering Guide	19

11/2010—Rev. C to Rev. D

Changed 5 V to 6 V in Endnote 2, Table 4	6
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12/2009—Rev. B to Rev. C

Added ADA4691-4, 16-Lead LFCSP	Throughout
Added Figure 1, Figure 2, and Table 1; Renumbered Sequentially	1
Changes to Applications Section and General Description Section.....	1
Changes to Table 1.....	3
Changes to Table 2.....	4
Changes to Table 4.....	6
Updated Outline Dimensions	17
Changes to Ordering Guide	20

9/2009—Rev. A to Rev. B

Added ADA4691-2, 9-Ball WLCSP; ADA4692-2, 8-Lead LFCSP; and ADA4692-4, 14-Lead TSSOP.....	Throughout
Changes to General Description	1
Updated Outline Dimensions.....	16
Changes to Ordering Guide	17

6/2009—Rev. 0 to Rev. A

Added ADA4691-2, 10 Lead LFCSP	Throughout
Changes to Table 1.....	3
Changes to Table 2.....	4
Changes to Captions for Figure 40, Figure 41, Figure 43, and Figure 44	13
Added Shutdown Operations Section	15
Updated Outline Dimensions.....	16
Changes to Ordering Guide	16

3/2009—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—2.7 V OPERATION

Supply voltage (V_{SY}) = 2.7 V, common-mode voltage (V_{CM}) = $V_{SY}/2$, T_A = 25°C, unless otherwise specified.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = -0.3 \text{ V to } +1.6 \text{ V}$		0.5	2.5	mV
Dual (ADA469x-2)		$V_{CM} = -0.1 \text{ V to } +1.6 \text{ V}; -40^\circ\text{C} < T_A < +125^\circ\text{C}$			3.5	mV
Quad (ADA469x-4)		$V_{CM} = -0.1 \text{ V to } +1.6 \text{ V}; -40^\circ\text{C} < T_A < +125^\circ\text{C}$			4.0	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1	4	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_B	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.5	5	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			360	pA
Input Voltage Range		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-0.3		+1.6	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -0.3 \text{ V to } +1.6 \text{ V}$	70	90		dB
		$V_{CM} = -0.1 \text{ V to } +1.6 \text{ V}; -40^\circ\text{C} < T_A < +125^\circ\text{C}$	62			dB
Large Signal Voltage Gain	A_{VO}	Load resistance (R_L) = 2 k Ω , output voltage (V_{OUT}) = 0.5 V to 2.2 V	90	100		dB
		$-40^\circ\text{C} < T_A < +85^\circ\text{C}$	80			dB
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	63			dB
		$R_L = 600 \Omega$, $V_{OUT} = 0.5 \text{ V to } 2.2 \text{ V}$	85	95		dB
Input Capacitance	C_{IN}					
Differential Mode	C_{INDM}			2.5		pF
Common Mode	C_{INCM}			7		pF
Logic High Voltage (Enabled)	V_{IH}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	1.6			V
Logic Low Voltage (Power-Down)	V_{IL}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			0.5	V
Logic Input Current (Per Pin)	I_{IN}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$, 0 V $\leq$ shutdown voltage (V_{SD}) $\leq$ 2.7 V			1	μA
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 2 \text{ k}\Omega \text{ to } V_{CM}$	2.65	2.67		V
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	2.6			V
		$R_L = 600 \Omega \text{ to } V_{CM}$	2.55	2.59		V
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	2.5			V
Output Voltage Low	V_{OL}	$R_L = 2 \text{ k}\Omega \text{ to } V_{CM}$		24	33	mV
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			43	mV
		$R_L = 600 \Omega \text{ to } V_{CM}$		78	103	mV
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			138	mV
Short-Circuit Current	I_{SC}	$V_{OUT} = V_{SY} \text{ or GND}$		± 15		mA
Closed-Loop Output Impedance	Z_{OUT}	Frequency (f) = 1 MHz, voltage gain (A_v) = -100		372		Ω
Output Pin Leakage Current		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$, shutdown active, $V_{SD} =$ negative supply voltage (V_{SS})		10		nA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_{SY} = 2.7 \text{ V to } 5.5 \text{ V}$	80	90		dB
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	75			dB
Supply Current Per Amplifier	I_{SY}	$V_{OUT} = V_{SY}/2$		165	200	μA
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			240	μA
Supply Current Shutdown Mode	I_{SD}	All amplifiers shut down, $V_{SD} = V_{SS}$		10		nA
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			2	μA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 600\ \Omega$, load capacitance (C_L) = 20 pF, $A_v = +1$		1.1		V/ μ s
		$R_L = 2\ \text{k}\Omega$, $C_L = 20\ \text{pF}$, $A_v = +1$		1.4		V/ μ s
Settling Time to 0.1%	t_s	Step = 0.5 V, $R_L = 2\ \text{k}\Omega$, 600 Ω		1		μ s
Gain Bandwidth Product	GBP	$R_L = 1\ \text{M}\Omega$, $C_L = 35\ \text{pF}$, $A_v = +1$		3.6		MHz
Phase Margin	Φ_M	$R_L = 1\ \text{M}\Omega$, $C_L = 35\ \text{pF}$, $A_v = +1$		49		Degrees
Turn-On/Turn-Off Time		$R_L = 600\ \Omega$		1		μ s
NOISE PERFORMANCE						
Distortion	THD + N	$A_v = -1$, $R_L = 2\ \text{k}\Omega$, $f = 1\ \text{kHz}$, input voltage (V_{IN}) rms = 0.15 V rms		0.009		%
		$A_v = -1$, $R_L = 600\ \Omega$, $f = 1\ \text{kHz}$, V_{IN} rms = 0.15 V rms		0.01		%
		$A_v = +1$, $R_L = 2\ \text{k}\Omega$, $f = 1\ \text{kHz}$, V_{IN} rms = 0.15 V rms		0.006		%
		$A_v = +1$, $R_L = 600\ \Omega$, $f = 1\ \text{kHz}$, V_{IN} rms = 0.15 V rms		0.009		%
Voltage Noise	e_n p-p	$f = 0.1\ \text{Hz}$ to 10 Hz		3.1		μ V p-p
Voltage Noise Density	e_n	$f = 1\ \text{kHz}$		16		nV/ $\sqrt{\text{Hz}}$
		$f = 10\ \text{kHz}$		13		nV/ $\sqrt{\text{Hz}}$

ELECTRICAL CHARACTERISTICS—5 V OPERATION

$V_{SY} = 5\ \text{V}$, $V_{CM} = V_{SY}/2$, $T_A = 25^\circ\text{C}$, unless otherwise specified.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = -0.3\ \text{V}$ to $+3.9\ \text{V}$		0.5	2.5	mV
Dual (ADA469x-2)		$V_{CM} = -0.1\ \text{V}$ to $+3.9\ \text{V}$; $-40^\circ\text{C} < T_A < +125^\circ\text{C}$			3.5	mV
Quad (ADA469x-4)		$V_{CM} = -0.1\ \text{V}$ to $+3.9\ \text{V}$; $-40^\circ\text{C} < T_A < +125^\circ\text{C}$			4.0	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1	4	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_B	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.5	5	pA
					360	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1	8	pA
					260	pA
Input Voltage Range		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-0.3		+3.9	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -0.3\ \text{V}$ to $+3.9\ \text{V}$	75	98		dB
		$V_{CM} = -0.1\ \text{V}$ to $+3.9\ \text{V}$; $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	68			dB
Large Signal Voltage Gain	A_{VO}	$R_L = 2\ \text{k}\Omega$, $V_{OUT} = 0.5\ \text{V}$ to $4.5\ \text{V}$, $V_{CM} = 0\ \text{V}$	95	110		dB
		$-40^\circ\text{C} < T_A < +85^\circ\text{C}$	80			dB
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	70			dB
		$R_L = 600\ \Omega$, $V_{OUT} = 0.5\ \text{V}$ to $4.5\ \text{V}$, $V_{CM} = 0\ \text{V}$	90	100		dB
Input Capacitance						
Differential Mode	C_{INDM}			2.5		pF
Common Mode	C_{INCM}			7		pF
Logic High Voltage (Enabled)	V_{IH}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	2.0			V
Logic Low Voltage (Power-Down)	V_{IL}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			0.8	V
Logic Input Current (Per Pin)	I_{IN}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$, $0\ \text{V} \leq V_{SD} \leq 2.7\ \text{V}$			1	μA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS						
Output Voltage High	V _{OH}	R _L = 2 kΩ to V _{CM} −40°C ≤ T _A ≤ +125°C	4.95	4.97		V
			4.90			V
		R _L = 600 Ω to V _{CM} −40°C ≤ T _A ≤ +125°C	4.85	4.88		V
			4.80			V
Output Voltage Low	V _{OL}	R _L = 2 kΩ to V _{CM} −40°C ≤ T _A ≤ +125°C		30	40	mV
					55	mV
		R _L = 600 Ω to V _{CM} −40°C ≤ T _A ≤ +125°C		100	128	mV
					173	mV
Short-Circuit Limit	I _{SC}	V _{OUT} = V _{SY} or GND		±55		mA
Closed-Loop Output Impedance	Z _{OUT}	ADA4691-2, f = 1 MHz, A _V = −100		364		Ω
		ADA4691-2, f = 1 MHz, A _V = −100		246		Ω
Output Pin Leakage Current		−40°C < T _A < +125°C, shutdown active, V _{SD} = V _{SS}		10		nA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V _{SY} = 2.7 V to 5.5 V −40°C ≤ T _A ≤ +125°C	80	90		dB
			75			dB
Supply Current Per Amplifier	I _{SY}	V _{OUT} = V _{SY} /2 −40°C ≤ T _A ≤ +125°C		180	225	μA
					275	μA
Supply Current Shutdown Mode	I _{SD}	All amplifiers shut down, V _{SD} = V _{SS} −40°C ≤ T _A ≤ +125°C		10		nA
					2	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R _L = 2 kΩ, 600 Ω, C _L = 20 pF, A _V = +1		1.3		V/μs
Settling Time to 0.1%	t _S	V _{IN} = 2 V step, R _L = 2 kΩ or 600 Ω		1.5		μs
Gain Bandwidth Product	GBP	R _L = 1 MΩ, C _L = 35 pF, A _V = +1		3.6		MHz
Phase Margin	Φ _M	R _L = 1 MΩ, C _L = 35 pF, A _V = +1		52		Degrees
Turn-On/Turn-Off Time		R _L = 600 Ω		1		μs
NOISE PERFORMANCE						
Distortion	THD + N	A _V = −1, R _L = 2 kΩ, f = 1 kHz, V _{IN rms} = 0.8 V rms		0.006		%
		A _V = −1, R _L = 600 Ω, f = 1 kHz, V _{IN rms} = 0.8 V rms		0.008		%
		A _V = +1, R _L = 2 kΩ, f = 1 kHz, V _{IN rms} = 0.8 V rms		0.001		%
		A _V = +1, R _L = 600 Ω, f = 1 kHz, V _{IN rms} = 0.8 V rms		0.003		%
Voltage Noise	e _n p-p	f = 0.1 Hz to 10 Hz		3.2		μV p-p
Voltage Noise Density	e _n	f = 1 kHz		16		nV/√Hz
	e _n	f = 10 kHz		13		nV/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	$V_{SS} - 0.3 \text{ V}$ to $V_{DD} + 0.3 \text{ V}$
Input Current ¹	$\pm 10 \text{ mA}$
Shutdown Pin Rise/Fall Times	50 μs maximum
Differential Input Voltage ²	$\pm V_{SY}$
Output Short-Circuit Duration to GND	Indefinite
Temperature	
Storage Temperature Range	-65°C to $+150^{\circ}\text{C}$
Operating Temperature Range	-40°C to $+125^{\circ}\text{C}$
Junction Temperature Range	-65°C to $+150^{\circ}\text{C}$
Lead Temperature (Soldering, 60 sec)	300°C

¹ Input pins have clamp diodes to the supply pins. Limit the input current to 10 mA or less whenever the input signal exceeds the power supply rail by 0.3 V.

² Differential input voltage is limited to 6 V or the supply voltage, whichever is less.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages and measured using a standard 4-layer board, unless otherwise specified.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC_N (R-8)	120	45	$^{\circ}\text{C/W}$
8-Lead LFCSP (CP-8-6)	125	40	$^{\circ}\text{C/W}$
9-Ball WLCSP (CB-9-3)	77	N/A ¹	$^{\circ}\text{C/W}$
10-Lead LFCSP (CP-10-11)	115	40	$^{\circ}\text{C/W}$
16-Lead LFCSP (CP-16-22)	75	12	$^{\circ}\text{C/W}$
14-Lead TSSOP (RU-14)	112	35	$^{\circ}\text{C/W}$

¹ N/A = not applicable.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS

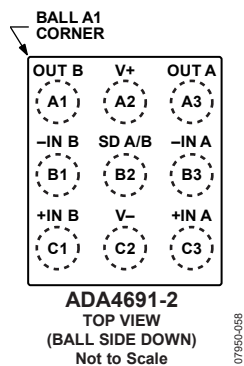


Figure 3. 9-Ball Wafer Level Chip Scale WLCSP (CB-9-3)

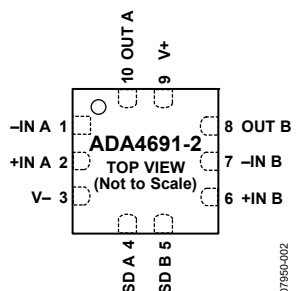
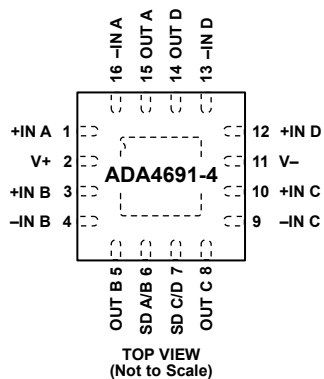


Figure 4. 10-Lead, 2 mm x 2 mm LFCSP (CP-10-11)



NOTES

1. IT IS RECOMMENDED THAT THE EXPOSED PAD BE CONNECTED TO V-.

Figure 5. 16-Lead, 3 mm x 3 mm LFCSP (CP-16-22)

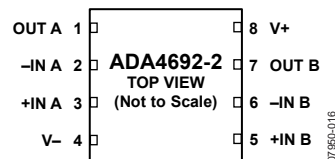


Figure 6. 8-Lead, 2 mm x 2 mm LFCSP (CP-8-6)

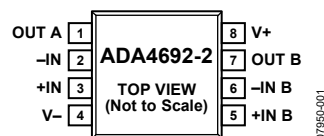


Figure 7. 8-Lead SOIC_N (R-8)

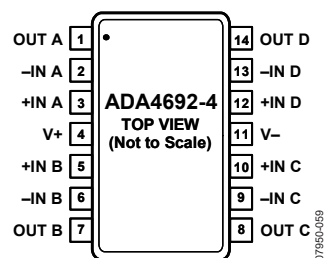


Figure 8. 14-Lead TSSOP (RU-14)

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

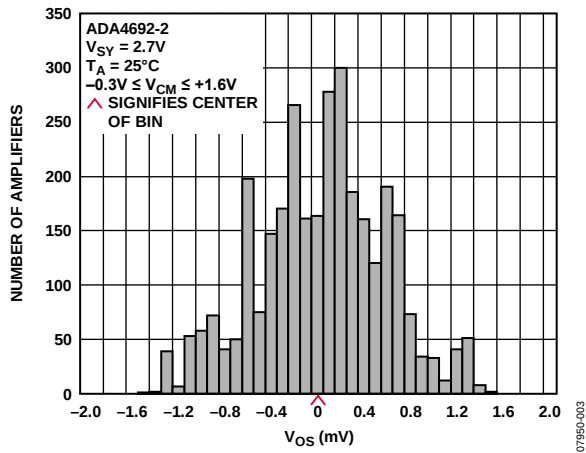


Figure 9. Input Offset Voltage Distribution

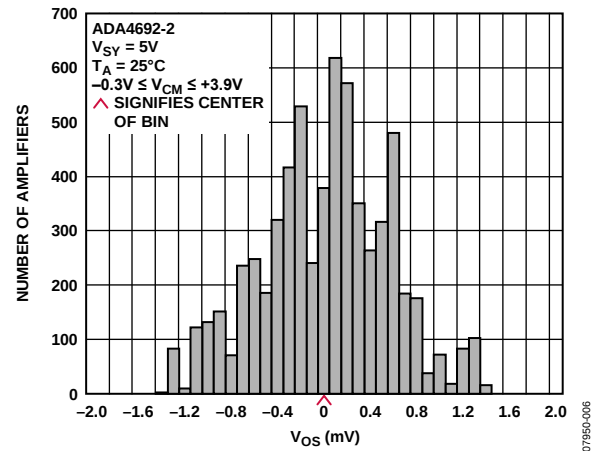


Figure 12. Input Offset Voltage Distribution

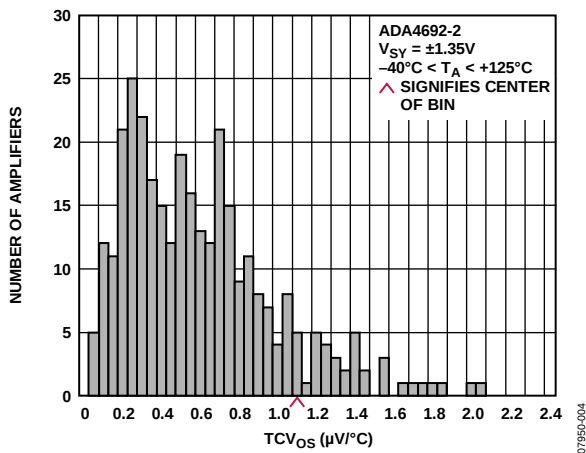


Figure 10. Input Offset Voltage Drift Distribution

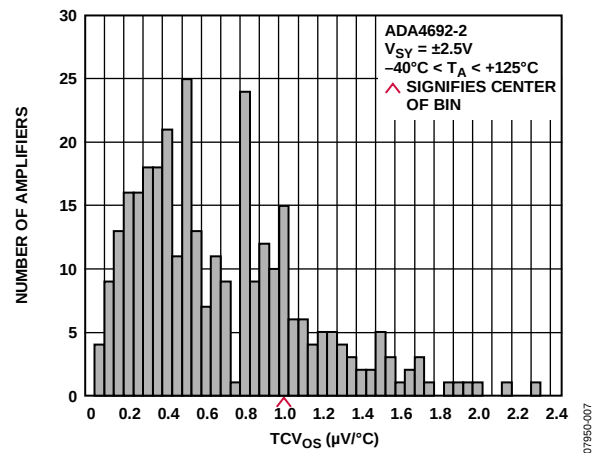


Figure 13. Input Offset Voltage Drift Distribution

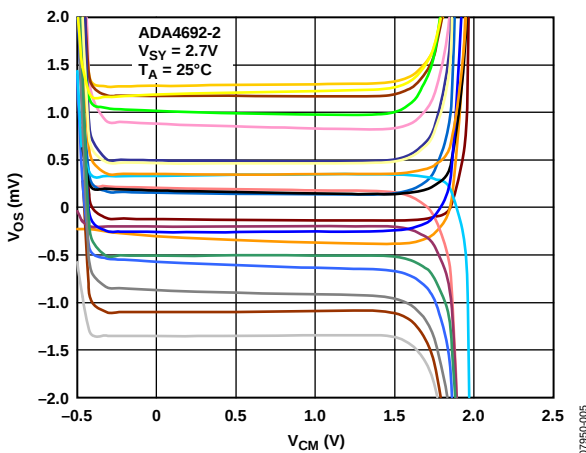


Figure 11. Input Offset Voltage vs. Common-Mode Voltage

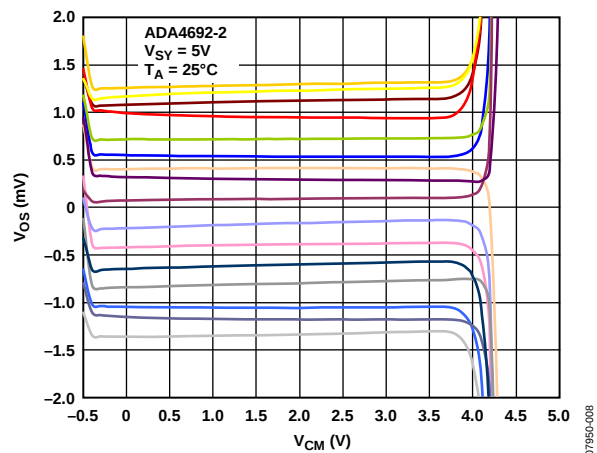


Figure 14. Input Offset Voltage vs. Common-Mode Voltage

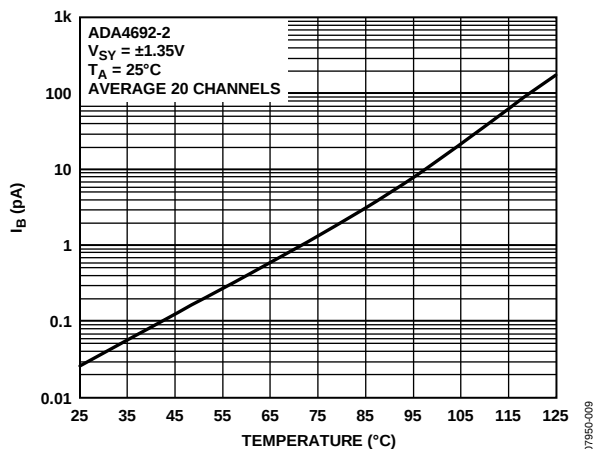


Figure 15. Input Bias Current vs. Temperature

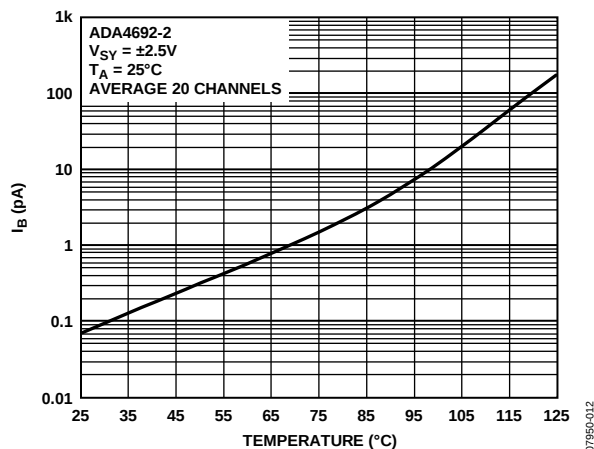


Figure 18. Input Bias Current vs. Temperature

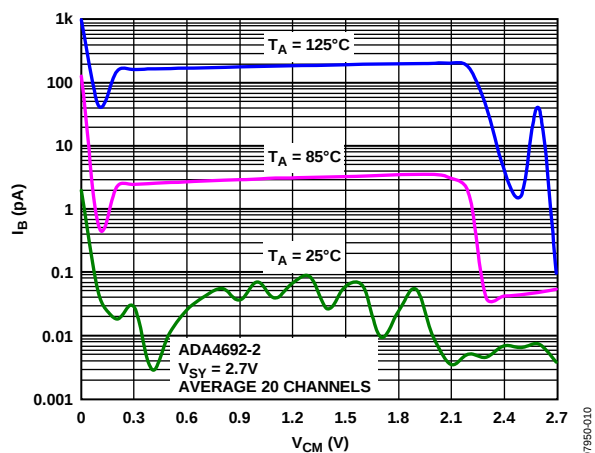


Figure 16. Input Bias Current vs. Common-Mode Voltage

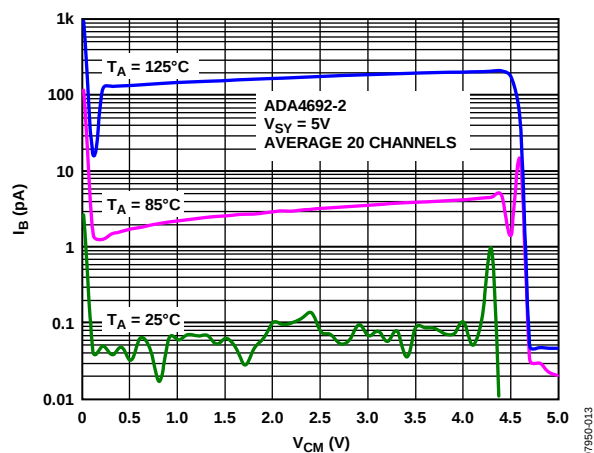
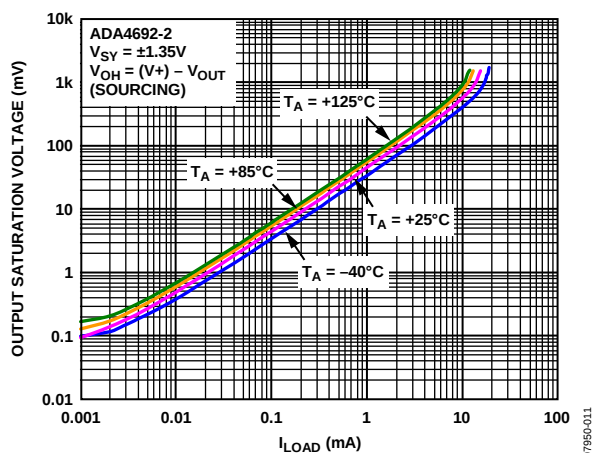
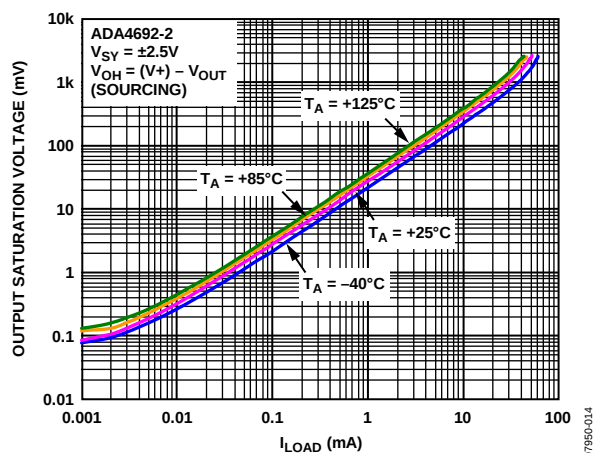


Figure 19. Input Bias Current vs. Common-Mode Voltage

Figure 17. Output Voltage (V_{OH}) to Supply Rail vs. Load CurrentFigure 20. Output Voltage (V_{OH}) to Supply Rail vs. Load Current

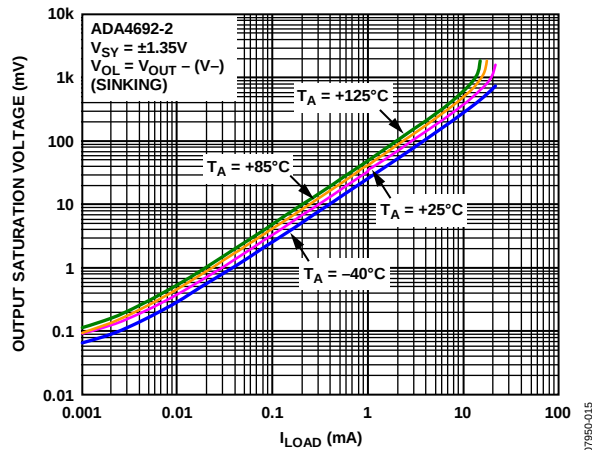


Figure 21. Output Voltage (V_{OL}) to Supply Rail vs. Load Current

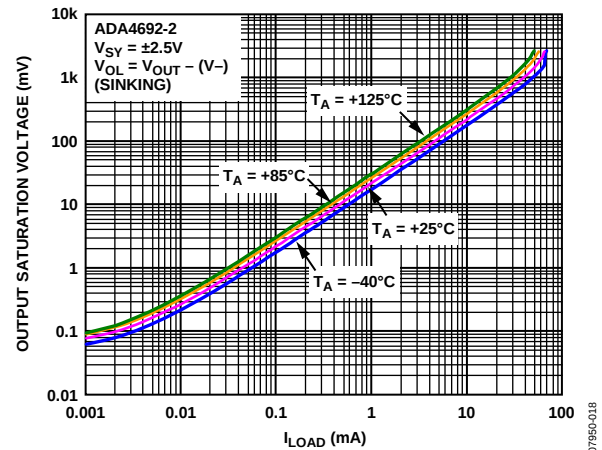


Figure 24. Output Voltage (V_{OL}) to Supply Rail vs. Load Current

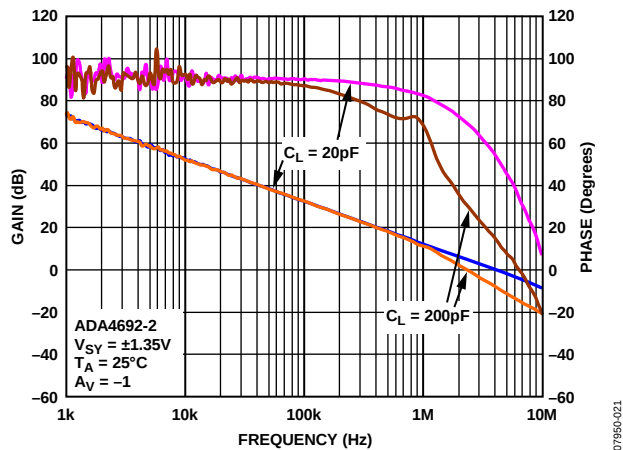


Figure 22. Open-Loop Gain and Phase vs. Frequency

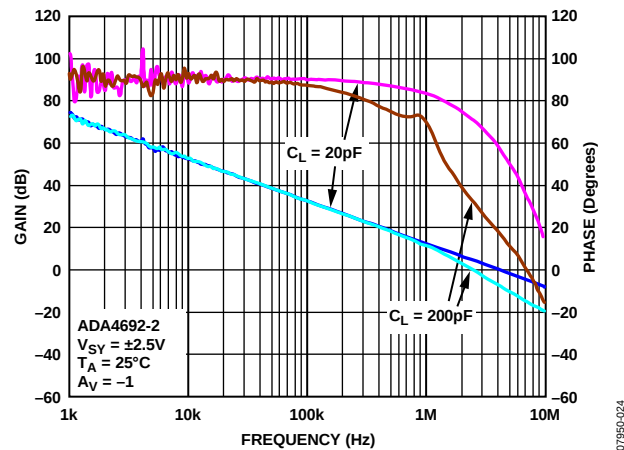


Figure 25. Open-Loop Gain and Phase vs. Frequency

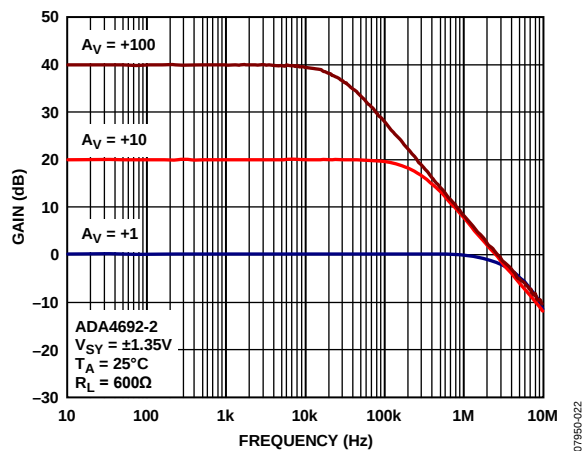


Figure 23. Closed-Loop Gain vs. Frequency

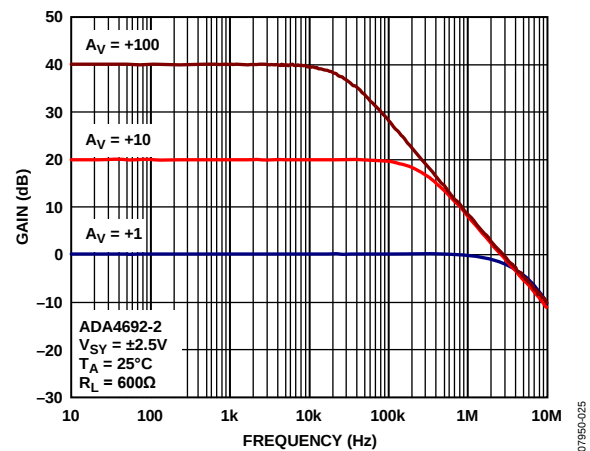


Figure 26. Closed-Loop Gain vs. Frequency

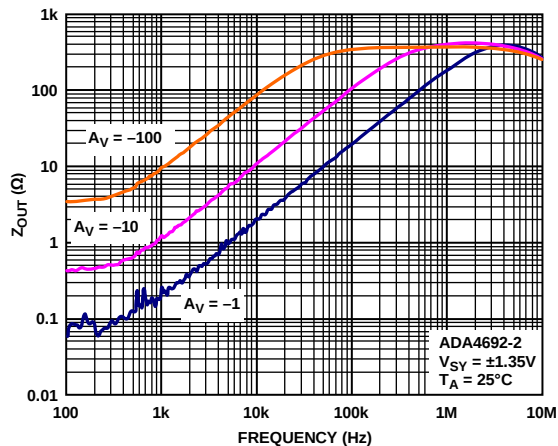


Figure 27. Output Impedance vs. Frequency

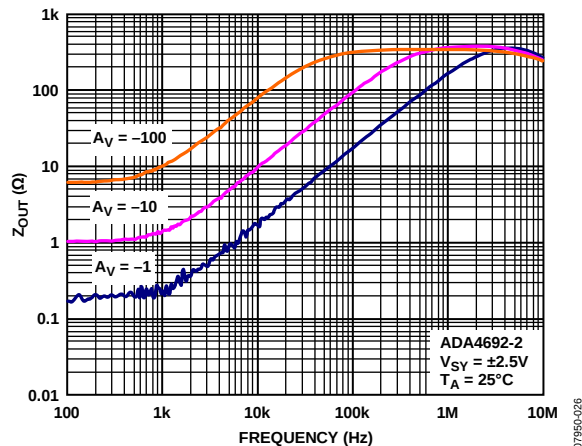


Figure 30. Output Impedance vs. Frequency

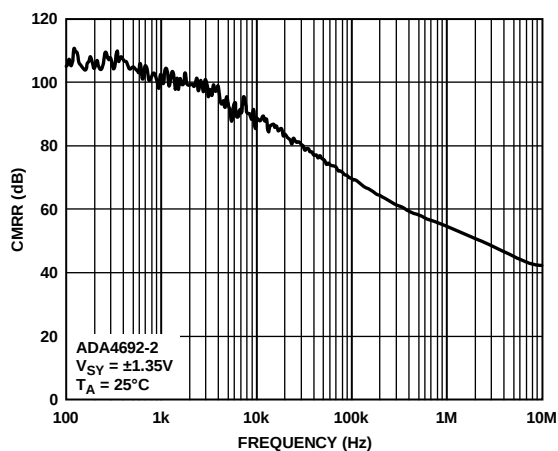


Figure 28. CMRR vs. Frequency

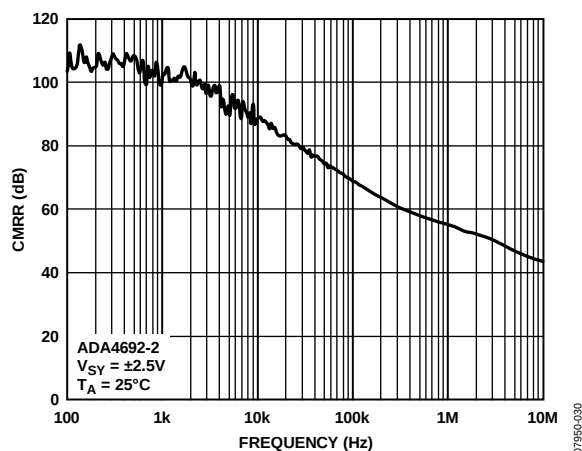


Figure 31. CMRR vs. Frequency

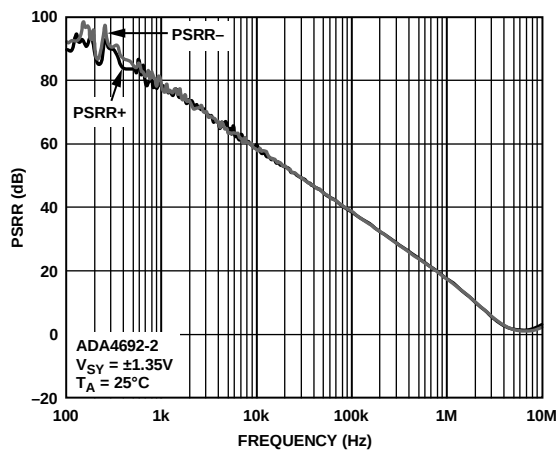


Figure 29. PSRR vs. Frequency

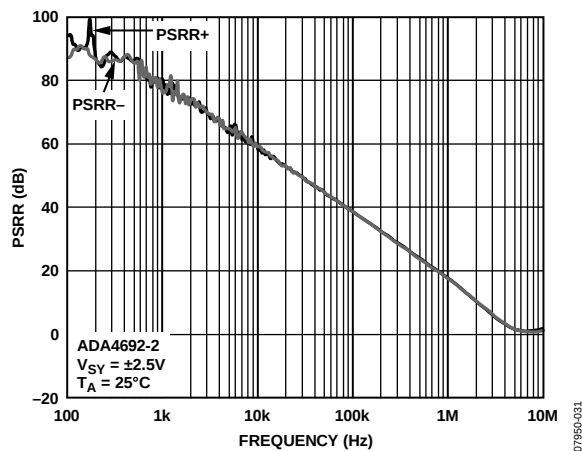


Figure 32. PSRR vs. Frequency

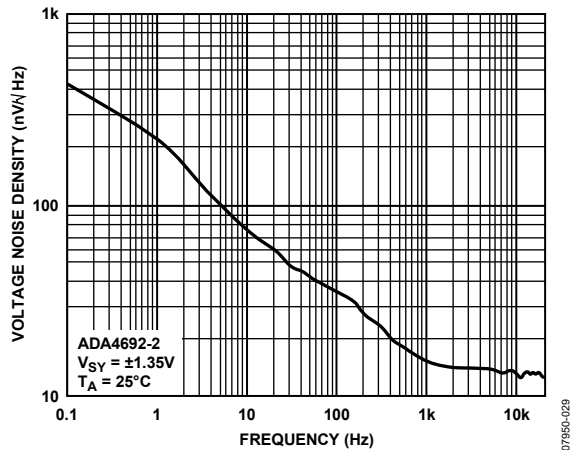


Figure 33. Voltage Noise Density vs. Frequency

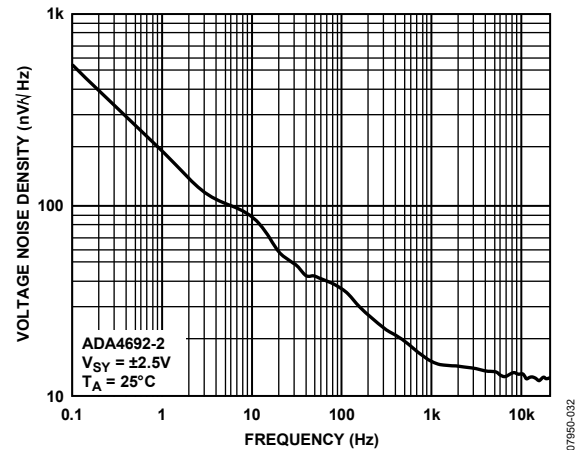


Figure 36. Voltage Noise Density vs. Frequency

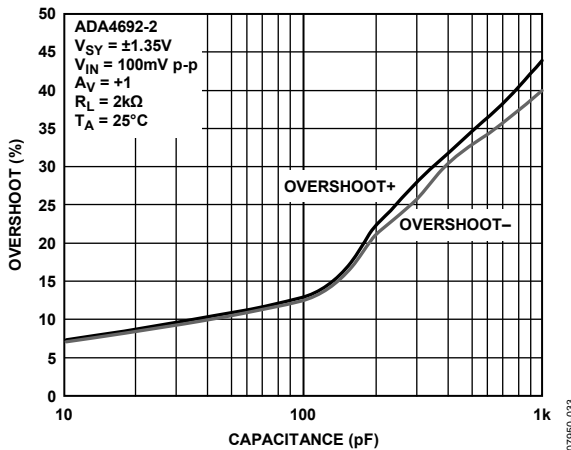


Figure 34. Small Signal Overshoot vs. Load Capacitance

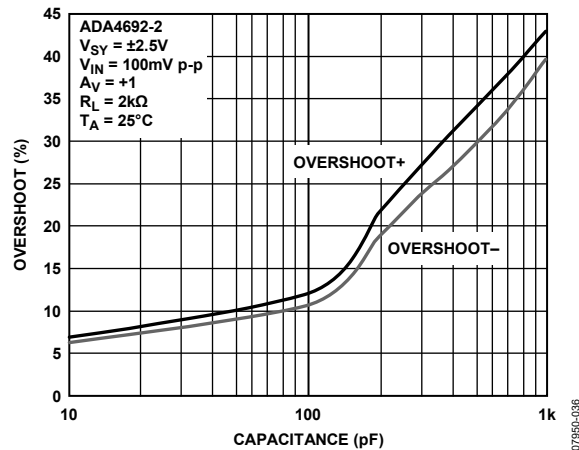


Figure 37. Small Signal Overshoot vs. Load Capacitance

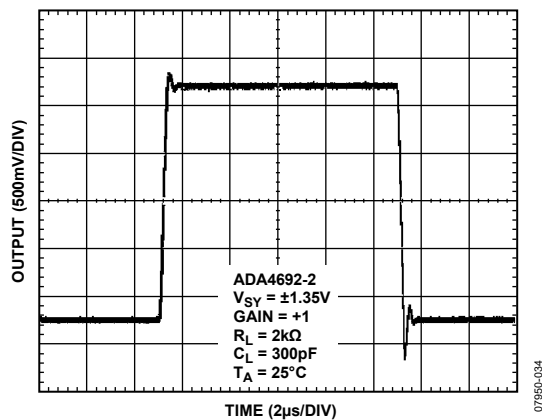


Figure 35. Large Signal Transient Response

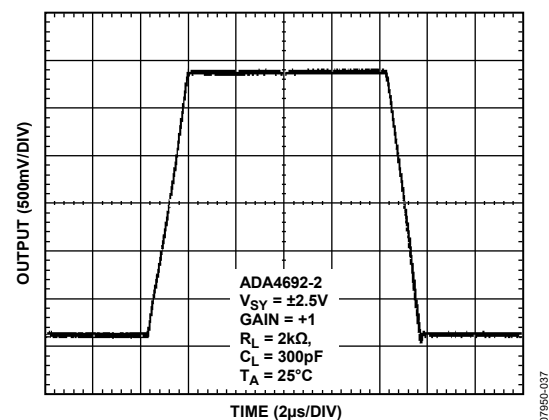


Figure 38. Large Signal Transient Response

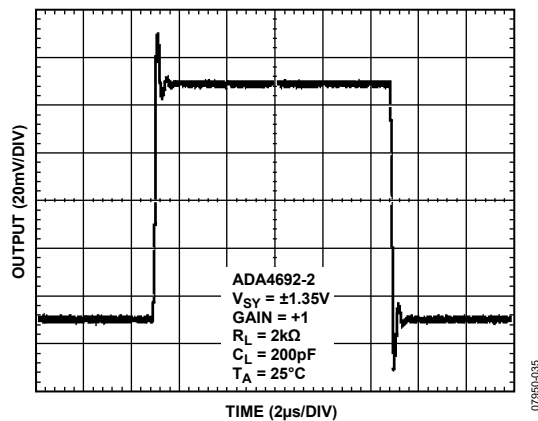


Figure 39. Small Signal Transient Response

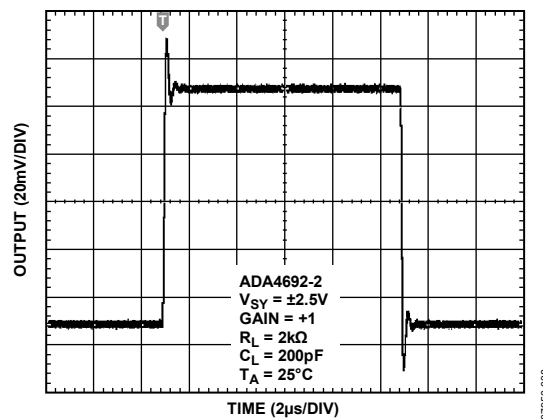


Figure 42. Small Signal Transient Response

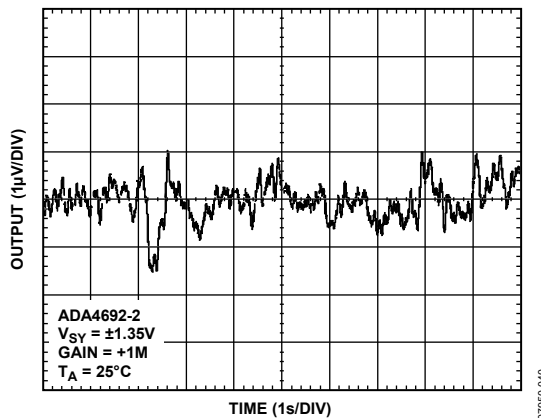


Figure 40. 0.1 Hz to 10 Hz Noise

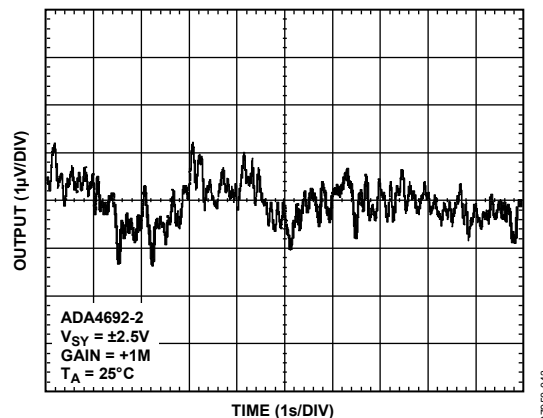


Figure 43. 0.1 Hz to 10 Hz Noise

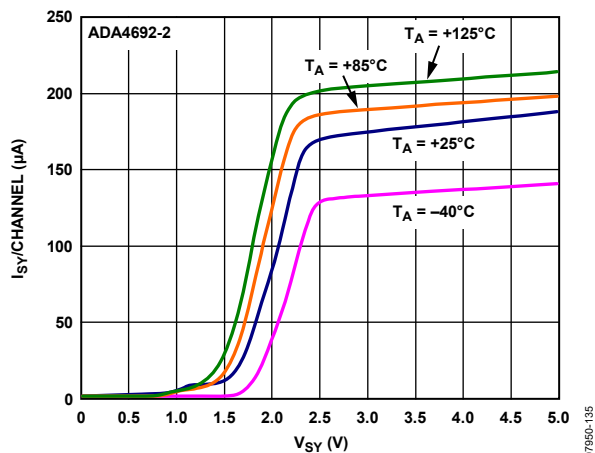


Figure 41. Supply Current per Amplifier vs. Supply Voltage

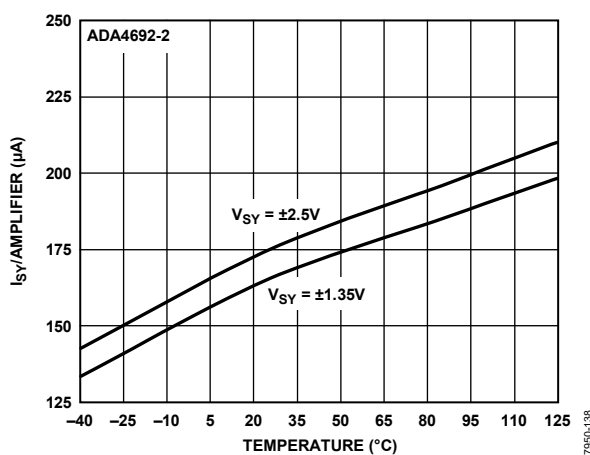


Figure 44. Supply Current per Channel vs. Temperature

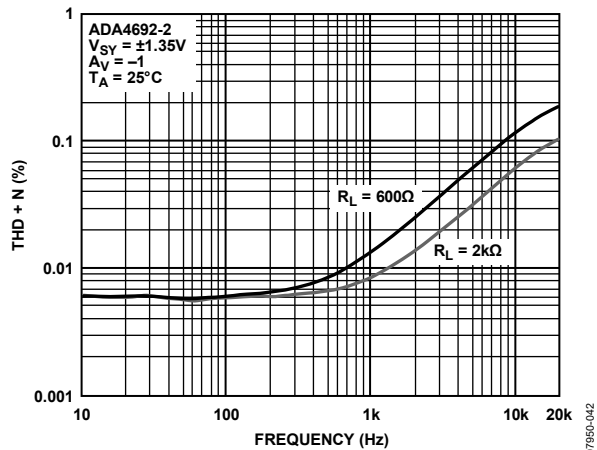


Figure 45. THD + Noise vs. Frequency

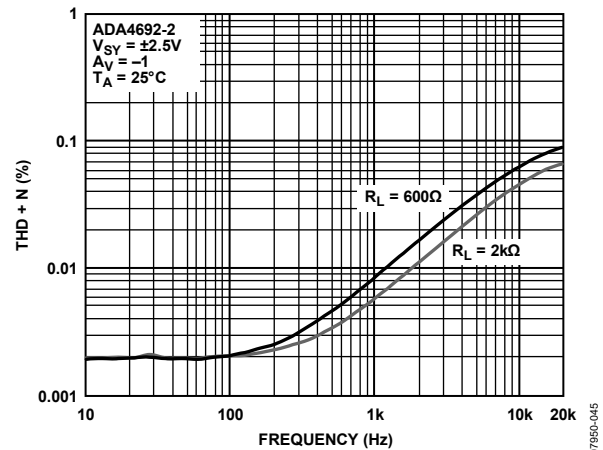


Figure 48. THD + Noise vs. Frequency

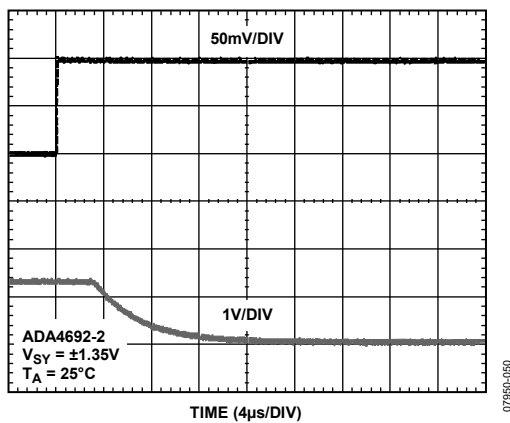


Figure 46. Positive Overload Recovery

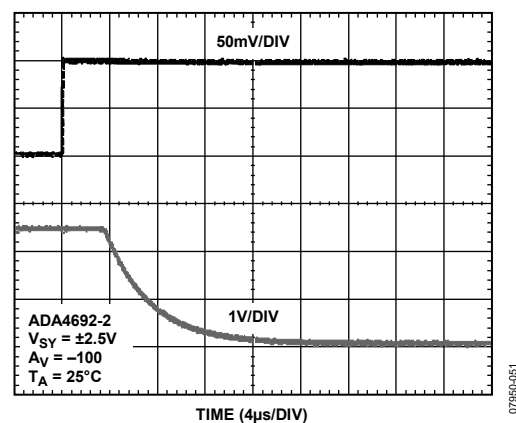


Figure 49. Positive Overload Recovery

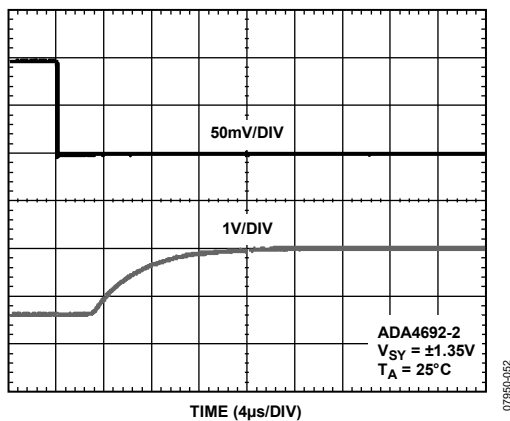


Figure 47. Negative Overload Recovery

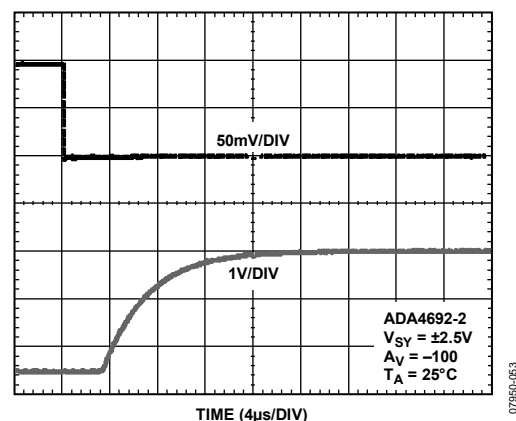


Figure 50. Negative Overload Recovery

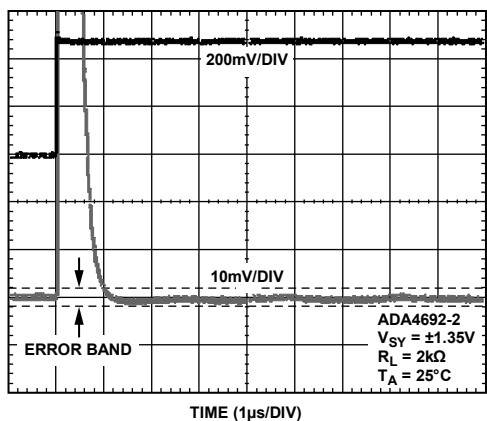


Figure 51. Positive Settling Time to 0.1%

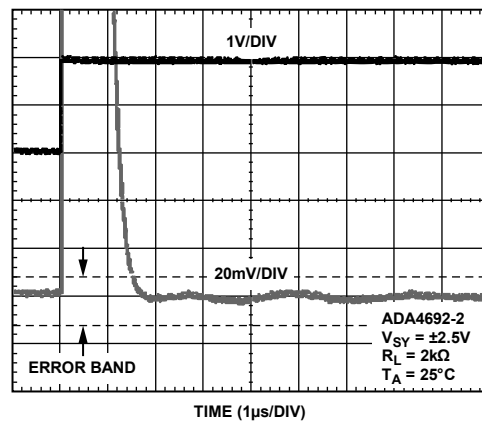


Figure 54. Positive Settling Time to 0.1%

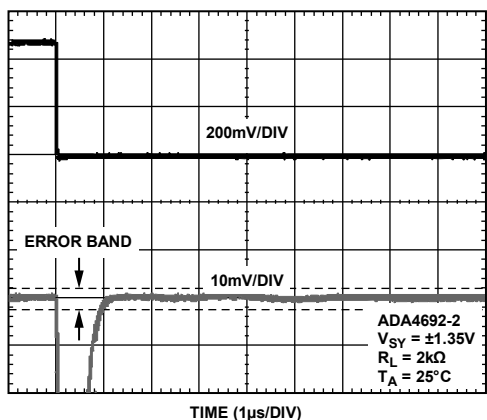


Figure 52. Negative Settling Time to 0.1%

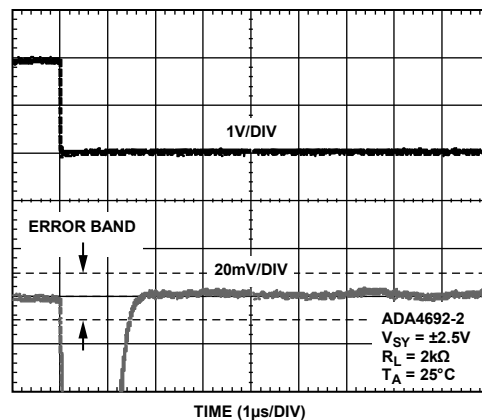


Figure 55. Negative Settling Time to 0.1%

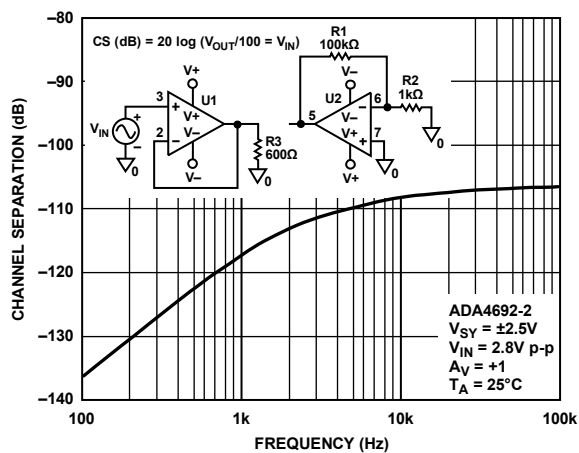


Figure 53. Channel Separation (CS) vs. Frequency

SHUTDOWN OPERATION

INPUT PIN CHARACTERISTICS

The ADA4691-2 has a classic CMOS logic inverter input for each shutdown pin, as shown in Figure 56.

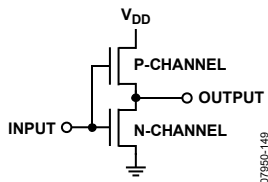


Figure 56. CMOS Inverter

With slowly changing inputs, the top transistor and bottom transistor may be slightly on at the same time, increasing the supply current. This can be avoided by driving the input with a digital logic output having fast rise and fall times. Figure 57 through Figure 59 show the supply current for both sections switching simultaneously with rise times of 1 μ s, 10 μ s, and 1 ms. Clearly, the rise and fall times should be faster than 10 μ s. Using an RC time constant to enable/disable shutdown is not recommended.

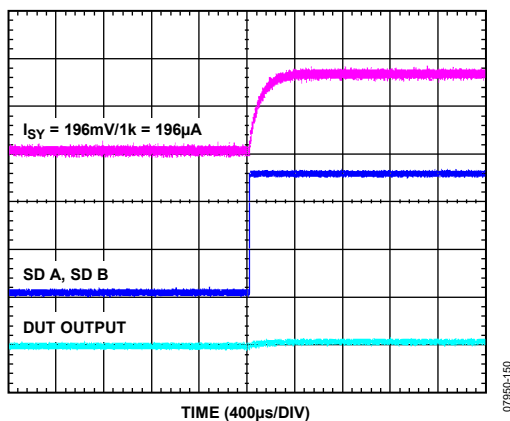


Figure 57. Shutdown Pin Rise Time = 1 μ s

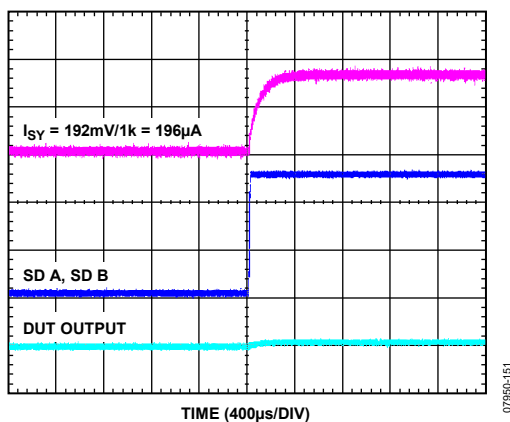


Figure 58. Shutdown Pin Rise Time = 10 μ s

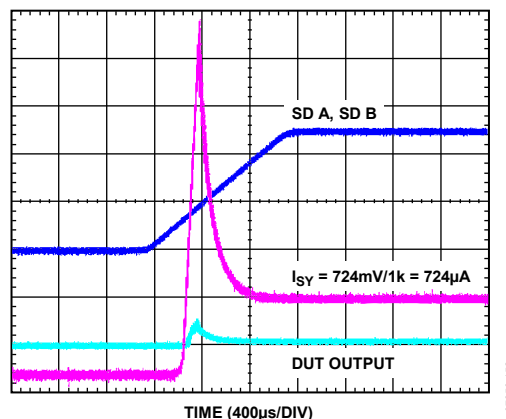


Figure 59. Shutdown Pin Rise Time = 1 ms

INPUT THRESHOLD

The input threshold is approximately 1.2 V above the V₋ pin when operating on ground and 5 V and 0.9 V when operating on 2.7 V (see Figure 60 and Figure 61). The threshold is relatively stable over temperature. For operation on split supplies, the logic swing may have to be level shifted.

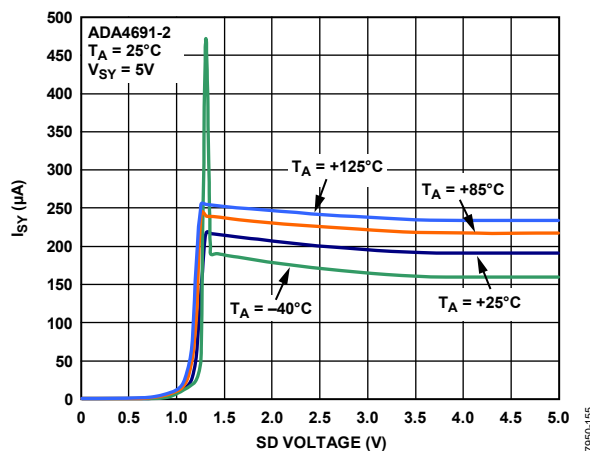


Figure 60. Supply Current vs. Temperature, $V_{SV} = 5$ V

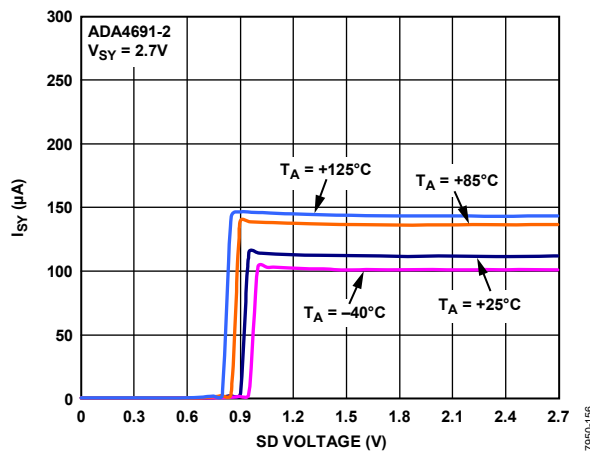
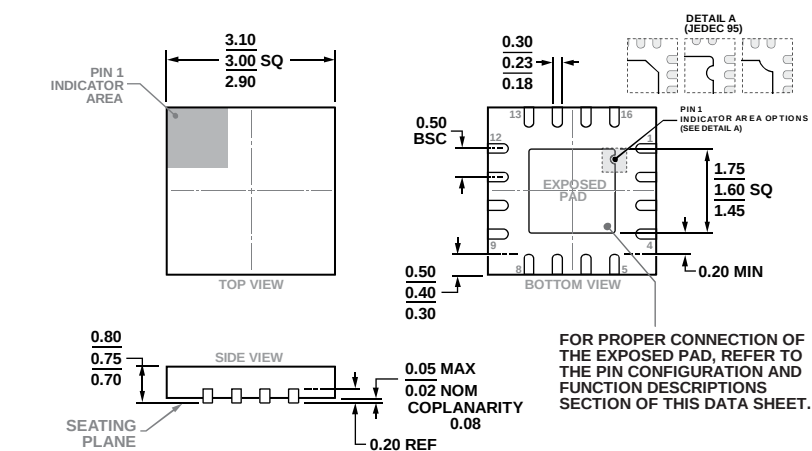


Figure 61. Supply Current vs. Temperature, $V_{SV} = 2.7$ V

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6

Figure 62. 16-Lead Lead Frame Chip Scale Package [LFCSP]

3 mm × 3 mm Body and 0.75 mm Package Height

(CP-16-22)

Dimensions shown in millimeters

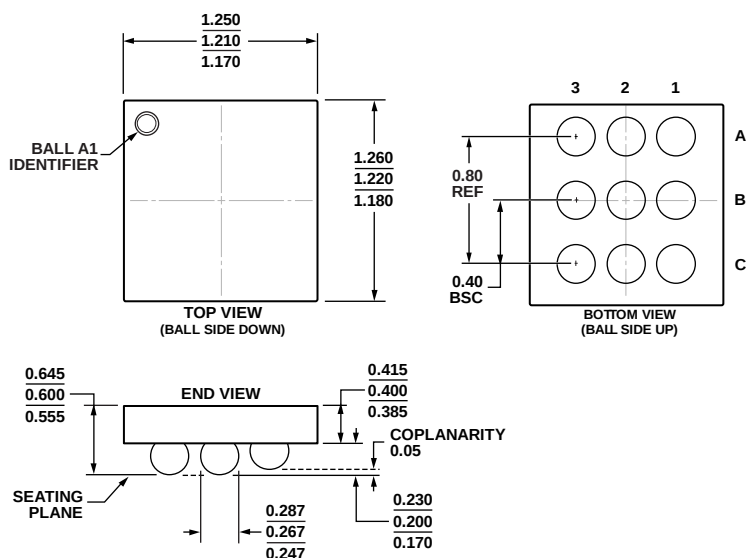


Figure 63. 9-Ball Wafer Level Chip Scale Package [WLCSP]

(CB-9-3)

Dimensions shown in millimeters

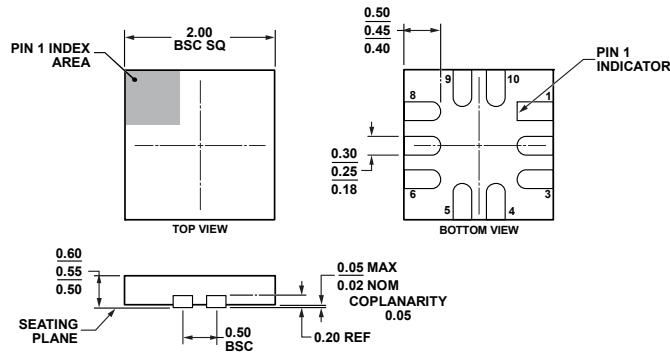


Figure 64. 10-Lead Lead Frame Chip Scale Package [LFCSP]
2 mm x 2 mm Body and 0.55 mm Package Height
(CP-10-11)
Dimensions shown in millimeters

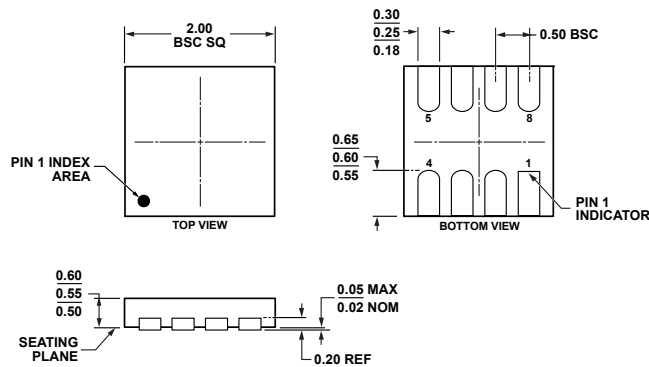
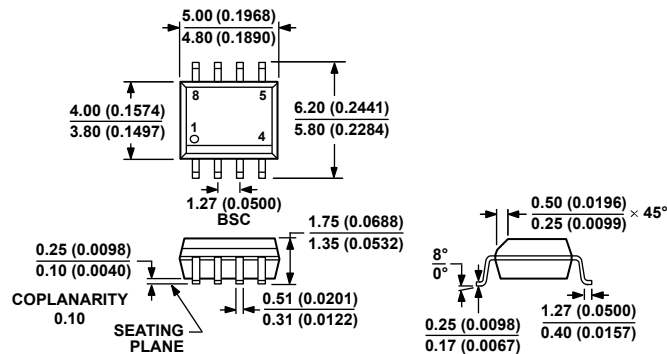


Figure 65. 8-Lead Lead Frame Chip Scale Package [LFCSP]
2 mm x 2 mm Body and 0.55 mm Package Height
(CP-8-6)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 66. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

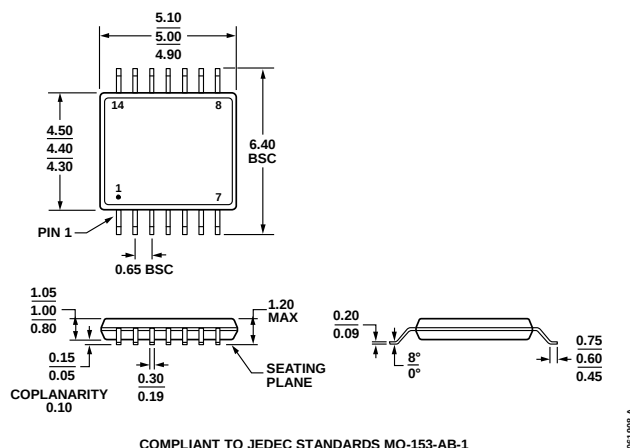


Figure 67. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Marking Code
ADA4691-2ACBZ-R7	–40°C to +125°C	9-Ball WLCSP	CB-9-3	A2C
ADA4691-2ACPZ-R7	–40°C to +125°C	10-Lead LFCSP	CP-10-11	A2
ADA4691-4ACPZ-R2	–40°C to +125°C	16-Lead LFCSP	CP-16-22	A2P
ADA4691-4ACPZ-R7	–40°C to +125°C	16-Lead LFCSP	CP-16-22	A2P
ADA4691-4ACPZ-RL	–40°C to +125°C	16-Lead LFCSP	CP-16-22	A2P
ADA4692-2ACPZ-R7	–40°C to +125°C	8-Lead LFCSP	CP-8-6	A3
ADA4692-2ARZ	–40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4692-2ARZ-R7	–40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4692-2ARZ-RL	–40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4692-4ARUZ	–40°C to +125°C	14-Lead TSSOP	RU-14	
ADA4692-4ARUZ-RL	–40°C to +125°C	14-Lead TSSOP	RU-14	

¹ Z = RoHS Compliant Part.