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REVISION HISTORY

3/14—Rev. F to Rev. G

Changes to Second Paragraph of Theory of Operation Section...	13
Changes to Ordering Guide	20

8/13—Rev. E to Rev. F

Changed Input Current Noise at $f = 100$ kHz from 2.4 pA/√Hz to 0.4 pA/√Hz (Throughout)	3
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6/13—Rev. D to Rev. E

Changes to DC Performance Parameter, Table 1	3
Updated Outline Dimensions	19
Changes to Ordering Guide	20

11/08—Rev. C to Rev. D

Change to Table 3 Column Heading.....	5
Change to Ordering Guide	20

7/06—Rev. B to Rev. C

Updated Format.....	Universal
Updated Outline Dimensions	18
Change to Ordering Guide	20

9/99—Rev. A to Rev. B

SPECIFICATIONS

+2.7 V SUPPLY

@ $T_A = 25^\circ\text{C}$, $V_S = 2.7\text{ V}$, $R_L = 1\text{ k}\Omega$ to 1.35 V , $R_F = 2.5\text{ k}\Omega$, unless otherwise noted.

Table 1.

Parameter	Conditions	AD8031A/AD8032A			AD8031B/AD8032B			Unit
		Min	Typ	Max	Min	Typ	Max	
DYNAMIC PERFORMANCE								
–3 dB Small Signal Bandwidth	G = +1, V _O < 0.4 V p-p	54	80		54	80		MHz
Slew Rate	G = –1, V _O = 2 V step	25	30		25	30		V/μs
Settling Time to 0.1%	G = –1, V _O = 2 V step, C _L = 10 pF		125			125		ns
DISTORTION/NOISE PERFORMANCE								
Total Harmonic Distortion	f _C = 1 MHz, V _O = 2 V p-p, G = +2		–62			–62		dBc
	f _C = 100 kHz, V _O = 2 V p-p, G = +2		–86			–86		dBc
Input Voltage Noise	f = 1 kHz		15			15		nV/√Hz
Input Current Noise	f = 100 kHz		0.4			0.4		pA/√Hz
	f = 1 kHz		5			5		pA/√Hz
Crosstalk (AD8032 Only)	f = 5 MHz		–60			–60		dB
DC PERFORMANCE								
Input Offset Voltage	V _{CM} = V _{CC} /2; V _{OUT} = 1.35 V		±1	±6		±0.5	±1.5	mV
	T _{MIN} to T _{MAX}		±6	±10		±1.6	±2.5	mV
Offset Drift	V _{CM} = V _{CC} /2; V _{OUT} = 1.35 V		10			10		μV/°C
Input Bias Current	V _{CM} = V _{CC} /2; V _{OUT} = 1.35 V		0.45	2		0.45	2	μA
	T _{MIN} to T _{MAX}			2.2			2.2	μA
Input Offset Current			50	500		50	500	nA
Open-Loop Gain	V _{CM} = V _{CC} /2; V _{OUT} = 0.35 V to 2.35 V	76	80		76	80		dB
	T _{MIN} to T _{MAX}	74			74			dB
INPUT CHARACTERISTICS								
Common-Mode Input Resistance			40			40		MΩ
Differential Input Resistance			280			280		kΩ
Input Capacitance			1.6			1.6		pF
Input Voltage Range			–0.5 to +3.2			–0.5 to +3.2		V
Input Common-Mode Voltage Range			–0.2 to +2.9			–0.2 to +2.9		V
Common-Mode Rejection Ratio	V _{CM} = 0 V to 2.7 V	46	64		46	64		dB
	V _{CM} = 0 V to 1.55 V	58	74		58	74		dB
Differential Input Voltage				3.4			3.4	V
OUTPUT CHARACTERISTICS								
Output Voltage Swing Low	R _L = 10 kΩ	0.05	0.02		0.05	0.02		V
Output Voltage Swing High		2.6	2.68		2.6	2.68		V
Output Voltage Swing Low	R _L = 1 kΩ	0.15	0.08		0.15	0.08		V
Output Voltage Swing High		2.55	2.6		2.55	2.6		V
Output Current			15			15		mA
Short Circuit Current	Sourcing		21			21		mA
	Sinking		–34			–34		mA
Capacitive Load Drive	G = +2 (See Figure 46)		15			15		pF
POWER SUPPLY								
Operating Range		2.7		12	2.7		12	V
Quiescent Current per Amplifier			750	1250		750	1250	μA
Power Supply Rejection Ratio	V _{S–} = 0 V to –1 V or V _{S+} = +2.7 V to +3.7 V	75	86		75	86		dB

+5 V SUPPLY

@ $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_L = 1\text{ k}\Omega$ to 2.5 V , $R_F = 2.5\text{ k}\Omega$, unless otherwise noted.

Table 2.

Parameter	Conditions	AD8031A/AD8032A			AD8031B/AD8032B			Unit
		Min	Typ	Max	Min	Typ	Max	
DYNAMIC PERFORMANCE								
–3 dB Small Signal Bandwidth	G = +1, V _O < 0.4 V p-p	54	80		54	80		MHz
Slew Rate	G = –1, V _O = 2 V step	27	32		27	32		V/μs
Settling Time to 0.1%	G = –1, V _O = 2 V step, C _L = 10 pF		125			125		ns
DISTORTION/NOISE PERFORMANCE								
Total Harmonic Distortion	f _C = 1 MHz, V _O = 2 V p-p, G = +2		–62			–62		dBc
	f _C = 100 kHz, V _O = 2 V p-p, G = +2		–86			–86		dBc
Input Voltage Noise	f = 1 kHz		15			15		nV/√Hz
Input Current Noise	f = 100 kHz		0.4			0.4		pA/√Hz
	f = 1 kHz		5			5		pA/√Hz
Differential Gain	R _L = 1 kΩ		0.17			0.17		%
Differential Phase	R _L = 1 kΩ		0.11			0.11		Degrees
Crosstalk (AD8032 Only)	f = 5 MHz		–60			–60		dB
DC PERFORMANCE								
Input Offset Voltage	V _{CM} = V _{CC} /2; V _{OUT} = 2.5 V		±1	±6		±0.5	±1.5	mV
	T _{MIN} to T _{MAX}		±6	±10		±1.6	±2.5	mV
Offset Drift	V _{CM} = V _{CC} /2; V _{OUT} = 2.5 V		5			5		μV/°C
Input Bias Current	V _{CM} = V _{CC} /2; V _{OUT} = 2.5 V		0.45	1.2		0.45	1.2	μA
	T _{MIN} to T _{MAX}			2.0			2.0	μA
Input Offset Current			50	350		50	250	nA
Open-Loop Gain	V _{CM} = V _{CC} /2; V _{OUT} = 1.5 V to 3.5 V	76	82		76	82		dB
	T _{MIN} to T _{MAX}	74			74			dB
INPUT CHARACTERISTICS								
Common-Mode Input Resistance			40			40		MΩ
Differential Input Resistance			280			280		kΩ
Input Capacitance			1.6			1.6		pF
Input Voltage Range			–0.5 to +5.5			–0.5 to +5.5		V
Input Common-Mode Voltage Range			–0.2 to +5.2			–0.2 to +5.2		V
Common-Mode Rejection Ratio	V _{CM} = 0 V to 5 V	56	70		56	70		dB
	V _{CM} = 0 V to 3.8 V	66	80		66	80		dB
Differential Input Voltage				3.4			3.4	V
OUTPUT CHARACTERISTICS								
Output Voltage Swing Low	R _L = 10 kΩ	0.05	0.02		0.05	0.02		V
Output Voltage Swing High		4.95	4.98		4.95	4.98		V
Output Voltage Swing Low	R _L = 1 kΩ	0.2	0.1		0.2	0.1		V
Output Voltage Swing High		4.8	4.9		4.8	4.9		V
Output Current			15			15		mA
Short Circuit Current	Sourcing		28			28		mA
	Sinking		–46			–46		mA
Capacitive Load Drive	G = +2 (See Figure 46)		15			15		pF
POWER SUPPLY								
Operating Range		2.7		12	2.7		12	V
Quiescent Current per Amplifier			800	1400		800	1400	μA
Power Supply Rejection Ratio	V _{S–} = 0 V to –1 V or V _{S+} = +5 V to +6 V	75	86		75	86		dB

±5 V SUPPLY

@ $T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{ V}$, $R_L = 1\text{ k}\Omega$ to 0 V , $R_F = 2.5\text{ k}\Omega$, unless otherwise noted.

Table 3.

Parameter	Conditions	AD8031A/AD8032A			AD8031B/AD8032B			Unit
		Min	Typ	Max	Min	Typ	Max	
DYNAMIC PERFORMANCE								
–3 dB Small Signal Bandwidth	G = +1, V _O < 0.4 V p-p	54	80		54	80		MHz
Slew Rate	G = –1, V _O = 2 V step	30	35		30	35		V/μs
Settling Time to 0.1%	G = –1, V _O = 2 V step, C _L = 10 pF		125			125		ns
DISTORTION/NOISE PERFORMANCE								
Total Harmonic Distortion	f _C = 1 MHz, V _O = 2 V p-p, G = +2		–62			–62		dBc
	f _C = 100 kHz, V _O = 2 V p-p, G = +2		–86			–86		dBc
Input Voltage Noise	f = 1 kHz		15			15		nV/√Hz
Input Current Noise	f = 100 kHz		0.4			0.4		pA/√Hz
	f = 1 kHz		5			5		pA/√Hz
Differential Gain	R _L = 1 kΩ		0.15			0.15		%
Differential Phase	R _L = 1 kΩ		0.15			0.15		Degrees
Crosstalk (AD8032 Only)	f = 5 MHz		–60			–60		dB
DC PERFORMANCE								
Input Offset Voltage	V _{CM} = 0 V; V _{OUT} = 0 V		±1	±6		±0.5	±1.5	mV
	T _{MIN} to T _{MAX}		±6	±10		±1.6	±2.5	mV
Offset Drift	V _{CM} = 0 V; V _{OUT} = 0 V		5			5		μV/°C
Input Bias Current	V _{CM} = 0 V; V _{OUT} = 0 V		0.45	1.2		0.45	1.2	μA
	T _{MIN} to T _{MAX}			2.0			2.0	μA
Input Offset Current			50	350		50	250	nA
Open-Loop Gain	V _{CM} = 0 V; V _{OUT} = ±2 V	76	80		76	80		dB
	T _{MIN} to T _{MAX}	74			74			dB
INPUT CHARACTERISTICS								
Common-Mode Input Resistance			40			40		MΩ
Differential Input Resistance			280			280		kΩ
Input Capacitance			1.6			1.6		pF
Input Voltage Range			–5.5 to +5.5			–5.5 to +5.5		V
Input Common-Mode Voltage Range			–5.2 to +5.2			–5.2 to +5.2		V
Common-Mode Rejection Ratio	V _{CM} = –5 V to +5 V	60	80		60	80		dB
	V _{CM} = –5 V to +3.5 V	66	90		66	90		dB
Differential/Input Voltage				3.4			3.4	V
OUTPUT CHARACTERISTICS								
Output Voltage Swing Low	R _L = 10 kΩ	–4.94	–4.98		–4.94	–4.98		V
Output Voltage Swing High		+4.94	+4.98		+4.94	+4.98		V
Output Voltage Swing Low	R _L = 1 kΩ	–4.7	–4.85		–4.7	–4.85		V
Output Voltage Swing High		+4.7	+4.75		+4.7	+4.75		V
Output Current			15			15		mA
Short Circuit Current	Sourcing		35			35		mA
	Sinking		–50			–50		mA
Capacitive Load Drive	G = +2 (See Figure 46)		15			15		pF
POWER SUPPLY								
Operating Range		±1.35		±6	±1.35		±6	V
Quiescent Current per Amplifier			900	1600		900	1600	μA
Power Supply Rejection Ratio	V _S – = –5 V to –6 V or V _S + = +5 V to +6 V	76	86		76	86		dB

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	12.6 V
Internal Power Dissipation ¹	
8-Lead PDIP (N)	1.3 W
8-Lead SOIC_N (R)	0.8 W
8-Lead MSOP (RM)	0.6 W
5-Lead SOT-23 (RJ)	0.5 W
Input Voltage (Common Mode)	$\pm V_s \pm 0.5$ V
Differential Input Voltage	± 3.4 V
Output Short-Circuit Duration	Observe Power Derating Curves
Storage Temperature Range (N, R, RM, RJ)	-65°C to +125°C
Lead Temperature (Soldering 10 sec)	300°C

¹ Specification is for the device in free air:

8-Lead PDIP: $\theta_{JA} = 90^\circ\text{C/W}$.

8-Lead SOIC_N: $\theta_{JA} = 155^\circ\text{C/W}$.

8-Lead MSOP: $\theta_{JA} = 200^\circ\text{C/W}$.

5-Lead SOT-23: $\theta_{JA} = 240^\circ\text{C/W}$.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8031/AD8032 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Exceeding this limit temporarily can cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

While the AD8031/AD8032 are internally short-circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves shown in Figure 7.

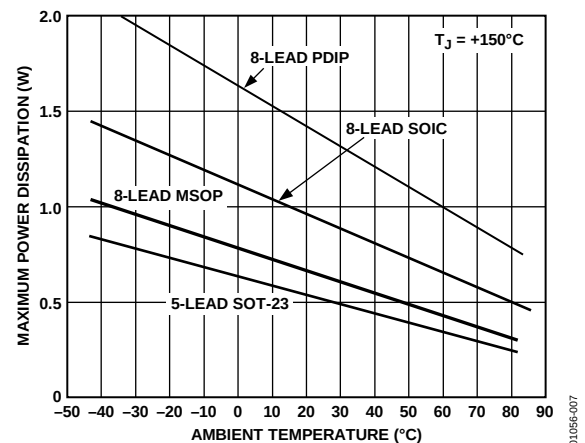


Figure 7. Maximum Power Dissipation vs. Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TYPICAL PERFORMANCE CHARACTERISTICS

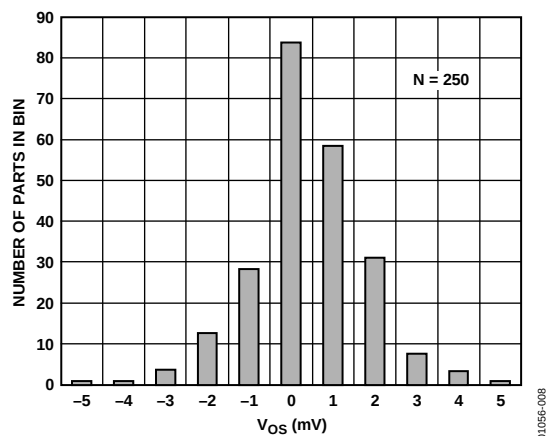
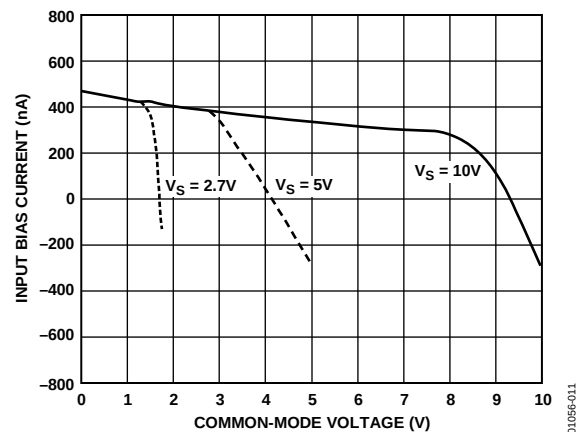
Figure 8. Typical V_{OS} Distribution @ $V_S = 5\text{ V}$ 

Figure 11. Input Bias Current vs. Common-Mode Voltage

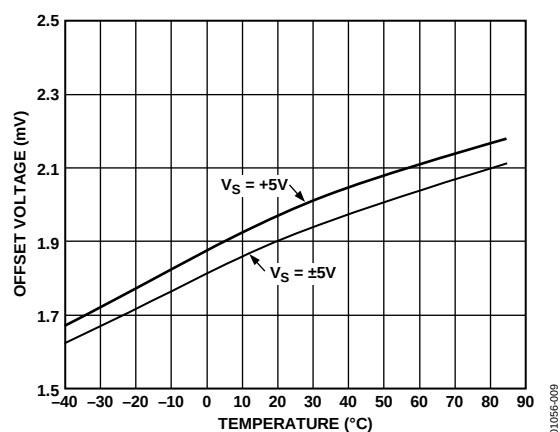


Figure 9. Input Offset Voltage vs. Temperature

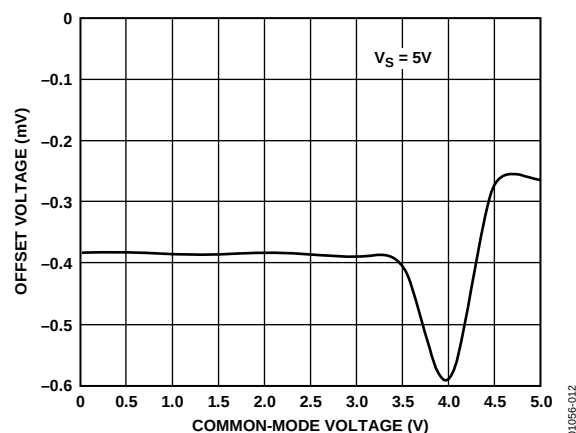
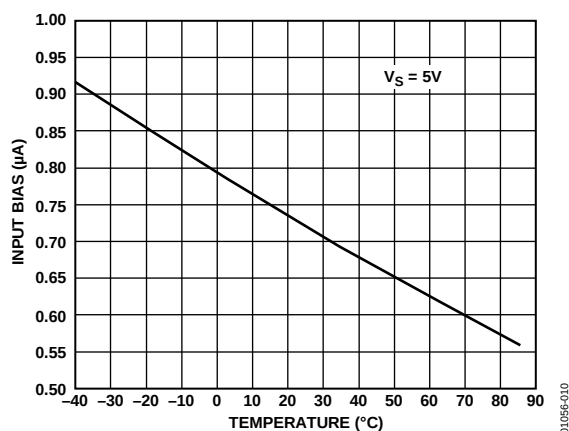
Figure 12. V_{OS} vs. Common-Mode Voltage

Figure 10. Input Bias Current vs. Temperature

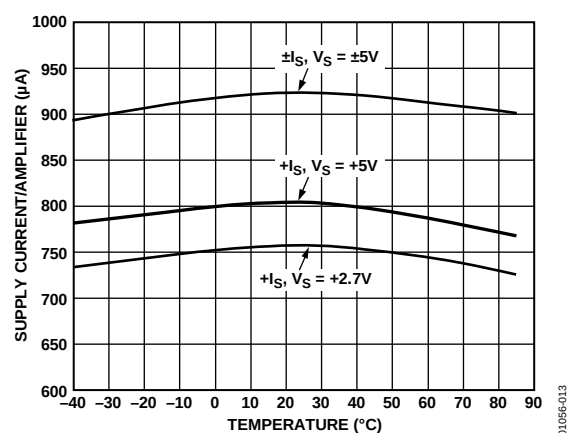
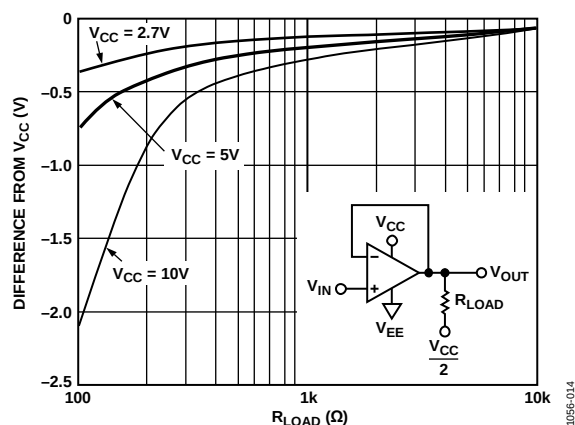
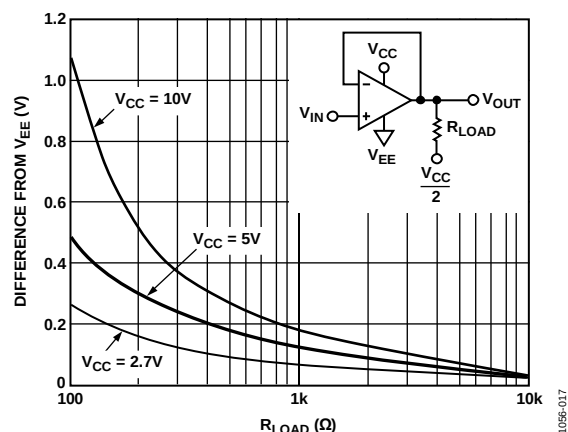
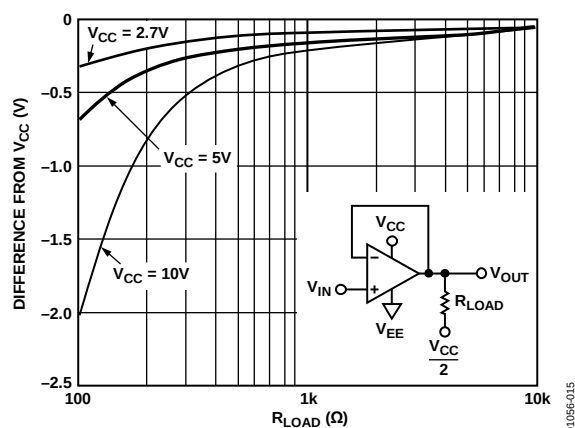
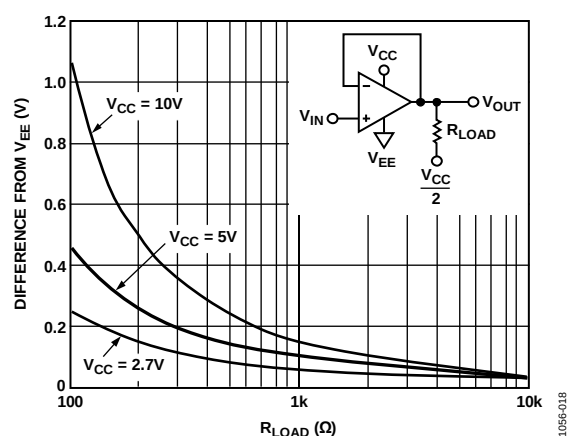
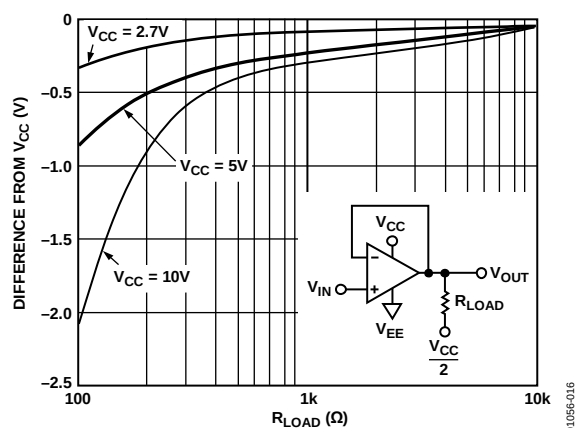
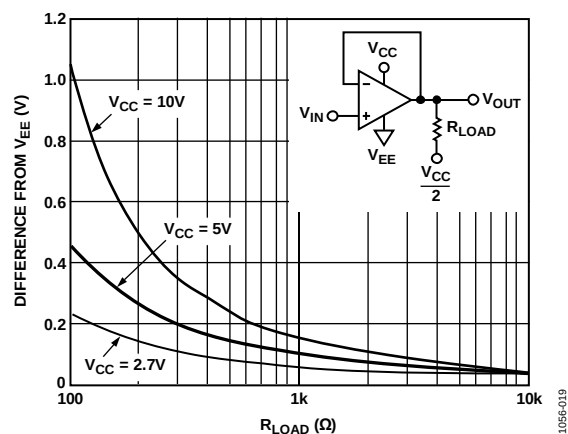


Figure 13. Supply Current vs. Temperature

Figure 14. +Output Saturation Voltage vs. R_{LOAD} @ +85°CFigure 17. -Output Saturation Voltage vs. R_{LOAD} @ +85°CFigure 15. +Output Saturation Voltage vs. R_{LOAD} @ +25°CFigure 18. -Output Saturation Voltage vs. R_{LOAD} @ +25°CFigure 16. +Output Saturation Voltage vs. R_{LOAD} @ -40°CFigure 19. -Output Saturation Voltage vs. R_{LOAD} @ -40°C

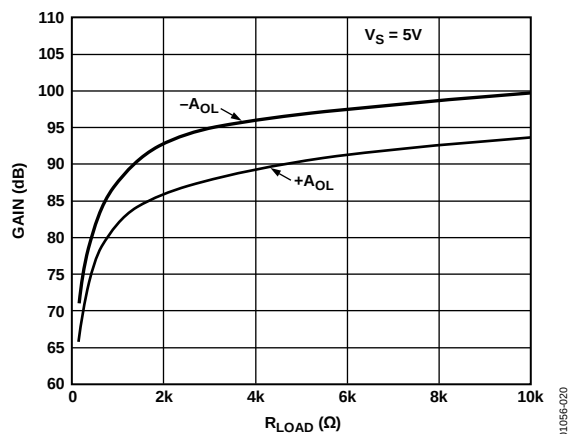
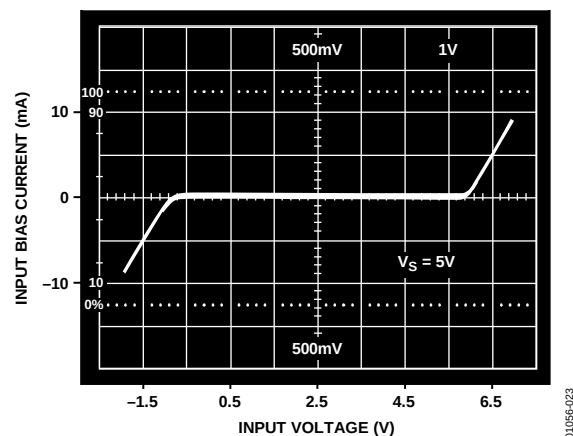
Figure 20. Open-Loop Gain (A_{OL}) vs. R_{LOAD} 

Figure 23. Differential Input Overvoltage I-V Characteristics

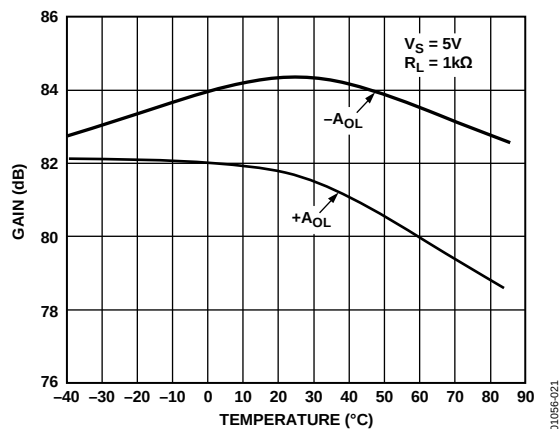
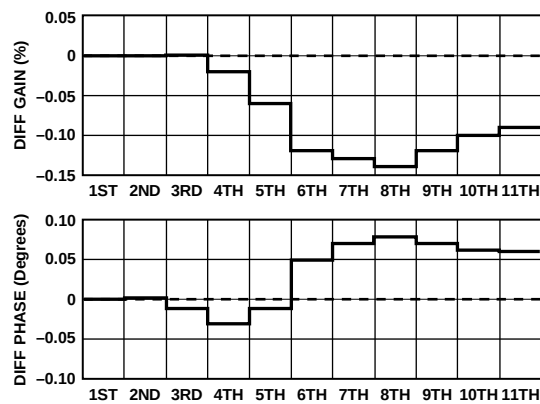
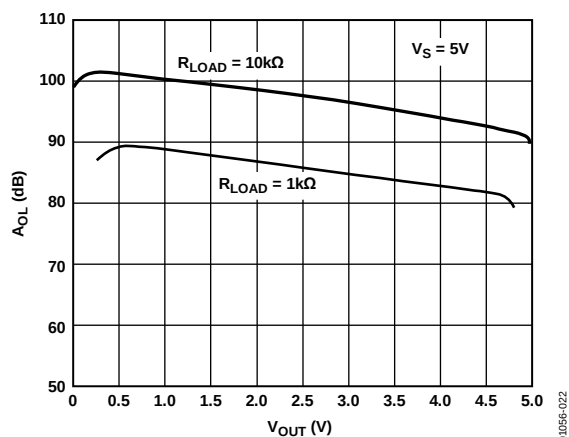
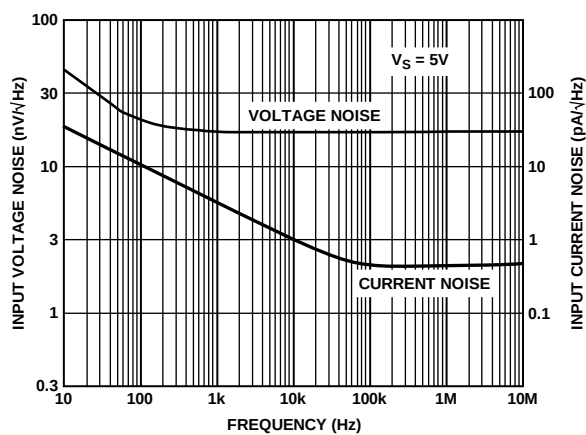
Figure 21. Open Loop Gain vs. (A_{OL}) TemperatureFigure 24. Differential Gain and Phase @ $V_S = \pm 5V$; $R_L = 1k\Omega$ Figure 22. Open-Loop Gain (A_{OL}) vs. V_{OUT} 

Figure 25. Input Voltage Noise vs. Frequency

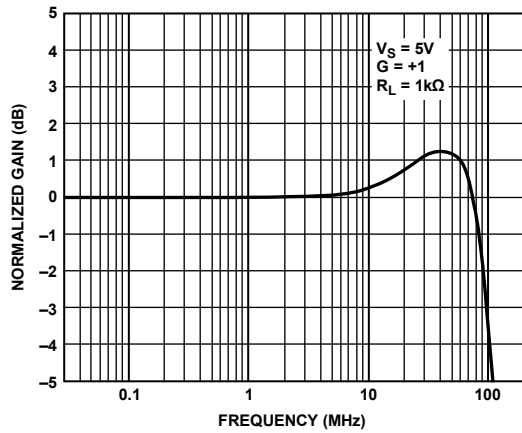


Figure 26. Unity Gain, -3 dB Bandwidth

01056-026

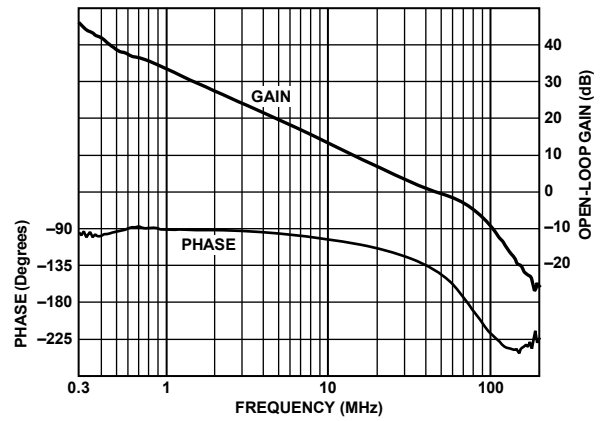


Figure 29. Open-Loop Frequency Response

01056-029

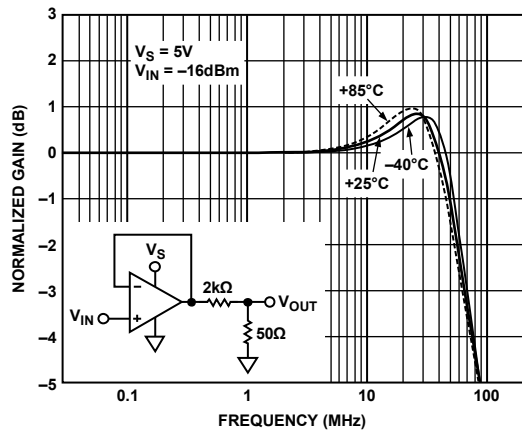
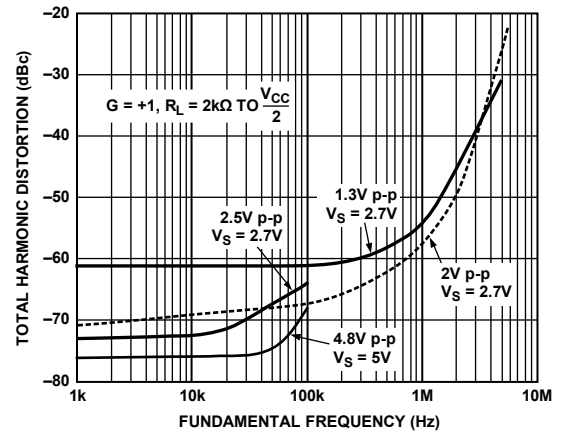


Figure 27. Closed-Loop Gain vs. Temperature

01056-027

Figure 30. Total Harmonic Distortion vs. Frequency; $G = +1$

01056-030

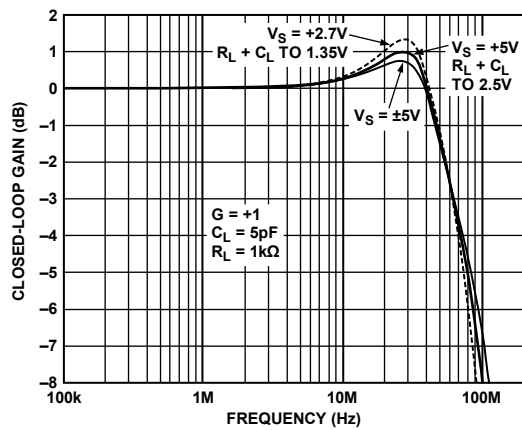
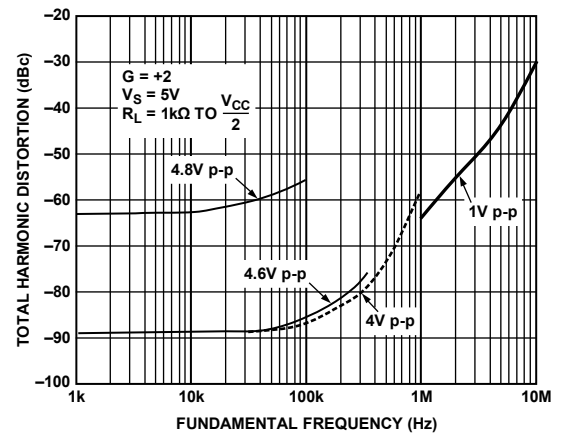


Figure 28. Closed-Loop Gain vs. Supply Voltage

01056-028

Figure 31. Total Harmonic Distortion vs. Frequency; $G = +2$

01056-031

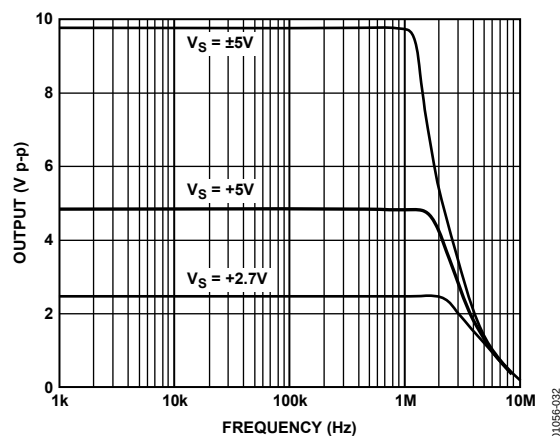


Figure 32. Large Signal Response

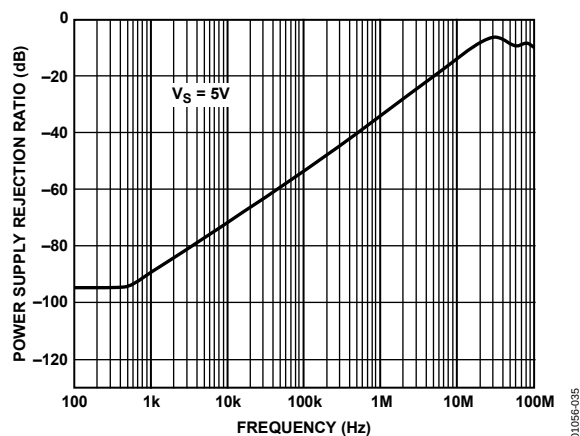


Figure 35. PSRR vs. Frequency

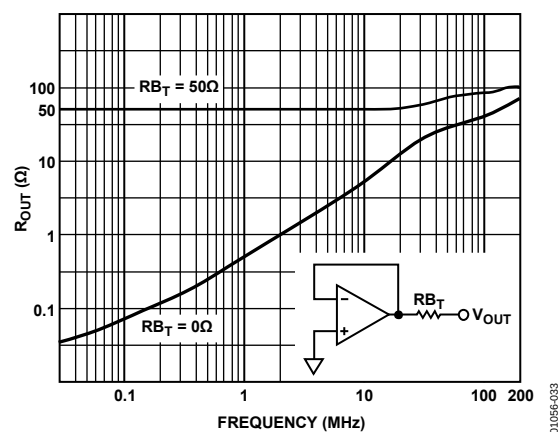
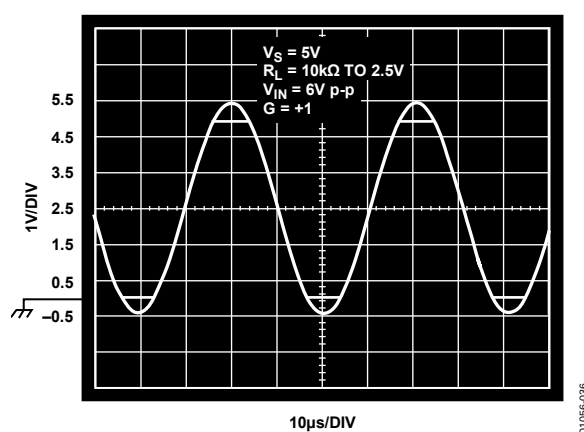
Figure 33. R_{OUT} vs. Frequency

Figure 36. Output Voltage

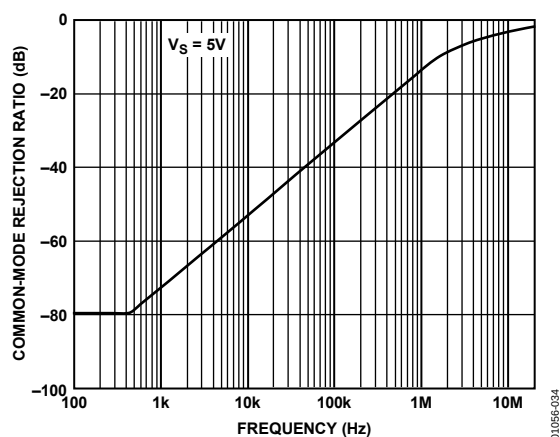


Figure 34. CMRR vs. Frequency

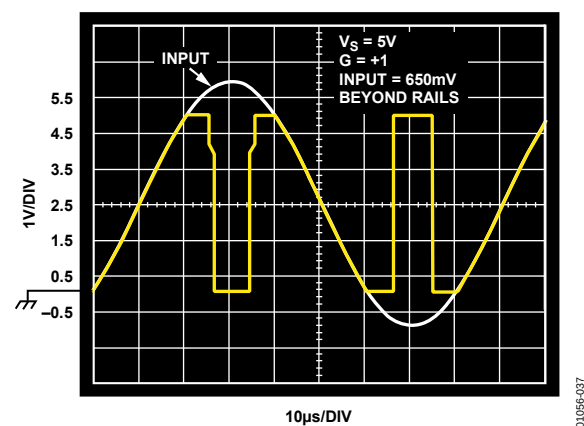


Figure 37. Output Voltage Phase Reversal Behavior

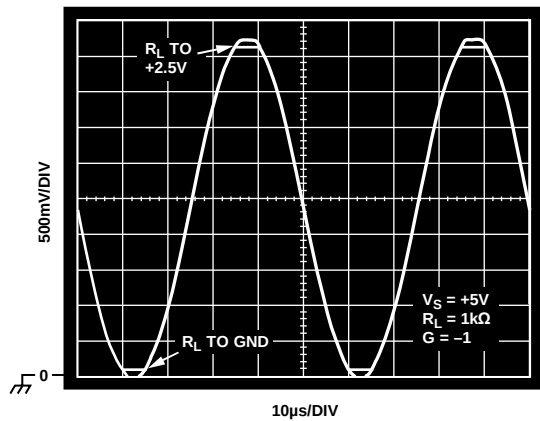


Figure 38. Output Swing

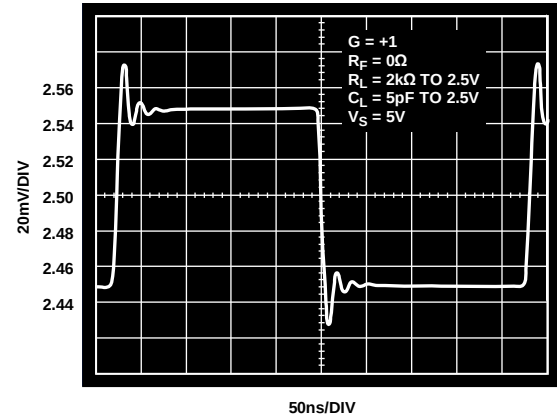


Figure 41. 100 mV Step Response

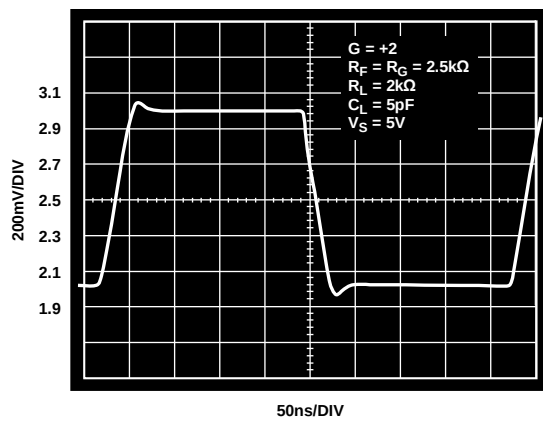


Figure 39. 1 V Step Response

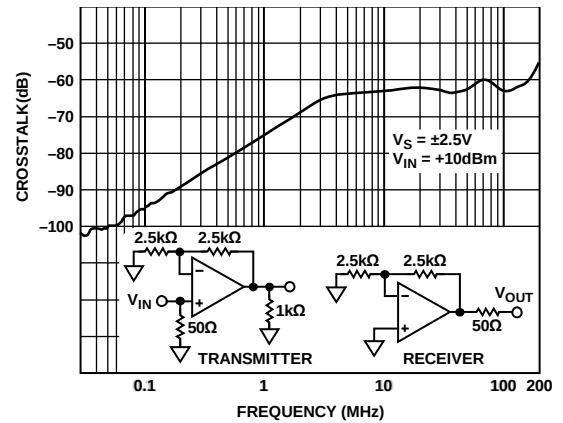


Figure 42. Crosstalk vs. Frequency

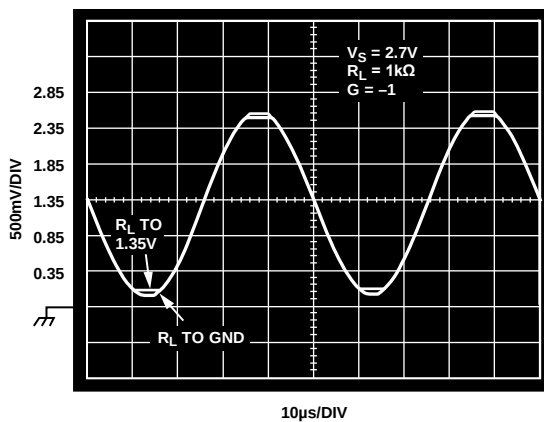


Figure 40. Output Swing

THEORY OF OPERATION

The AD8031/AD8032 are single and dual versions of high speed, low power, voltage feedback amplifiers featuring an innovative architecture that maximizes the dynamic range capability on the inputs and outputs. The linear input common-mode range exceeds either supply voltage by 200 mV, and the amplifiers show no phase reversal up to 500 mV beyond supply. The output swings to within 20 mV of either supply when driving a light load; 300 mV when driving up to 5 mA.

Fabricated on Analog Devices, Inc. eXtra Fast Complementary Bipolar (XFCB) process, the amplifier provides an impressive 80 MHz bandwidth when used as a follower and a 30 V/ μ s slew rate at only 800 μ A supply current. Careful design allows the amplifier to operate with a supply voltage as low as 2.7 V.

INPUT STAGE OPERATION

A simplified schematic of the input stage appears in Figure 43. For common-mode voltages up to 1.1 V within the positive supply (0 V to 3.9 V on a single 5 V supply), tail current I_2 flows through the PNP differential pair, Q13 and Q17. Q5 is cut off; no bias current is routed to the parallel NPN differential pair, Q2 and Q3. As the common-mode voltage is driven within 1.1 V of the positive supply, Q5 turns on and routes the tail current away from the PNP pair and to the NPN pair. During this transition region, the input current of the amplifier changes magnitude and direction. Reusing the same tail current ensures that the input stage has the same transconductance, which determines the gain and bandwidth of the amplifier, in both regions of operation.

Switching to the NPN pair as the common-mode voltage is driven beyond 1 V within the positive supply allows the amplifier to provide useful operation for signals at either end of the supply voltage range and eliminates the possibility of phase reversal for input signals up to 500 mV beyond either power supply. Offset voltage also changes to reflect the offset of the input pair in control. The transition region is small, approximately 180 mV. These sudden changes in the dc parameters of the input stage can produce glitches that adversely affect distortion.

OVERDRIVING THE INPUT STAGE

Sustained input differential voltages greater than 3.4 V should be avoided as the input transistors can be damaged. Input clamp diodes are recommended if the possibility of this condition exists.

The voltages at the collectors of the input pairs are set to 200 mV from the power supply rails. This allows the amplifier to remain in linear operation for input voltages up to 500 mV beyond the supply voltages. Driving the input common-mode voltage beyond that point will forward bias the collector junction of the input transistor, resulting in phase reversal. Sustaining this condition for any length of time should be avoided because it is easy to exceed the maximum allowed input differential voltage when the amplifier is in phase reversal.

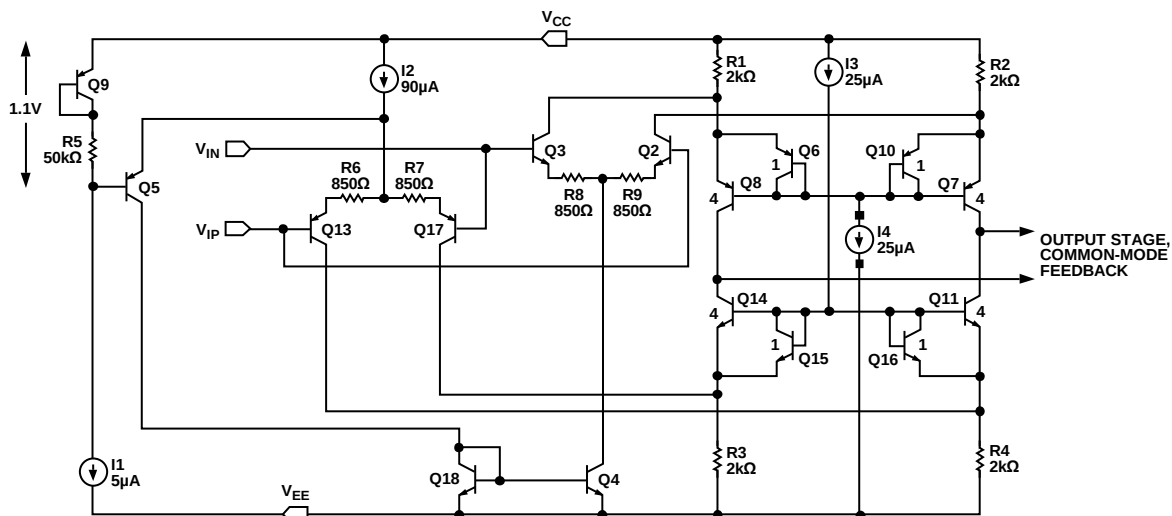


Figure 43. Simplified Schematic of AD8031 Input Stage

01056-043

OUTPUT STAGE, OPEN-LOOP GAIN AND DISTORTION vs. CLEARANCE FROM POWER SUPPLY

The AD8031 features a rail-to-rail output stage. The output transistors operate as common-emitter amplifiers, providing the output drive current as well as a large portion of the amplifier's open-loop gain.

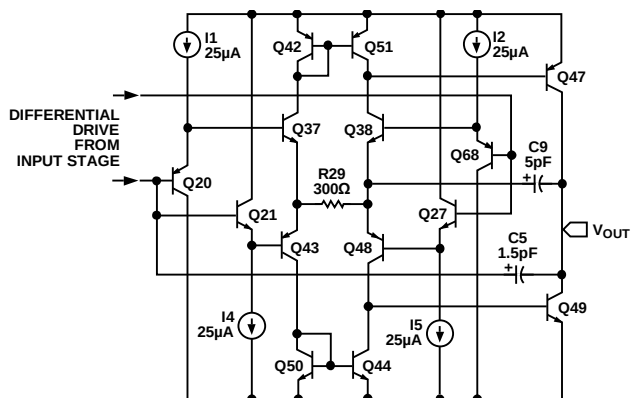


Figure 44. Output Stage Simplified Schematic

The output voltage limit depends on how much current the output transistors are required to source or sink. For applications with low drive requirements (for instance, a unity gain follower driving another amplifier input), the AD8031 typically swings within 20 mV of either voltage supply. As the required current load increases, the saturation output voltage increases linearly as

$$I_{LOAD} \times R_C$$

where:

I_{LOAD} is the required load current.

R_C is the output transistor collector resistance.

For the AD8031, the collector resistances for both output transistors are typically 25 Ω. As the current load exceeds the rated output current of 15 mA, the amount of base drive current required to drive the output transistor into saturation reaches its limit, and the amplifier's output swing rapidly decreases.

The open-loop gain of the AD8031 decreases approximately linearly with load resistance and depends on the output voltage. Open-loop gain stays constant to within 250 mV of the positive power supply, 150 mV of the negative power supply, and then decreases as the output transistors are driven further into saturation.

The distortion performance of the AD8031/AD8032 amplifiers differs from conventional amplifiers. Typically, the distortion performance of the amplifier degrades as the output voltage amplitude increases.

Used as a unity gain follower, the output of the AD8031/AD8032 exhibits more distortion in the peak output voltage region around $V_{CC} - 0.7$ V. This unusual distortion characteristic is caused by the input stage architecture and is discussed in detail in the Input Stage Operation section,

OUTPUT OVERDRIVE RECOVERY

Output overdrive of an amplifier occurs when the amplifier attempts to drive the output voltage to a level outside its normal range. After the overdrive condition is removed, the amplifier must recover to normal operation in a reasonable amount of time. As shown in Figure 45, the AD8031/AD8032 recover within 100 ns from negative overdrive and within 80 ns from positive overdrive.

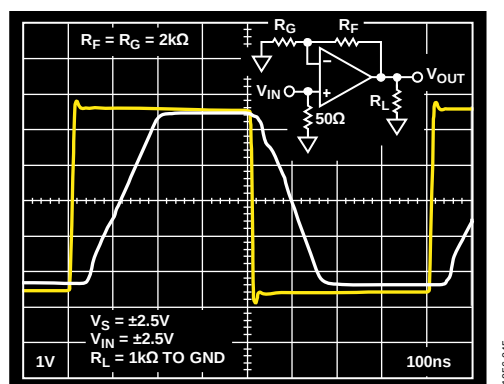


Figure 45. Overdrive Recovery

DRIVING CAPACITIVE LOADS

Capacitive loads interact with an op amp's output impedance to create an extra delay in the feedback path. This reduces circuit stability and can cause unwanted ringing and oscillation. A given value of capacitance causes much less ringing when the amplifier is used with a higher noise gain.

The capacitive load drive of the AD8031/AD8032 can be increased by adding a low valued resistor in series with the capacitive load. Introducing a series resistor tends to isolate the capacitive load from the feedback loop, thereby diminishing its influence. Figure 46 shows the effects of a series resistor on the capacitive drive for varying voltage gains. As the closed-loop gain is increased, the larger phase margin allows for larger capacitive loads with less overshoot. Adding a series resistor at lower closed-loop gains accomplishes the same effect. For large capacitive loads, the frequency response of the amplifier is dominated by the roll-off of the series resistor and capacitive load.

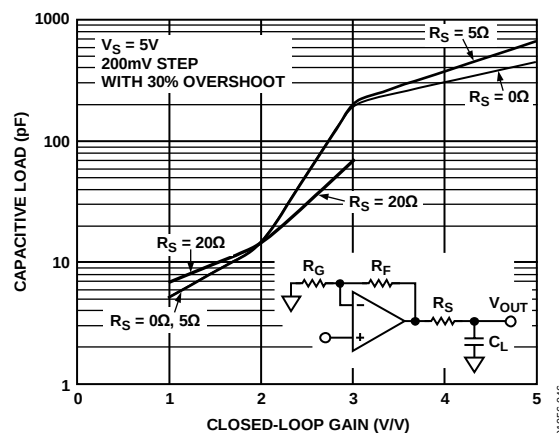


Figure 46. Capacitive Load Drive vs. Closed-Loop Gain

APPLICATIONS

A 2 MHz SINGLE-SUPPLY, BIQUAD BAND-PASS FILTER

Figure 47 shows a circuit for a single-supply, biquad band-pass filter with a center frequency of 2 MHz. A 2.5 V bias level is easily created by connecting the noninverting inputs of all three op amps to a resistor divider consisting of two 1 k Ω resistors connected between 5 V and ground. This bias point is also decoupled to ground with a 0.1 μ F capacitor. The frequency response of the filter is shown in Figure 48.

To maintain an accurate center frequency, it is essential that the op amp have sufficient loop gain at 2 MHz. This requires the choice of an op amp with a significantly higher unity gain, crossover frequency. The unity gain, crossover frequency of the [AD8031/AD8032](#) is 40 MHz. Multiplying the open-loop gain by the feedback factors of the individual op amp circuits yields the loop gain for each gain stage. From the feedback networks of the individual op amp circuits, it can be seen that each op amp has a loop gain of at least 21 dB. This level is high enough to ensure that the center frequency of the filter is not affected by the op amp's bandwidth. If, for example, an op amp with a gain bandwidth product of 10 MHz was chosen in this application, the resulting center frequency would shift by 20% to 1.6 MHz.

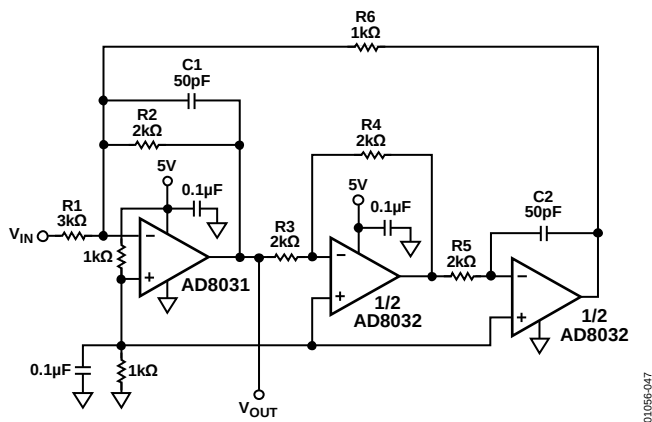


Figure 47. A 2 MHz, Biquad Band-Pass Filter Using AD8031/AD8032

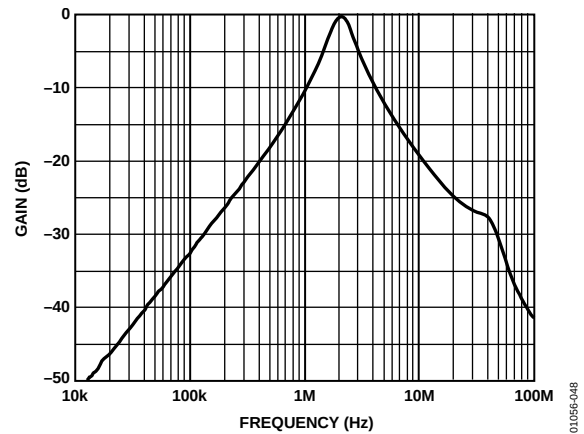


Figure 48. Frequency Response of 2 MHz Band-Pass Filter

HIGH PERFORMANCE, SINGLE-SUPPLY LINE DRIVER

Even though the AD8031/AD8032 swing close to both rails, the AD8031 has optimum distortion performance when the signal has a common-mode level half way between the supplies and when there is about 500 mV of headroom to each rail. If low distortion is required in single-supply applications for signals that swing close to ground, an emitter-follower circuit can be used at the op amp output.

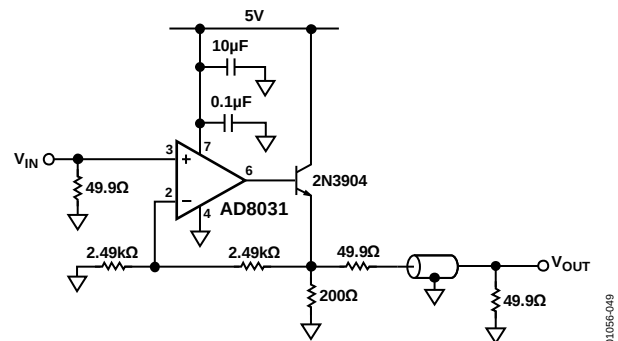


Figure 49. Low Distortion Line Driver for Single-Supply, Ground Referenced Signals

Figure 49 shows the [AD8031](#) configured as a single-supply, gain-of-2 line driver. With the output driving a back-terminated 50 Ω line, the overall gain from V_{IN} to V_{OUT} is unity. In addition to minimizing reflections, the 50 Ω back termination resistor protects the transistor from damage if the cable is short circuited. The emitter follower, which is inside the feedback loop, ensures that the output voltage from the [AD8031](#) stays about 700 mV above ground. Using this circuit, low distortion is attainable even when the output signal swings to within 50 mV of ground. The circuit was tested at 500 kHz and 2 MHz.

Figure 50 and Figure 51 show the output signal swing and frequency spectrum at 500 kHz. At this frequency, the output signal (at V_{OUT}), which has a peak-to-peak swing of 1.95 V (50 mV to 2 V), has a THD of -68 dB (SFDR = -77 dB).

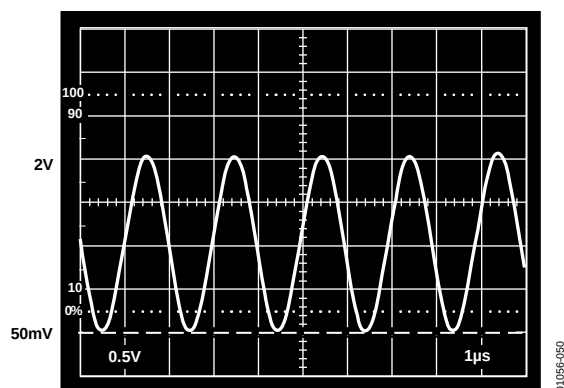


Figure 50. Output Signal Swing of Low Distortion Line Driver at 500 kHz

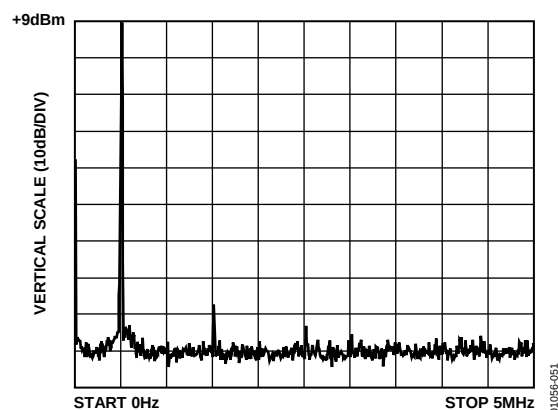


Figure 51. THD of Low Distortion Line Driver at 500 kHz

Figure 52 and Figure 53 show the output signal swing and frequency spectrum at 2 MHz. As expected, there is some degradation in signal quality at the higher frequency. When the output signal has a peak-to-peak swing of 1.45 V (swinging from 50 mV to 1.5 V), the THD is -55 dB (SFDR = -60 dB).

This circuit could also be used to drive the analog input of a single-supply, high speed ADC whose input voltage range is referenced to ground (for example, 0 V to 2 V or 0 V to 4 V). In this case, a back termination resistor is not necessary (assuming a short physical distance from transistor to ADC); therefore, the emitter of the external transistor would be connected directly to the ADC input. The available output voltage swing of the circuit would therefore be doubled.

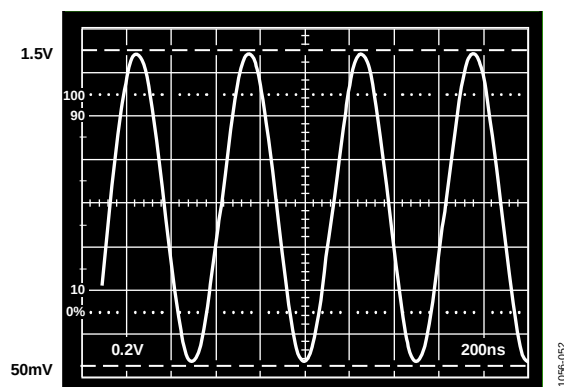


Figure 52. Output Signal Swing of Low Distortion Line Driver at 2 MHz

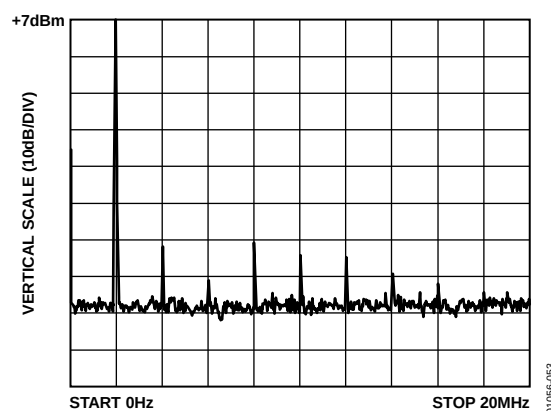
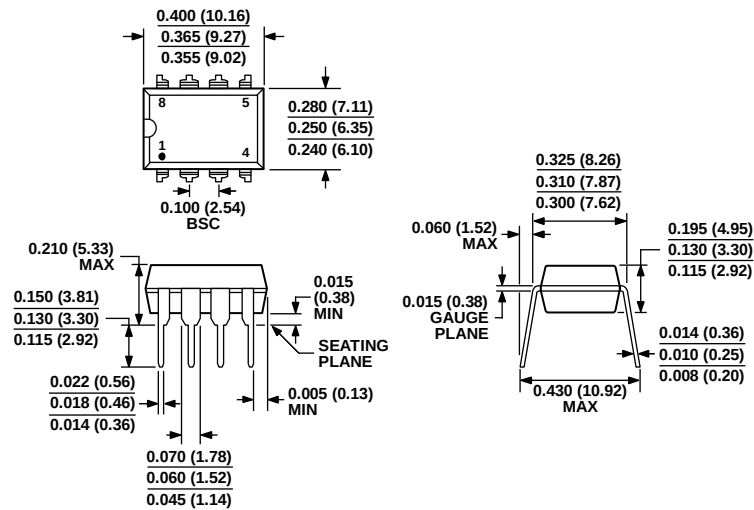


Figure 53. THD of Low Distortion Line Driver at 2 MHz

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001

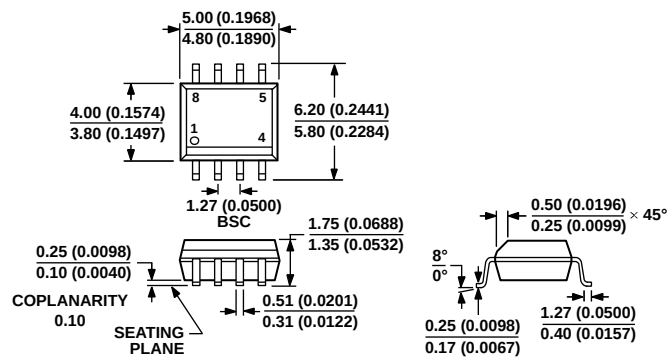
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 54. 8-Lead Plastic Dual In-Line Package [PDIP]

Narrow Body (N-8)

Dimensions shown in inches and (millimeters)

070606-A



COMPLIANT TO JEDEC STANDARDS MS-012-AA

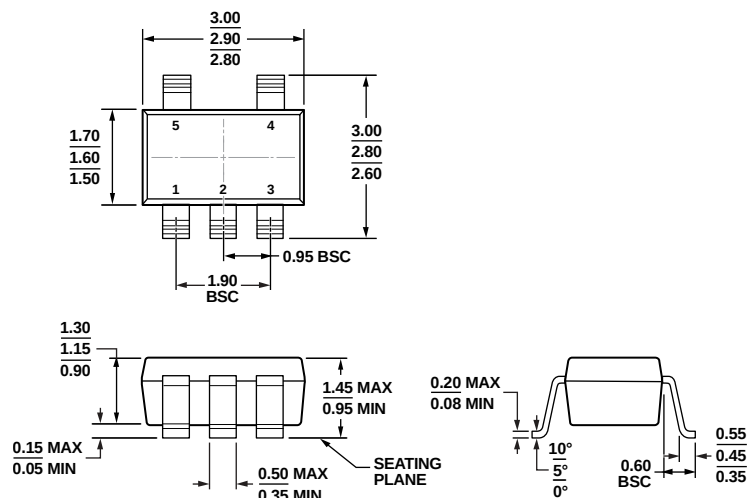
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 55. 8-Lead Standard Small Outline Package [SOIC_N]

Narrow Body (R-8)

Dimensions shown in millimeters and (inches)

012407-A

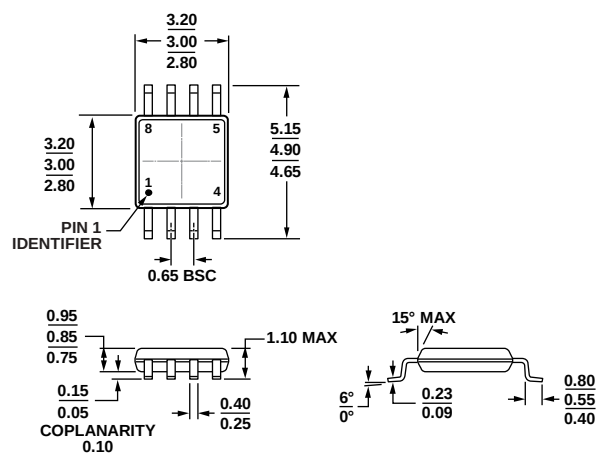


COMPLIANT TO JEDEC STANDARDS MO-178-AA

Figure 56. 5-Lead Small Outline Transistor Package [SOT-23]
(RJ-5)

Dimensions shown in millimeters

11-01-2010-A



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 57. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)

Dimensions shown in millimeters

10-07-2009-B

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Branding
AD8031ANZ	–40°C to +85°C	8-Lead PDIP	N-8	H0A H0A H04 H04 H04
AD8031AR	–40°C to +85°C	8-Lead SOIC_N	R-8	
AD8031ARZ	–40°C to +85°C	8-Lead SOIC_N	R-8	
AD8031ARZ-REEL	–40°C to +85°C	8-Lead SOIC_N, 13" Tape and Reel	R-8	
AD8031ARZ-REEL7	–40°C to +85°C	8-Lead SOIC_N, 7" Tape and Reel	R-8	
AD8031ART-R2	–40°C to +85°C	5-Lead SOT-23	RJ-5	
AD8031ART-REEL7	–40°C to +85°C	5-Lead SOT-23, 7" Tape and Reel	RJ-5	
AD8031ARTZ-R2	–40°C to +85°C	5-Lead SOT-23	RJ-5	
AD8031ARTZ-REEL	–40°C to +85°C	5-Lead SOT-23, 13" Tape and Reel	RJ-5	
AD8031ARTZ-REEL7	–40°C to +85°C	5-Lead SOT-23, 7" Tape and Reel	RJ-5	
AD8031BNZ	–40°C to +85°C	8-Lead PDIP	N-8	
AD8031BR	–40°C to +85°C	8-Lead SOIC_N	R-8	
AD8031BRZ	–40°C to +85°C	8-Lead SOIC_N	R-8	
AD8031BRZ-REEL	–40°C to +85°C	8-Lead SOIC_N, 13" Tape and Reel	R-8	
AD8031BRZ-REEL7	–40°C to +85°C	8-Lead SOIC_N, 7" Tape and Reel	R-8	
AD8031AR-EBZ		8-Lead SOIC Evaluation Board		
AD8031ART-EBZ		5-Lead SOT-23 Evaluation Board		
AD8032ANZ	–40°C to +85°C	8-Lead PDIP	N-8	H9A H9A H9A H9A# H9A# H9A#
AD8032AR	–40°C to +85°C	8-Lead SOIC_N	R-8	
AD8032AR-REEL7	–40°C to +85°C	8-Lead SOIC_N, 7" Tape and Reel	R-8	
AD8032ARZ	–40°C to +85°C	8-Lead SOIC_N	R-8	
AD8032ARZ-REEL	–40°C to +85°C	8-Lead SOIC_N, 13" Tape and Reel	R-8	
AD8032ARZ-REEL7	–40°C to +85°C	8-Lead SOIC_N, 7" Tape and Reel	R-8	
AD8032ARM	–40°C to +85°C	8-Lead MSOP	RM-8	
AD8032ARM-REEL	–40°C to +85°C	8-Lead MSOP, 13" Tape and Reel	RM-8	
AD8032ARM-REEL7	–40°C to +85°C	8-Lead MSOP, 7" Tape and Reel	RM-8	
AD8032ARMZ	–40°C to +85°C	8-Lead MSOP	RM-8	
AD8032ARMZ-REEL	–40°C to +85°C	8-Lead MSOP, 13" Tape and Reel	RM-8	
AD8032ARMZ-REEL7	–40°C to +85°C	8-Lead MSOP, 7" Tape and Reel	RM-8	
AD8032BNZ	–40°C to +85°C	8-Lead PDIP	N-8	
AD8032BR	–40°C to +85°C	8-Lead SOIC_N	R-8	
AD8032BR-REEL7	–40°C to +85°C	8-Lead SOIC_N, 7" Tape and Reel	R-8	
AD8032BRZ	–40°C to +85°C	8-Lead SOIC_N	R-8	
AD8032BRZ-REEL	–40°C to +85°C	8-Lead SOIC_N, 13" Tape and Reel	R-8	
AD8032BRZ-REEL7	–40°C to +85°C	8-Lead SOIC_N, 7" Tape and Reel	R-8	
AD8032ACHIPS		Die		
AD8032AR-EBZ		8-Lead SOIC Evaluation Board		
AD8032ARM-EBZ		8-Lead MSOP Evaluation Board		

¹ Z = RoHS Compliant Part, # denotes lead-free product may be top or bottom marked.