AD570—SPECIFICATIONS

(T_A = +25°C, V+ = +5 V, V– = –12 V or –15 V, all voltages measured with respect to digital common, unless otherwise noted)

Model	AD570J Min	AD570J Typ	AD570J Max	AD570S Min	AD570S Typ	AD570S Max	Units
RESOLUTION[1]			8			8	Bits
RELATIVE ACCURACY							LSB
T_{MIN} to T_{MAX}			**±1/2**			**±1/2**	LSB
FULL-SCALE CALIBRATION		±2			±2		LSB
UNIPOLAR OFFSET			**±1/2**			**±1/2**	LSB
BIPOLAR OFFSET			**±1/2**			**±1/2**	LSB
DIFFERENTIAL NONLINEAIRTY							
T_{MIN} to T_{MAX}	**8**			**8**			Bits
TEMPERATURE RANGE	0		+70	–55		+125	°C
TEMPERATURE COEFFICIENTS							
Unipolar Offset			**±1**			**±1**	LSB
Bipolar Offset			**±1**			**±1**	LSB
Full-Scale Calibration			**±2**			**±2**	LSB
POWER SUPPLY REJECTION							
TTL Positive Supply							
+4.5 V ≤ V + ≤ +5.5 V			**±2**			**±2**	LSB
Negative Supply							
–16.0 V ≤ V – ≤ –13.5 V			**±2**			**±2**	LSB
ANALOG INPUT IMPEDANCE	**3.0**	5.0	7.0	**3.0**	5.0	7.0	kΩ
ANALOG INPUT RANGES							
Unipolar	0		+10	0		+10	V
Bipolar	–5		+5	–5		+5	V
OUTPUT CODING							
Unipolar	Positive True Binary			Positive True Binary			
Bipolar	Positive True Offset Binary			Positive True Offset Binary			
LOGIC OUTPUT							
Output Sink Current							
(V_{OUT} = 0.4 V max, T_{MIN} to T_{MAX})	**3.2**			**3.2**			mA
Output Source Current							
(V_{OUT} = 2.4 V max, T_{MIN} to T_{MAX})	**0.5**			**0.5**			mA
Output Leakage			**±40**			**±40**	µA
LOGIC INPUTS							
Input Current			**±100**			**±100**	µA
Logic "1"	**2.0**			**2.0**			V
Logic "0"			**0.8**			**0.8**	V
CONVERSION TIME	**15**	25	**40**	**15**	25	**40**	µs
POWER SUPPLY							
V+	**+4.5**	+5.0	**+7.0**	**+4.5**	+5.0	**+7.0**	V
V–	**–12.0**	–15	**–16.5**	**–12.0**	–15	**–16.5**	V
OPERATING CURRENT							
V+		7	**15**		7	**15**	mA
V–		9	**15**		9	**15**	mA
PACKAGE OPTION[2]							
Ceramic DIP (D-18)	AD570JD			AD570SD			

NOTES

[1]The AD570 is a selected version of the AD571 10-bit A-to-D converter. Only TTL logic inputs should be connected to Pins 1 and 18 (or no connection made) or damage may result.

[2]For details on grade package offerings for SD-grade in accorance with MIL-STD-883, refer to Analog Devices' Military Products databook or current /883 data sheet.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common . . . . . 0 V to +7 V
V– to Digital Common . . . . . 0 V to –16.5 V
Analog Common to Digital Common . . . . . ±1 V
Analog Input to Analog Common . . . . . ±15 V
Control Inputs . . . . . 0 V to V+
Digital Outputs (Blank Mode) . . . . . 0 V to V+
Power Dissipation. . . . . 800 mW

CIRCUIT DESCRIPTION

The AD570 is a complete 8-bit A/D converter which requires no external components to provide the complete successive-approximation analog-to-digital conversion function. A block diagram of the AD570 is shown on last page. Upon receipt of the $\overline{\text{CONVERT}}$ command, the internal 8-bit current output DAC is sequenced by the I^2L successive-approximation register (SAR) from its most-significant bit (MSB) to least-significant bit (LSB) to provide an output current which accurately balances the input signal current through the 5 kΩ input resistor. The comparator determines whether the addition of each successively-weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is less the bit is left on, if more, the bit is turned off. After testing all the bits, the SAR contains a 8-bit binary code which accurately represents the input signal to within ±1/2 LSB (0.20%).

Upon completion of the sequence, the $\overline{\text{DATA READY}}$ signal goes low, and the bit output lines become active high or low depending on the code in the SAR. When the $\overline{\text{BLANK}}$ and $\overline{\text{CONVERT}}$ line is brought high, the output buffers again go "open", and the SAR is prepared for another conversion cycle.

The temperature compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The bipolar offset input controls a switch which allows the positive bipolar offset current (exactly equal to the value of the MSB less 1/2 LSB)

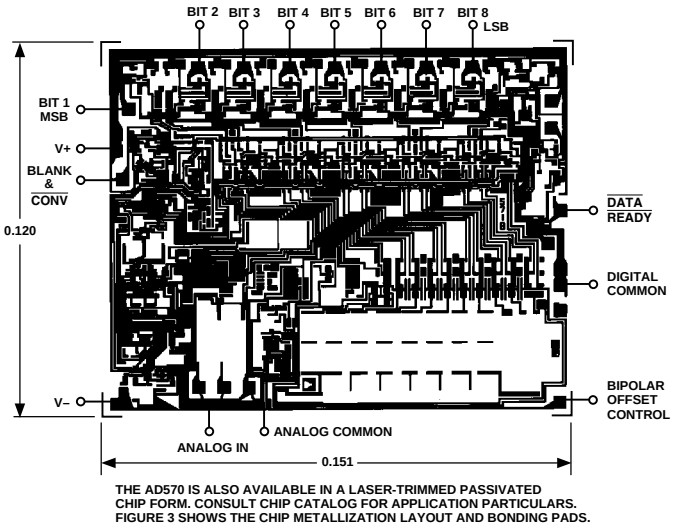


Figure 1. Chip Bonding Diagram

to be injected into the summing (+) node of the comparator to offset the DAC output. Thus the nominal 0 V to +10 V unipolar input range becomes a –5 V to +5 V range. The 5 kΩ thin-film input resistor is trimmed so that with a full-scale input signal, an input current will be generated which exactly matches the DAC output with all bits on. (The input resistor is trimmed slightly low to facilitate user trimming, as discussed on the next page.)

POWER SUPPLY SELECTION

The AD570 is designed and specified for optimum performance using a +5 V and –15 V supply. The supply current drawn by the device is a function of the operating mode (BLANK or CONVERT), as given on the specification page. The supply currents change only moderately over temperature as shown in Figure 2, and do not change significantly with changes in V– from –10.8 volts to –16 volts.

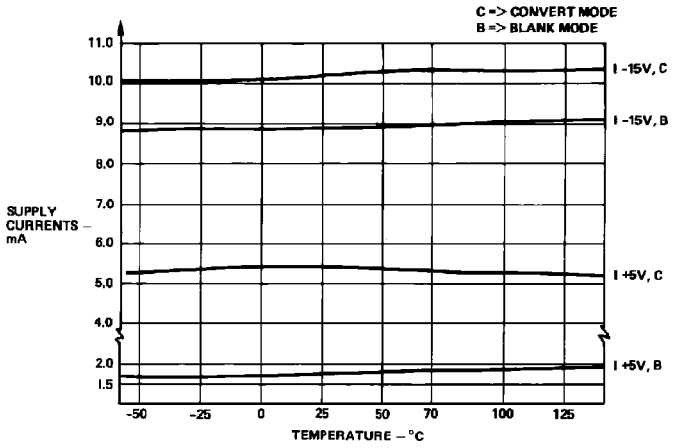


Figure 2. AD570 Power Supply Current vs. Temperature

CONNECTING THE AD570 FOR STANDARD OPERATION

The AD570 contains all the active components required to perform a complete A/D conversion. Thus, for most situations, all that is necessary is to connect the power supply (+5 V and –15 V), the analog input, and the conversion start signal. But, there are some features and special connections which should be considered for achieving optimum performance. The functional pinout is shown in Figure 3.

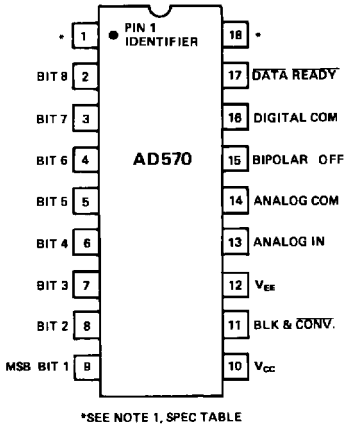


Figure 3. AD570 Pin Connections

FULL-SCALE CALIBRATION

The 5 kΩ thin-film input resistor is laser trimmed to produce a current which matches the full-scale current of the internal DAC—plus about 0.3%—when a full-scale analog input voltage of 9.961 volts (10 volts—1 LSB) is applied at the input. The input resistor is trimmed in this way so that if a fine trimming potentiometer is inserted in series with the input signal, the input current at the full-scale input voltage can be trimmed down to match the DAC full-scale current as precisely as desired. However, for many applications the nominal 9.961 volt full scale can be achieved to sufficient accuracy by simply inserting a 15 Ω resistor in series with the analog input to Pin 13. Typical full-scale calibration error will then be about ±2 LSB or ±0.8%. If a more precise calibration is desired, a 200 Ω trimmer should be used instead. Set the analog input at 9.961 volts, and set the trimmer so that the output code is just at the transition between 11111110 and 11111111. Each LSB will then have a weight of 39.06 mV. If a nominal full scale of 10.24 volts is desired (which makes the LSB have a value of exactly 40.00 mV), a 50 Ω resistor in series with a 200 Ω trimmer (or a 500 Ω trimmer with good resolution) should be used. Of course, larger full-scale ranges can be arranged by using a larger input resistor, but linearity and full-scale temperature coefficient may be compromised if the external resistor becomes a sizable percentage of 5 kΩ.

BIPOLAR OPERATION

The standard unipolar 0 V to +10 V range is obtained by shorting the bipolar offset control pin to digital common. If the pin is left open, the bipolar offset current will be switched into the comparator summing node, giving a –5 V to +5 V range with an

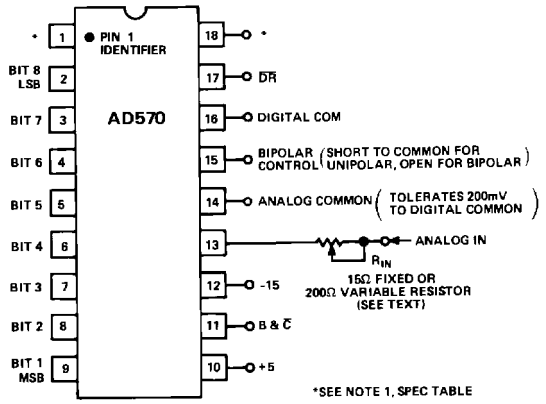


Figure 4. Standard AD570 Connections

offset binary output code. (–5.00 volts in will give a 8-bit code of 00000000; an input of 0.00 volts results in an output code of 10000000 and 4.96 volts at the input yields the 11111111 code.) The bipolar offset control input is not directly TTL compatible, but a TTL interface for logic control can be constructed as shown in Figure 5.

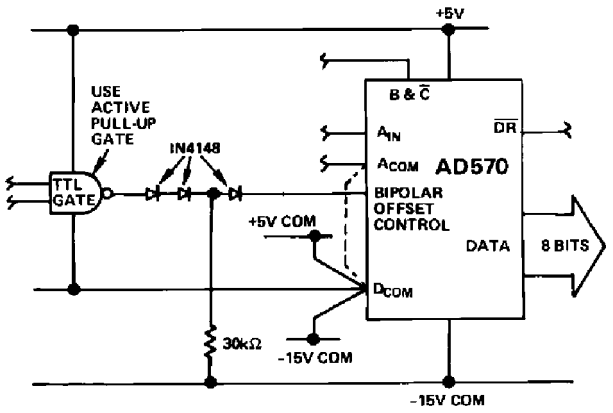


Figure 5. Bipolar Offset Controlled by Logic Gate
Gate Output = 1: Unipolar 0 V–10 V Input Range
Gate Output = 0: Bipolar ±5 V Input Range

COMMON-MODE RANGE

The AD570 provides separate analog and digital common connections. The circuit will operate properly with as much as ±200 mV of common-mode range between the two commons. This permits more flexible control of system common bussing and digital and analog returns.

In normal operation the analog common terminal may generate transient currents of up to 2 mA during a conversion. In addition, a static current of about 2 mA will flow into analog common in the unipolar mode after a conversion is complete. An additional 1 mA will flow in during a blank interval with zero analog input. The analog common current will be modulated by the variations in input signal.

The absolute maximum differential voltage rating between the two commons is ±1 volt. We recommend that a parallel pair of back-to-back protection diodes can be connected as shown in Figure 6 if they are not connected locally.

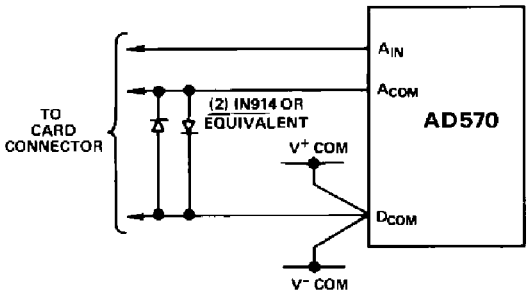


Figure 6. Differential Common Voltage Protection

ZERO OFFSET

The apparent zero point of the AD570 can be adjusted by inserting an offset voltage between the analog common of the device and the actual signal return or signal common. Figure 7 illustrates two methods of providing this offset. Figure 7a shows how the converter zero may be offset by up to ±3 bits to correct the device initial offset and/or input signal offsets. As shown, the circuit gives approximately symmetrical adjustment in unipolar mode. In bipolar mode R2 should be omitted to obtain a symmetrical range.

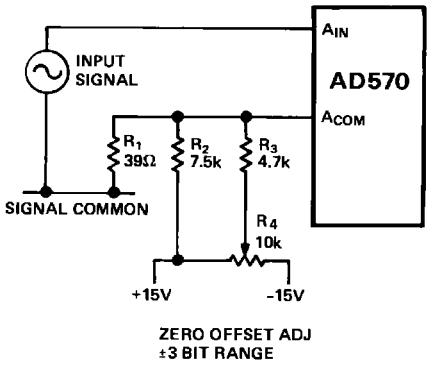


Figure 7a.

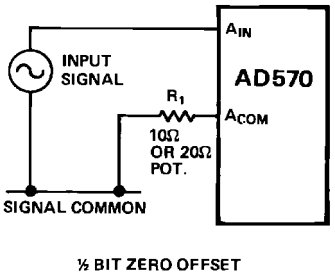


Figure 7b.

Figure 8 shows the nominal transfer curve near zero for an AD570 in unipolar mode. The code transitions are at the edges of the nominal bit weights. In some applications it will be preferable to offset the code transitions so that they fall between the nominal bit weights, as shown in the offset characteristics. This offset can easily be accomplished as shown in Figure 7b.

At balance (after a conversion) approximately 2 mA flows into the analog common terminal. A 10 Ω resistor in series with this terminal will result in approximately the desired 1/2 bit offset of the transfer characteristics. The nominal 2 mA analog common current is not closely controlled in manufacture. If high accuracy is required, a 20 Ω potentiometer (connected as a rheostat) can be used as R1. Additional negative offset range may be obtained by using larger values of R1. Of course, if the zero transition point is changed, the full-scale transition point will also move. Thus, if an offset of 1/2 LSB is introduced, full-scale trimming as described on previous page should be done with an analog input of 9.941 volts.

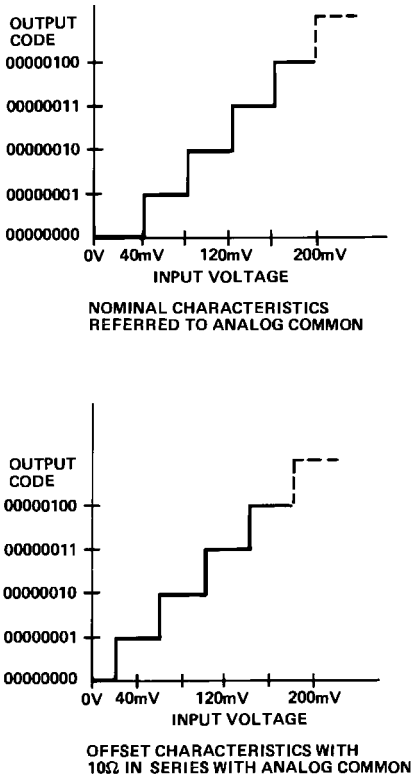


Figure 8. AD570 Transfer Curve—Unipolar Operation (Approximate Bit Weights Shown for Illustration, Nominal Bit Weights ~ 36.1 mV)

NOTE: During a conversion transient currents from the analog common terminal will disturb the offset voltage. Capacitive decoupling should not be used around the offset network. These transients will settle as appropriate during a conversion. Capacitive decoupling will "pump up" and fail to settle resulting in conversion errors. Power supply decoupling which returns to analog signal common should go to the signal input side of the resistive offset network.

CONTROL AND TIMING OF THE AD570

There are several important timing and control features on the AD570 which must be understood precisely to allow optimal interfacing to microprocessor or other types of control systems. All of these features are shown in the timing diagram in Figure 9.

The normal standby situation is shown at the left end of the drawing. The BLANK and $\overline{\text{CONVERT}}$ (B & $\overline{\text{C}}$) line is held high, the output lines will be "open", and the $\overline{\text{DATA READY}}$ ($\overline{\text{DR}}$) line will be high. This mode is the lowest power state of the device (typically 150 mW). When the (B & $\overline{\text{C}}$) line is brought low, the conversion cycle is initiated; but the $\overline{\text{DR}}$ and data lines do not change state. When the conversion cycle is complete (typically 25 µs), the $\overline{\text{DR}}$ line goes low, and within 500 ns, the data lines become active with the new data.

About 1.5 µs after the B & $\overline{\text{C}}$ line is again brought high, the $\overline{\text{DR}}$ line will go high and the data lines will go open. When the B & $\overline{\text{C}}$ line is again brought low, a new conversion will begin. The minimum pulse width for the B & $\overline{\text{C}}$ line to blank previous data and start a new conversion is 2 µs. If the B & $\overline{\text{C}}$ line is brought high during a conversion, the conversion will stop, and

the $\overline{DR}$ and data lines will not change. If a 2 µs or longer pulse is applied to the B & $\overline{C}$ line during a conversion, the converter will clear and start a new conversion cycle.

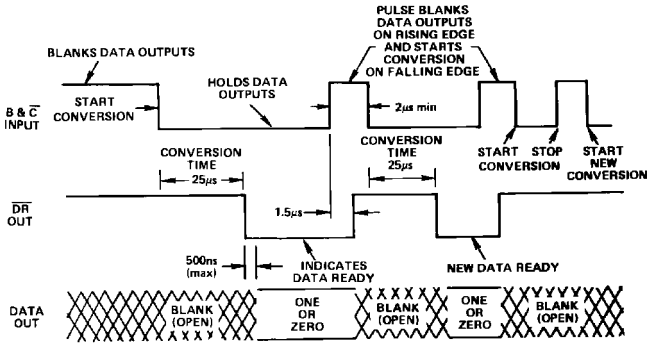


Figure 9. AD570 Timing and Control Sequence

CONTROL MODES WITH BLANK AND $\overline{CONVERT}$

The timing sequence of the AD570 discussed above allows the device to be easily operated in a variety of systems with differing control modes. The two most common control modes, the Convert Pulse Mode, and the Multiplex Mode, are illustrated here.

Convert Pulse Mode–In this mode, data is present at the output of the converter at all times except when conversion is taking place. Figure 10 illustrates the timing of this mode. The BLANK and $\overline{CONVERT}$ line is normally low and conversions are triggered by a positive pulse. A typical application for this timing mode is shown in Figure 13, in which µP bus interfacing is easily accomplished with three-state buffers.

Multiplex Mode—In this mode the outputs are blanked except when the device is selected for conversion and readout; this timing is shown in Figure 11. A typical AD570 multiplexing application is shown in Figure 14.

This operating mode allows multiple AD570 devices to drive common data lines. All BLANK and $\overline{CONVERT}$ lines are held high to keep the outputs blanked. A single AD570 is selected, its BLANK and $\overline{CONVERT}$ line is driven low and at the end of conversion, which is indicated by $\overline{DATA\ READY}$ going low, the conversion result will be present at the outputs. When this data has been read from the 8-bit bus, BLANK and $\overline{CONVERT}$ is restored to the blank mode to clear the data bus for other converters. When several AD570s are multiplexed in sequence, a new conversion may be started in one AD570 while data is being read from another. As long as the data is read and the first AD570 is cleared within 15 µs after the start of conversion of the second AD570, no data overlap will occur.

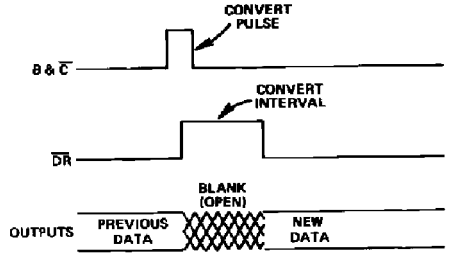


Figure 10. Convert Pulse Mode

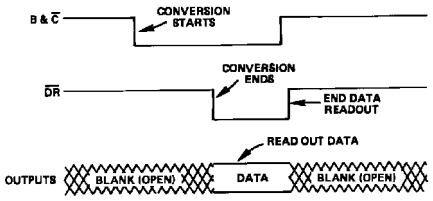


Figure 11. Multiplex Mode

SAMPLE-HOLD AMPLIFIER CONNECTION TO THE AD570

Many situations in high-speed acquisition systems or digitizing of rapidly changing signals require a sample-hold amplifier (SHA) in front of the A-D converter. The SHA can acquire and hold a signal faster than the converter can perform a conversion. A SHA can also be used to accurately define the exact point in time at which the signal is sampled. For the AD570, a SHA can also serve as a high input impedance buffer.

Figure 12 shows the AD570 connected to the AD582 monolithic SHA for high speed signal acquisition. In this configuration, the AD582 will acquire a 10 volt signal in less than 10 µs with a droop rate less than 100 µV/ms. The control signals are arranged so that when the control line goes low, the AD582 is put into the "hold" mode, and the AD570 will begin its conversion cycle. (The AD582 settles to final value well in advance of the

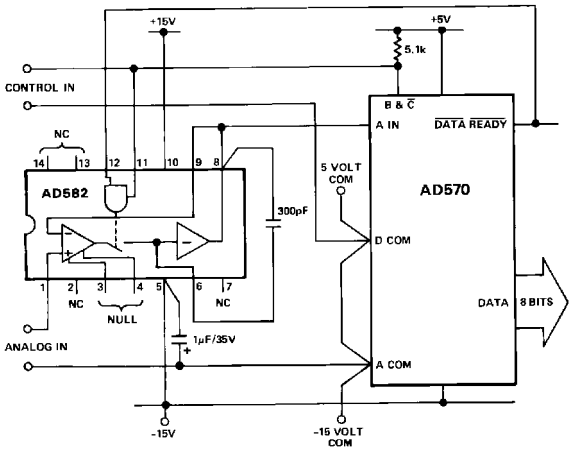


Figure 12. Sample-Hold Interface to the AD570

first comparator decision inside the AD570). The $\overline{DATA\ READY}$ line is fed back to the other side of the differential input control gate so that the AD582 cannot come out of the "hold" mode during the conversion cycle. At the end of the conversion cycle, the $\overline{DATA\ READY}$ line goes low, automatically placing the AD582 back into the sample mode. This feature allows simple control of both the SHA and the A-D converter with a single line. Observe carefully the ground, supply, and bypass capacitor connections between the two devices. The arrangement minimizes ground noise and interference during the conversion cycle to give the most accurate measurements.

INTERFACING THE AD570 TO A MICROPROCESSOR

The AD570 can easily be arranged to be driven from standard microprocessor control lines and to present data to any standard microprocessor bus (4-, 8-, 12- or 16-bit) with a minimum of additional control components. The configuration shown in Figure 13 is designed to operate with an 8-bit bus and standard 8080 control signals.

The input control circuitry shown is required to ensure that the AD570 receives a sufficiently long B & $\overline{C}$ input pulse. When the converter is ready to start a new conversion, the B & C line is low, and $\overline{DR}$ is low. To command a conversion, the start address decode line goes low, followed by $\overline{WR}$. The B & $\overline{C}$ line will now go high, followed about 1.5 µs later by $\overline{DR}$. This resets the external flip-flop and brings B & $\overline{C}$ back to low, which initiates the conversion cycle. At the end of the conversion cycle, the $\overline{DR}$ line goes low, the data outputs will become active with the new data and the control lines will return to the standby state. The new data will remain active until a new conversion is commanded. The self-pulsing nature of this circuit guarantees a sufficient convert pulse width.

This new data can now be presented to the data bus by enabling the three-state buffers when desired. An 8-bit data word is loaded onto the bus when its decoded address goes low and the $\overline{RD}$ line goes low. Polling the converter to determine if conversion is complete can be done by addressing the

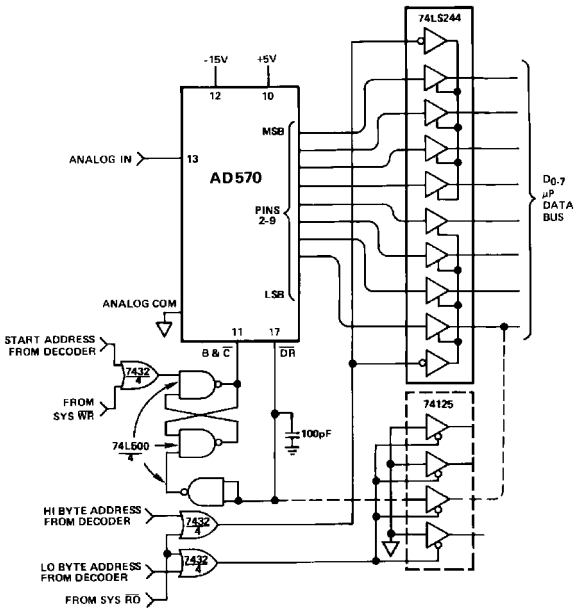


Figure 13. Interfacing AD570 to an 8-Bit Bus (8080 Control Structure)

gate (shown dotted) which buffers the $\overline{DR}$ line, if desired. In this configuration, there is no need for additional buffer register storage. The data is stored indefinitely in the, since the B & $\overline{C}$ line is continually held low.

BUS INTERFACING WITH A PERIPHERAL INTERFACE CIRCUIT

An improved technique for interfacing to a µP bus involves the use of special peripheral interfacing circuits (or I/O devices), such as the MC6821 Peripheral Interface Adapter (PIA). Shown in Figure 14 is a straightforward application of a PIA to multiplex up to 10 AD570 circuits. The AD570 has 3-state outputs, hence the data bit outputs can be paralleled, provided that only one converter at a time is permitted to be the active state. The $\overline{DATA\ READY}$ output of the AD570 is an open collector with resistor pull-up, thus several $\overline{DR}$ lines can be wire-ORed to allow indication of the status of the selected device. One of the 8-bit ports of the PIA is programmed as an 8-bit input port. The 8-bits of the second port are programmed as outputs, and along with the 2 control bits (which act as outputs), are used to control the 10 AD570s. When a control line is in the "1" or high state, the ADC will be automatically blanked. That is, its outputs will be in the inactive open state. If a single control line is switched low, its ADC will convert and the outputs will automatically go active when the conversion is complete. The result can then be read from port A. When the next conversion is desired, a different control line can be switched to zero, blanking the previously active port at the same time. Subsequently, this second device can be read by the microprocessor, and so-forth. The status lines are wire-ORed in 2 groups and connected to the two remaining control pins. This allows a conversion status check to be made after a convert command, if necessary. The ADCs are divided into two groups to minimize the loading effect of the internal pull-up resistors on the $\overline{DATA\ READY}$ buffers. See the MC6821 data sheet for more application detail.

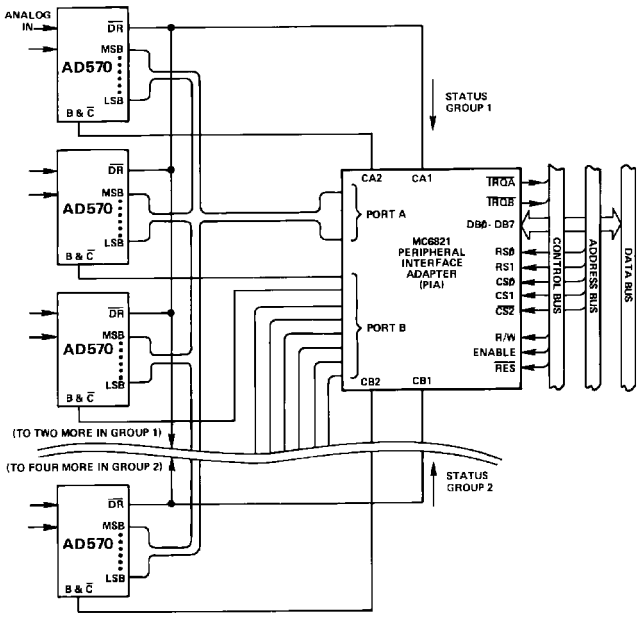
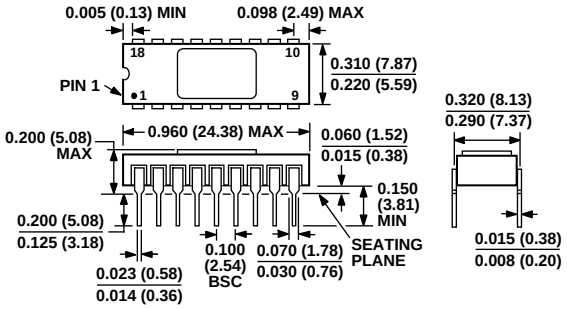


Figure 14. Multiplexing 10 AD570s Using Single PIA for µP Interface. No Other Logic Required (6800 Control Structure)

OUTLINE DIMENSIONS



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 15. 18-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP] (D-18)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
5962-8680201VA	−55°C to +125°C	18-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-18
AD570JD	0°C to 70°C	18-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-18
AD570SD	−55°C to +125°C	18-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-18
AD570SD/883B	−55°C to +125°C	18-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-18

REVISION HISTORY

4/12—Rev. A to Rev. B

Changed V+ Operating Current Maximum Parameter from 10 mA to 15 mA 2
Updated Outline Dimensions 8
Added Ordering Guide 8

3/86—Rev. 0 to Rev. A

D10741-0-4/12(B)