TABLE OF CONTENTS

REVISION HISTORY

3/13—Rev. C to Rev. D

Added $t_{\overline{WP}}$; Table 2 ... 5
Changes to Ordering Guide ... 27

1/07—Rev. B to Rev. C

Updated Format ... Universal
Changes to Dynamic Characteristics Specifications ... 4
Changes to Table 2 Footnote ... 5
Changes to Table 3 ... 7
Changes to Ordering Guide ... 27

9/04—Rev. A to Rev. B

Updated Format ... Universal
Changes to Table 20 ... 23
Changes to Resistance Scaling Section ... 25
Changes to Ordering Guide ... 27

5/04—Rev. 0 to Rev. A

Updated formatting ... Universal
Edits to Features, General Description, and Block Diagram ... 1
Changes to Specifications ... 3
Replaced Timing Diagrams ... 6
Changes to Pin Function Descriptions ... 8
Changes to Typical Performance Characteristics ... 9
Changes to Test Circuits ... 13
Edits to Theory of Operation ... 14
Edits to Applications ... 23
Updated Outline Dimensions ... 27

12/01—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—10 kΩ, 50 kΩ, 100 kΩ VERSIONS

V_{DD} = 3 V ± 10% or 5 V ± 10%, V_{SS} = 0 V, $V_A = V_{DD}$, V_B = 0 V, −40°C < T_A < +85°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS— RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = NC, monotonic	−1	±1/2	+1.8	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = NC	−0.2		+0.2	LSB
Nominal Resistor Tolerance	$\Delta R_{AB}/R_{AB}$	D = 0x3FF	−40		+20	%
Resistance Temperature Coefficient	$(\Delta R_{WB}/R_{WB})/\Delta T \times 10^6$			600		ppm/°C
Wiper Resistance	R_W	I_W = 100 µA, V_{DD} = 5.5 V, code = half scale		15	100	Ω
		I_W = 100 µA, V_{DD} = 3 V, code = half scale		50		Ω
DC CHARACTERISTICS— POTENTIOMETER DIVIDER MODE						
Resolution	N				10	Bits
Differential Nonlinearity[3]	DNL	Monotonic, T_A = 25°C	−1	±1/2	+1	LSB
		Monotonic, T_A = −40°C or +85°C	−1		+1.25	LSB
Integral Nonlinearity[3]	INL		−0.4		+0.4	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = half scale		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = full scale	−3		0	% FS
Zero-Scale Error	V_{WZSE}	Code = zero scale	0		1.5	% FS
RESISTOR TERMINALS						
Terminal Voltage Range[4]	$V_{A, B, W}$		V_{SS}		V_{DD}	V
Capacitance A, B[5]	$C_{A, B}$	f = 1 MHz, measured to GND, code = half-scale		50		pF
Capacitance W[5]	C_W	f = 1 MHz, measured to GND, code = half-scale		50		pF
Common-Mode Leakage Current[5, 6]	I_{CM}	$V_W = V_{DD}/2$		0.01	1	µA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	With respect to GND, V_{DD} = 5 V	2.4			V
Input Logic Low	V_{IL}	With respect to GND, V_{DD} = 5 V			0.8	V
Input Logic High	V_{IH}	With respect to GND, V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	With respect to GND, V_{DD} = 3 V			0.6	V
Input Logic High	V_{IH}	With respect to GND, V_{DD} = +2.5 V, V_{SS} = −2.5 V	2.0			V
Input Logic Low	V_{IL}	With respect to GND, V_{DD} = +2.5 V, V_{SS} = −2.5 V			0.5	V
Output Logic High (SDO, RDY)	V_{OH}	$R_{PULL-UP}$ = 2.2 kΩ to 5 V (see Figure 26)	4.9			V
Output Logic Low	V_{OL}	I_{OL} = 1.6 mA, V_{LOGIC} = 5 V (see Figure 26)			0.4	V
Input Current	I_{IL}	$V_{IN} = 0$ V or V_{DD}			±2.5	µA
Input Capacitance[5]	C_{IL}			4		pF
Output Current[5]	I_{O1}, I_{O2}	V_{DD} = 5 V, V_{SS} = 0 V, T_A = 25°C		50		mA
		V_{DD} = 2.5 V, V_{SS} = 0 V, T_A = 25°C		7		mA

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
POWER SUPPLIES						
Single-Supply Power Range	V_{DD}	V_{SS} = 0 V	2.7		5.5	V
Dual-Supply Power Range	V_{DD}/V_{SS}		±2.25		±2.75	V
Positive Supply Current	I_{DD}	$V_{IH} = V_{DD}$ or V_{IL} = GND		2.7	10	µA
Negative Supply Current	I_{SS}	$V_{IH} = V_{DD}$ or V_{IL} = GND, V_{DD} = +2.5 V, V_{SS} = −2.5 V		0.5	10	µA
EEMEM Store Mode Current	I_{DD} (store)	$V_{IH} = V_{DD}$ or V_{IL} = GND, V_{SS} = GND, $I_{SS} \approx 0$		40		mA
	I_{SS} (store)	V_{DD} = +2.5 V, V_{SS} = −2.5 V		−40		mA
EEMEM Restore Mode Current[7]	I_{DD} (restore)	$V_{IH} = V_{DD}$ or V_{IL} = GND, V_{SS} = GND, $I_{SS} \approx 0$	0.3	3	9	mA
	I_{SS} (restore)	V_{DD} = +2.5 V, V_{SS} = −2.5 V	−0.3	−3	−9	mA
Power Dissipation[8]	P_{DISS}	$V_{IH} = V_{DD}$ or V_{IL} = GND		0.018	0.05	mW
Power Supply Sensitivity[5]	P_{SS}	ΔV_{DD} = 5 V ± 10%		0.002	0.01	%/%
DYNAMIC CHARACTERISTICS[5, 9]						
Bandwidth	BW	−3 dB, R_{AB} = 10 kΩ/50 kΩ/ 100 kΩ		370/85/44		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz, R_{AB} = 10 kΩ		0.045		%
		V_A = 1 V rms, V_B = 0 V, f = 1 kHz, R_{AB} = 50 kΩ, 100 kΩ		0.022		%
V_W Settling Time	t_S	$V_A = V_{DD}$, V_B = 0 V, V_W = 0.50% error band, Code 0x000 to 0x200 for R_{AB} = 10 kΩ/50 kΩ/100 kΩ		1.2/3.7/7		µs
Resistor Noise Voltage	e_{N_WB}	R_{WB} = 5 kΩ, f = 1 kHz		9		nV/√Hz

[1] Typical values represent average readings at 25°C and V_{DD} = 5 V.
[2] Resistor position nonlinearity error (R-INL) is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. I_W ~ 50 µA @ V_{DD} = 2.7 V and I_W ~ 400 µA @ V_{DD} = 5 V for the R_{AB} = 10 kΩ version, I_W ~ 50 µA for the R_{AB} = 50 kΩ, and I_W ~ 25 µA for the R_{AB} = 100 kΩ version (see Figure 26).
[3] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output DAC. $V_A = V_{DD}$ and $V_B = V_{SS}$. DNL specification limits of −1 LSB minimum are guaranteed monotonic operating condition (see Figure 27).
[4] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other. Dual-supply operation enables ground-referenced bipolar signal adjustment.
[5] Guaranteed by design and not subject to production test.
[6] Common-mode leakage current is a measure of the dc leakage from any Terminal B–W to a common-mode bias level of $V_{DD}/2$.
[7] EEMEM restore mode current is not continuous. Current consumed while EEMEM locations are read and transferred to the RDAC register (see Figure 23). To minimize power dissipation, a NOP Instruction 0 (0x0) should be issued immediately after Instruction 1 (0x1).
[8] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$) + ($I_{SS} \times V_{SS}$).
[9] All dynamic characteristics use V_{DD} = +2.5 V and V_{SS} = −2.5 V.

TIMING CHARACTERISTICS—10 kΩ, 50 kΩ, 100 kΩ VERSIONS

V_{DD} = 3 V to 5.5 V, V_{SS} = 0 V, and −40°C < T_A < +85°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
INTERFACE TIMING CHARACTERISTICS[2, 3]						
Clock Cycle Time (t_{CYC})	t_1		20			ns
$\overline{CS}$ Setup Time	t_2		10			ns
CLK Shutdown Time to $\overline{CS}$ Rise	t_3		1			t_{CYC}
Input Clock Pulse Width	t_4, t_5	Clock level high or low	10			ns
Data Setup Time	t_6	From positive CLK transition	5			ns
Data Hold Time	t_7	From positive CLK transition	5			ns
$\overline{CS}$ to SDO-SPI Line Acquire	t_8				40	ns
$\overline{CS}$ to SDO-SPI Line Release	t_9				50	ns
CLK to SDO Propagation Delay[4]	t_{10}	R_P = 2.2 kΩ, C_L < 20 pF			50	ns
CLK to SDO Data Hold Time	t_{11}	R_P = 2.2 kΩ, C_L < 20 pF	0			ns
$\overline{CS}$ High Pulse Width[5]	t_{12}		10			ns
$\overline{CS}$ High to $\overline{CS}$ High[5]	t_{13}		4			t_{CYC}
RDY Rise to $\overline{CS}$ Fall	t_{14}		0			ns
$\overline{CS}$ Rise to RDY Fall Time	t_{15}			0.1	0.15	ms
Store/Read EEMEM Time[6]	t_{16}	Applies to instructions 0x2, 0x3, and 0x9		25		ms
Power-On EEMEM Restore Time	t_{EEMEM1}	R_{AB} = 10 kΩ		140		µs
Dynamic EEMEM Restore Time	t_{EEMEM2}	R_{AB} = 10 kΩ		140		µs
$\overline{WP}$ High or Low to $\overline{CS}$ Fall Time	$t_{\overline{WP}}$			40		ns
$\overline{CS}$ Rise to Clock Rise/Fall Setup	t_{17}		10			ns
Preset Pulse Width (Asynchronous)	t_{PRW}	Not shown in timing diagram	50			ns
Preset Response Time to Wiper Setting	t_{PRESP}	$\overline{PR}$ pulsed low to refresh wiper positions		70		µs
FLASH/EE MEMORY RELIABILITY						
Endurance[7]			100			kCycles
Data Retention[8]				100		Years

[1] Typical values represent average readings at 25°C and V_{DD} = 5 V.
[2] Guaranteed by design and not subject to production test.
[3] See timing diagrams (Figure 3 and Figure 4) for location of measured values. All input control voltages are specified with $t_R = t_F$ = 2.5 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V. Switching characteristics are measured using both V_{DD} = 3 V and V_{DD} = 35 V.
[4] Propagation delay depends on the value of V_{DD}, $R_{PULL-UP}$, and C_L.
[5] Valid for commands that do not activate the RDY pin.
[6] RDY pin low only for Instructions 2, 3, 8, 9, 10, and the $\overline{PR}$ hardware pulse: CMD_2, 3 ~ 20 ms; CMD_8 ~ 1 ms; CMD_9, 10 ~ 0.12 ms. Device operation at T_A = −40°C and V_{DD} < 3 V extends the EEMEM store time to 35 ms.
[7] Endurance is qualified to 100,000 cycles per JEDEC Standard 22, Method A117 and measured at −40°C, +25°C, and +85°C; typical endurance at +25°C is 700,000 cycles.
[8] Retention lifetime equivalent at junction temperature (T_J) = 55°C per JEDEC Standard 22, Method A117. Retention lifetime based on an activation energy of 0.6 eV derates with junction temperature, as shown in Figure 45 in the Flash/EEMEM Reliability section.

Timing Diagrams

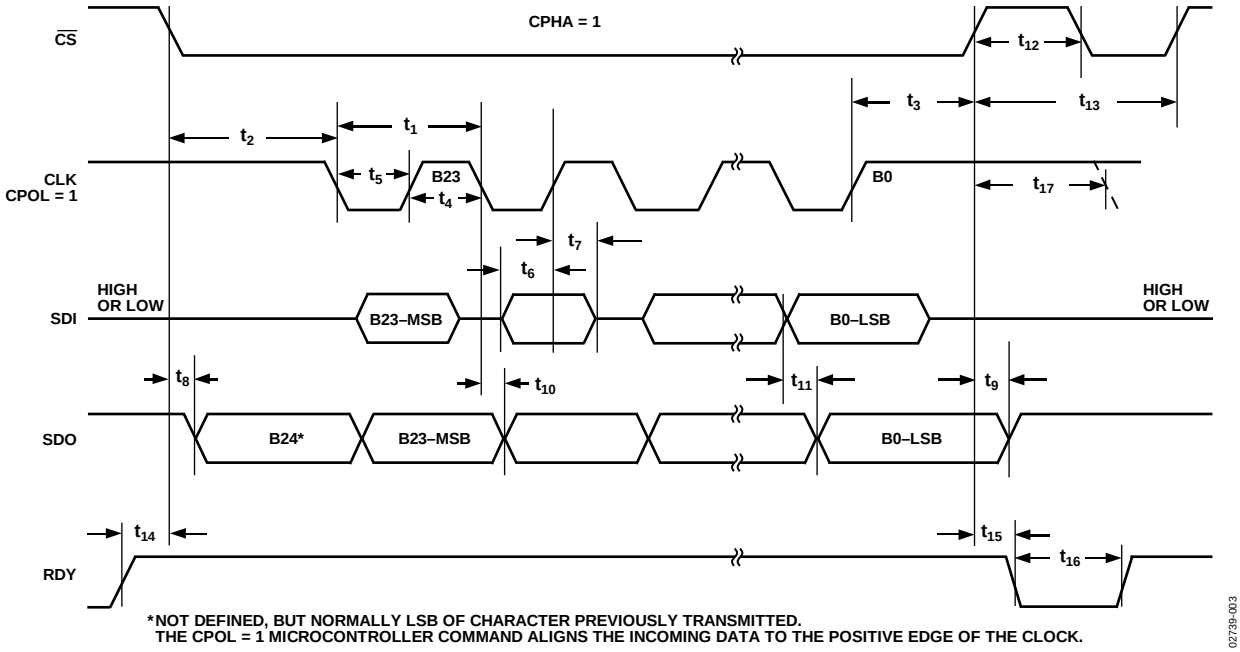

Figure 3. CPHA = 1 Timing Diagram

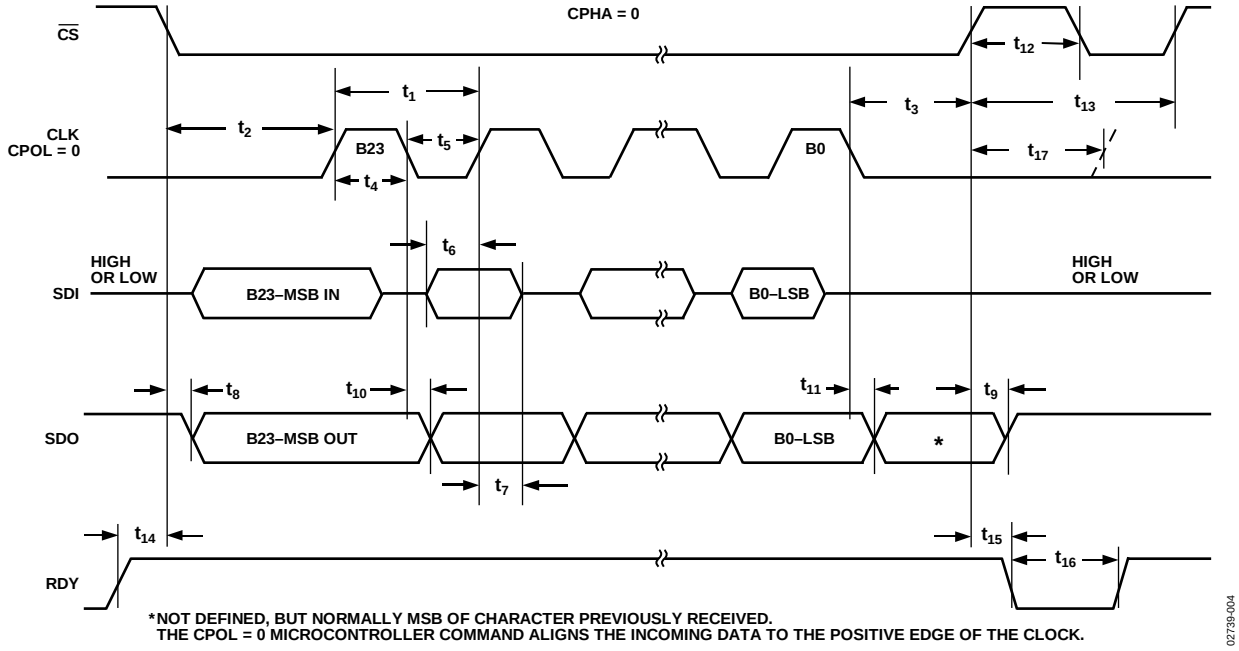

Figure 4. CPHA = 0 Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameters	Ratings
V_{DD} to GND	−0.3 V, +7 V
V_{SS} to GND	+0.3 V, −7 V
V_{DD} to V_{SS}	7 V
V_A, V_B, V_W to GND	V_{SS} − 0.3 V, V_{DD} + 0.3 V
A–B, A–W, B–W	
Intermittent[1]	±20 mA
Continuous	±2 mA
Digital Input and Output Voltage to GND	−0.3 V, V_{DD} + 0.3 V
Operating Temperature Range[2]	−40°C to +85°C
Maximum Junction Temperature (T_J max)	150°C
Storage Temperature	−65°C to +150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	20 sec to 40 sec
Thermal Resistance	150°C/W
Junction-to-Ambient (θ_{JA}),TSSOP-16	
Junction-to-Case (θ_{JC}), TSSOP-16	28°C/W
Package Power Dissipation	(T_J max − T_A)/θ_{JA}

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.
[2] Includes programming of nonvolatile memory.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

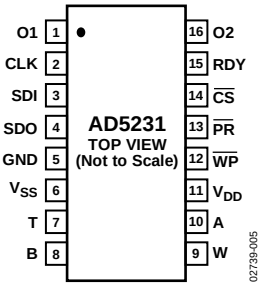

Figure 5. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	O1	Nonvolatile Digital Output 1. ADDR = 0x1, data bit position D0. For example, to store O1 high, the data bit format is 0x310001.
2	CLK	Serial Input Register Clock Pin. Shifts in one bit at a time on positive clock edges.
3	SDI	Serial Data Input Pin. Shifts in one bit at a time on positive clock CLK edges. MSB loaded first.
4	SDO	Serial Data Output Pin. Serves readback and daisy-chain functions. Command 9 and Command 10 activate the SDO output for the readback function, delayed by 24 or 25 clock pulses, depending on the clock polarity before and after the data-word (see Figure 3, Figure 4, and Table 7). In other commands, the SDO shifts out the previously loaded SDI bit pattern, delayed by 24 or 25 clock pulses depending on the clock polarity (see Figure 3 and Figure 4). This previously shifted-out SDI can be used for daisy-chaining multiple devices. Whenever SDO is used, a pull-up resistor in the range of 1 kΩ to 10 kΩ is needed.
5	GND	Ground Pin. Logic ground reference.
6	V_{SS}	Negative Supply. Connect to 0 V for single-supply applications. If V_{SS} is used in dual-supply applications, it must be able to sink 40 mA for 25 ms when storing data to EEMEM.
7	T	Reserved for factory testing. Connect to V_{DD} or V_{SS}.
8	B	Terminal B of RDAC.
9	W	Wiper Terminal of RDAC. ADDR (RDAC) = 0x0.
10	A	Terminal A of RDAC.
11	V_{DD}	Positive Power Supply Pin.
12	$\overline{WP}$	Optional Write Protect Pin. When active low, $\overline{WP}$ prevents any changes to the present contents, except $\overline{PR}$ and Instruction 1 and Instruction 8 and refreshes the RDAC register from EEMEM. Execute a NOP instruction before returning to $\overline{WP}$ high. Tie $\overline{WP}$ to V_{DD}, if not used.
13	$\overline{PR}$	Optional Hardware Override Preset Pin. Refreshes the scratchpad register with current contents of the EEMEM register. Factory default loads midscale 512_{10} until EEMEM is loaded with a new value by the user. $\overline{PR}$ is activated at the logic high transition. Tie $\overline{PR}$ to V_{DD}, if not used.
14	$\overline{CS}$	Serial Register Chip Select Active Low. Serial register operation takes place when $\overline{CS}$ returns to logic high.
15	RDY	Ready. Active-high open-drain output. Identifies completion of Instructions 2, 3, 8, 9, 10, and $\overline{PR}$.
16	O2	Nonvolatile Digital Output 2. ADDR = 0x1, data bit position D1. For example, to store O2 high, the data bit format is 0x310002.

TYPICAL PERFORMANCE CHARACTERISTICS

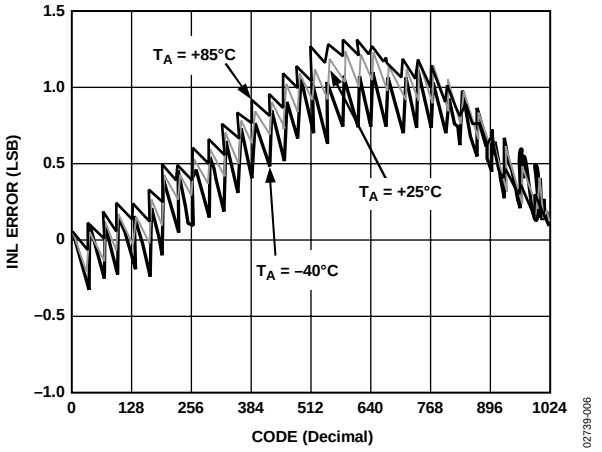

Figure 6. INL vs. Code, T_A = –40°C, +25°C, +85°C Overlay, R_{AB} = 10 kΩ

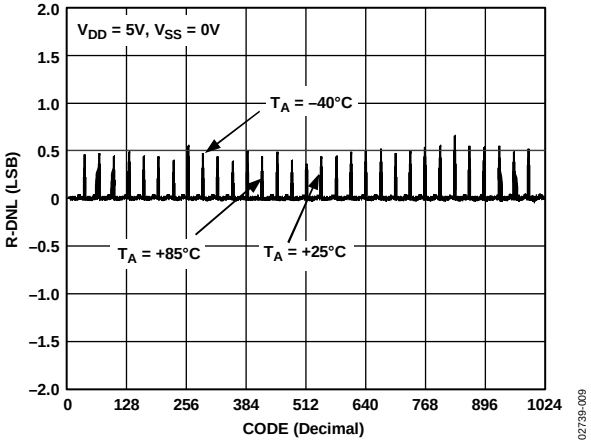

Figure 9. R-DNL vs. Code, T_A = –40°C, +25°C, +85°C Overlay, R_{AB} = 10 kΩ

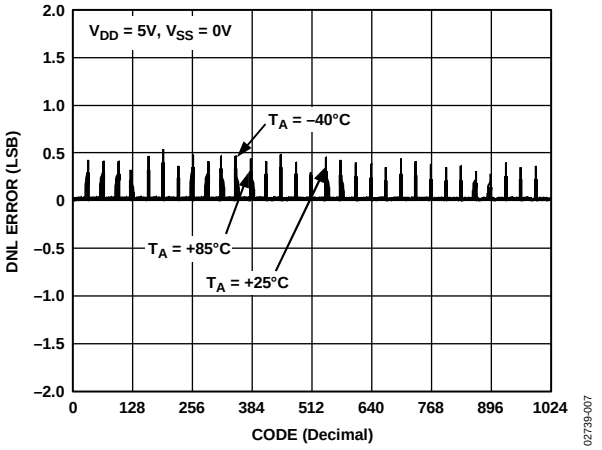

Figure 7. DNL vs. Code, T_A = –40°C, +25°C, +85°C Overlay, R_{AB} = 10 kΩ

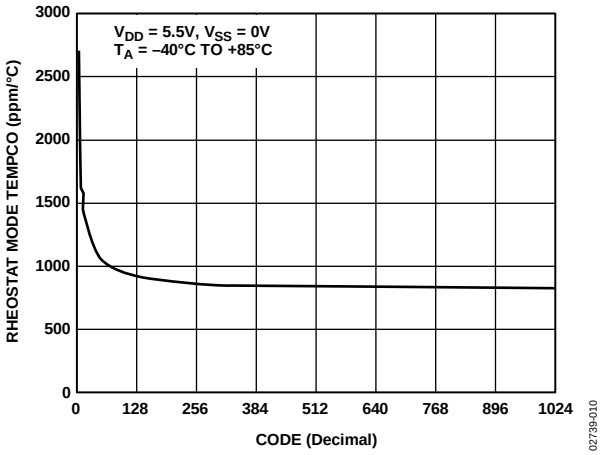

Figure 10. $(\Delta R_{WB}/R_{WB})/\Delta T \times 10^6$

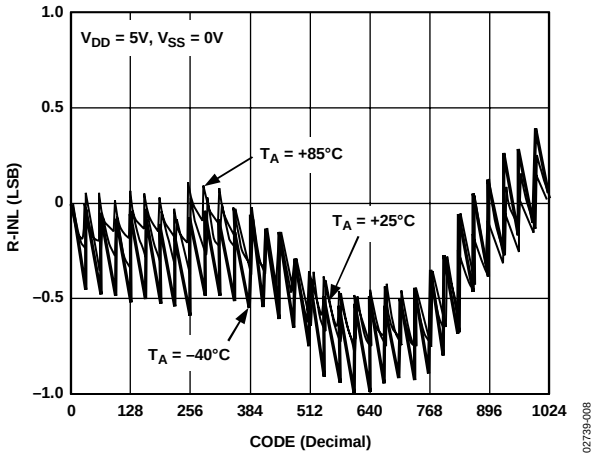

Figure 8. R-INL vs. Code, T_A = –40°C, +25°C, +85°C Overlay, R_{AB} = 10 kΩ

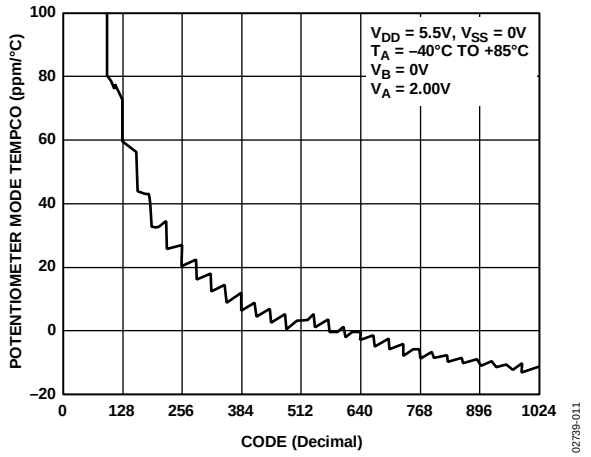

Figure 11. $(\Delta V_W/V_W)/\Delta T \times 10^6$

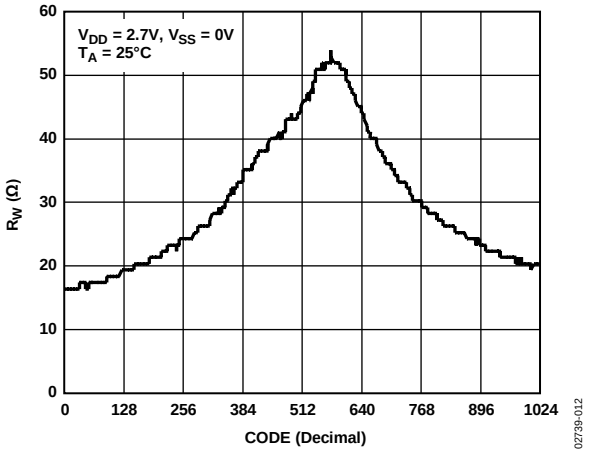

Figure 12. Wiper On Resistance vs. Code

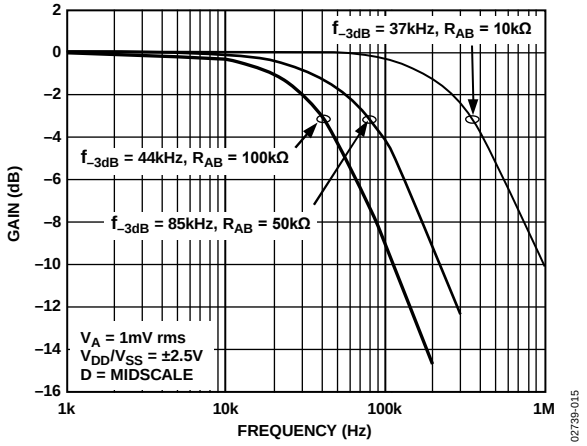

Figure 15. −3 dB Bandwidth vs. Resistance (Figure 32)

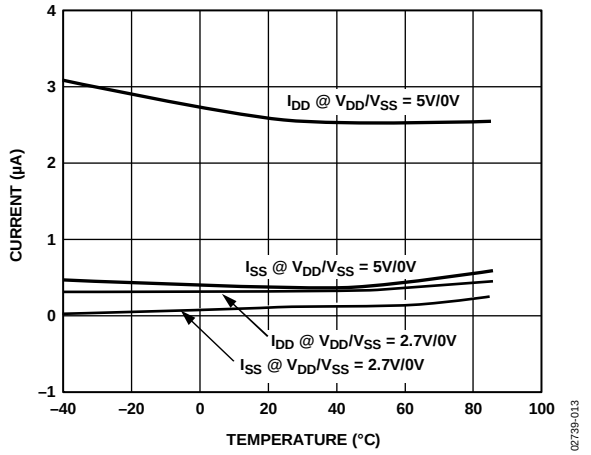

Figure 13. I_{DD} vs. Temperature, R_{AB} = 10 kΩ

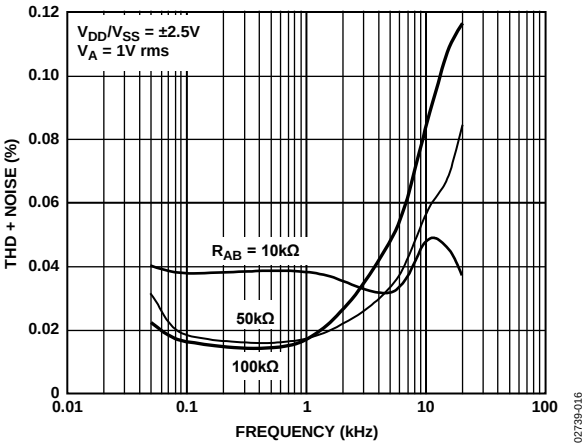

Figure 16. Total Harmonic Distortion vs. Frequency

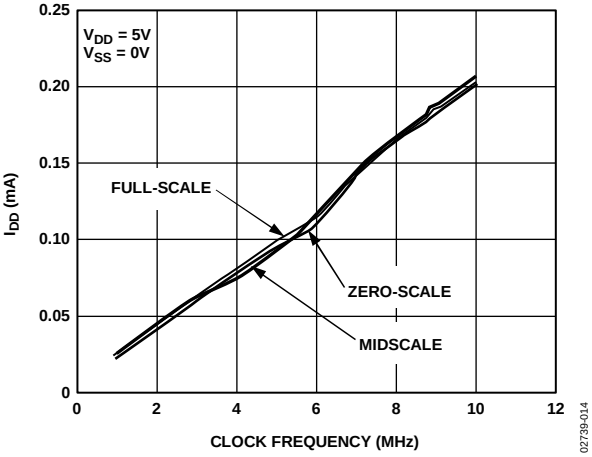

Figure 14. I_{DD} vs. Clock Frequency, R_{AB} = 10 kΩ

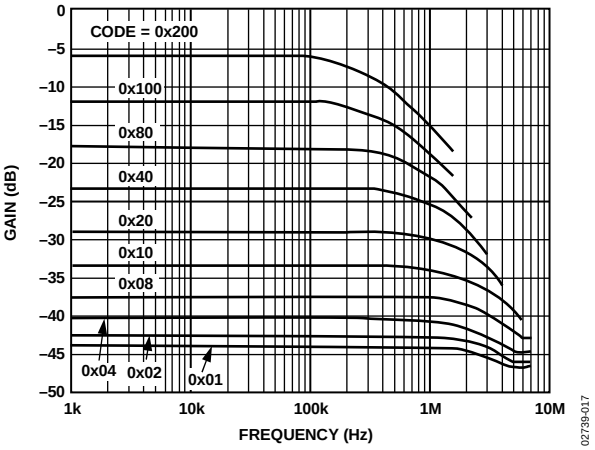

Figure 17. Gain vs. Frequency vs. Code, R_{AB} = 10 kΩ (Figure 32)

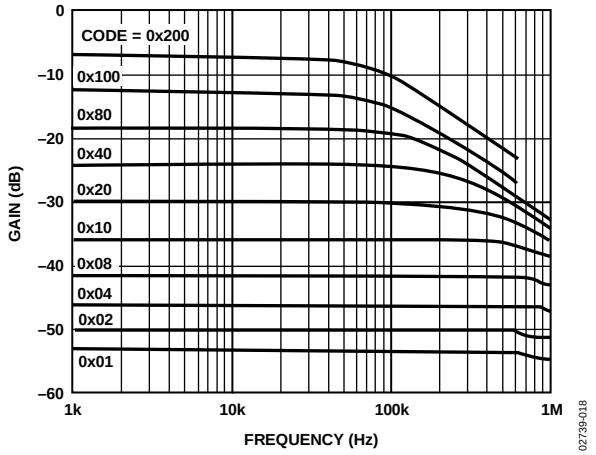

Figure 18. Gain vs. Frequency vs. Code, R_{AB} = 50 kΩ (Figure 32)

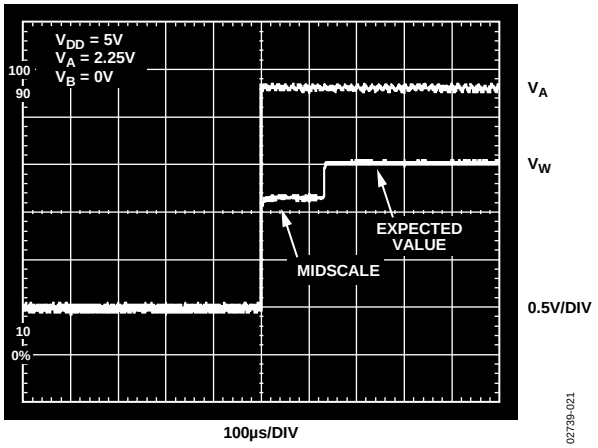

Figure 21. Power-On Reset, V_A = 2.25 V, V_B = 0 V, Code = 1010101010_B

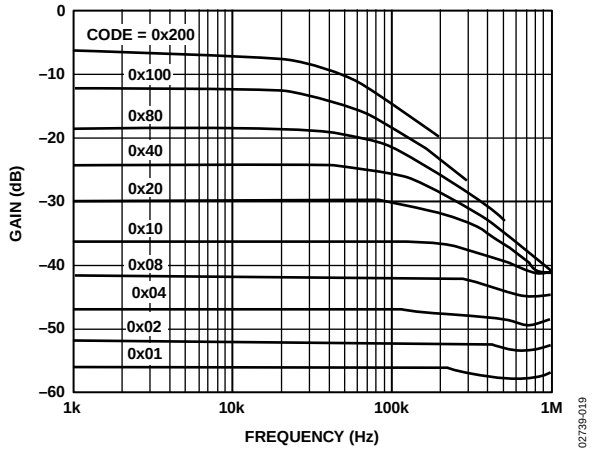

Figure 19. Gain vs. Frequency vs. Code, R_{AB} = 100 kΩ (Figure 32)

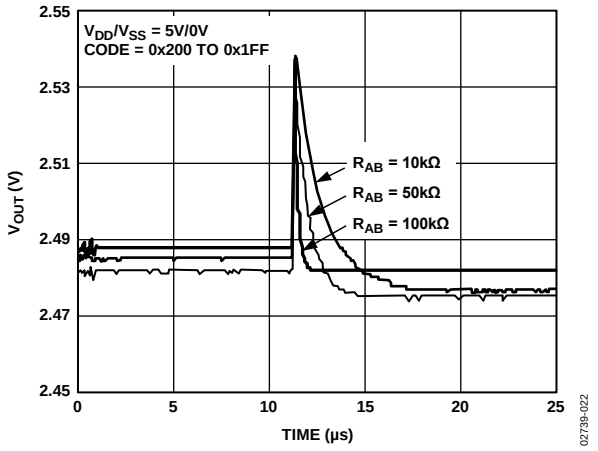

Figure 22. Midscale Glitch Energy, Code 0x200 to 0x1FF

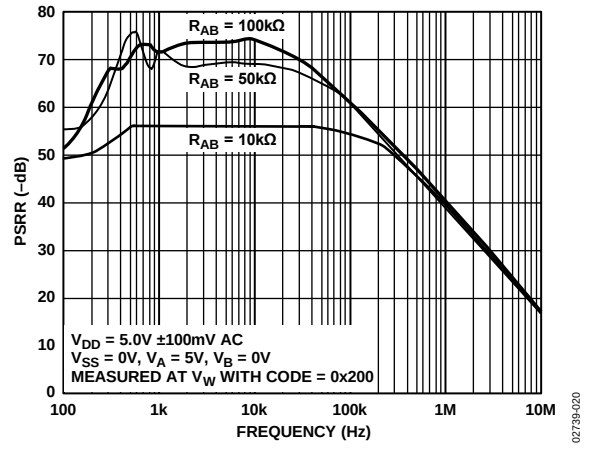

Figure 20. PSRR vs. Frequency

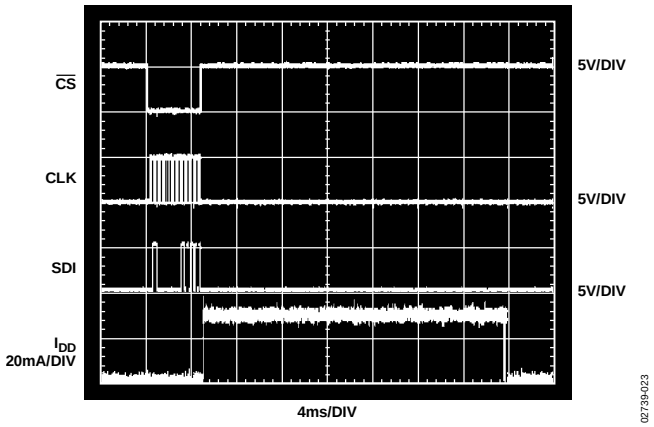

Figure 23. I_{DD} vs. Time when Storing Data to EEMEM

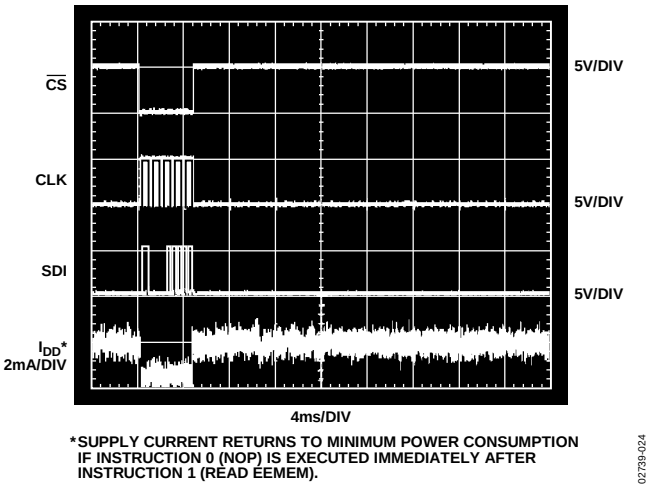

Figure 24. I_{DD} vs. Time when Restoring Data from EEMEM

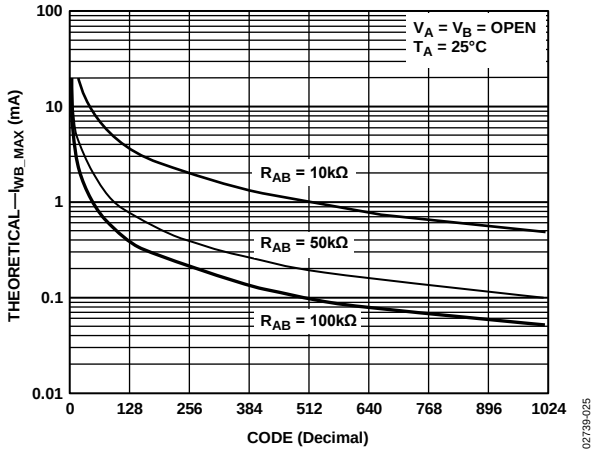

Figure 25. I_{WB_MAX} vs. Code

TEST CIRCUITS

Figure 26 to Figure 35 define the test conditions used in the specifications.

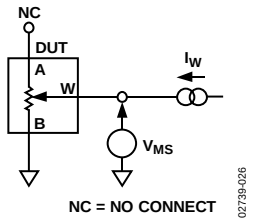

Figure 26. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

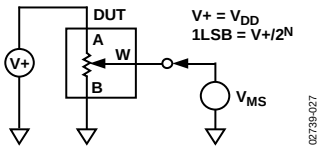

Figure 27. Potentiometer Divider Nonlinearity Error (INL, DNL)

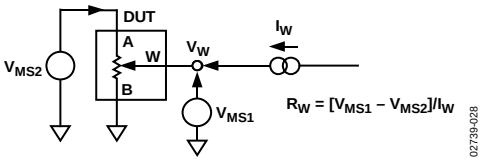

Figure 28. Wiper Resistance

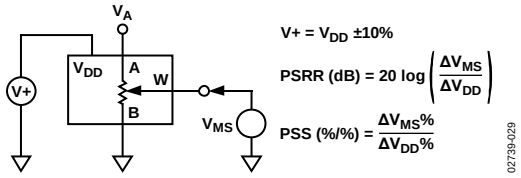

Figure 29. Power Supply Sensitivity (PSS, PSRR)

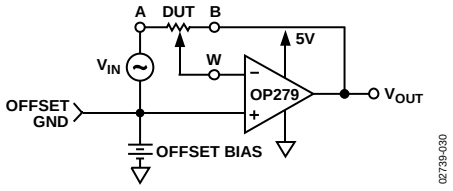

Figure 30. Inverting Gain

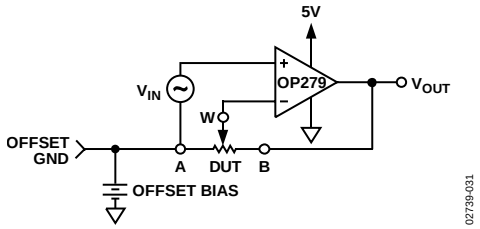

Figure 31. Noninverting Gain

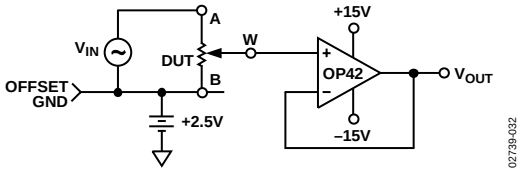

Figure 32. Gain vs. Frequency

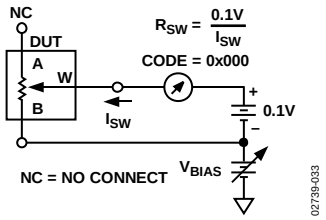

Figure 33. Incremental On Resistance

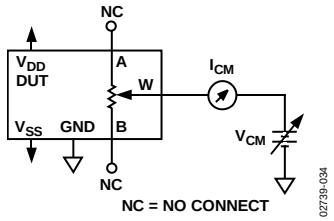

Figure 34. Common-Mode Leakage Current

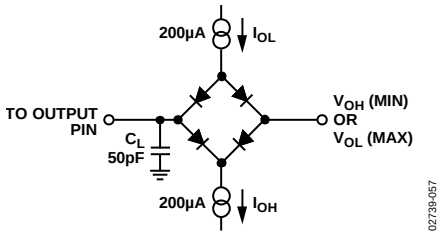

Figure 35. Load Circuit for Measuring V_{OH} and V_{OL} (The diode bridge test circuit is equivalent to the application circuit with $R_{PULL-UP}$ of 2.2 kΩ)

THEORY OF OPERATION

The AD5231 digital potentiometer is designed to operate as a true variable resistor replacement device for analog signals that remain within the terminal voltage range of $V_{SS} < V_{TERM} < V_{DD}$. The basic voltage range is limited to $V_{DD} - V_{SS} < 5.5$ V. The digital potentiometer wiper position is determined by the RDAC register contents.

The RDAC register acts as a scratchpad register, allowing as many value changes as necessary to place the potentiometer wiper in the correct position. The scratchpad register can be programmed with any position value using the standard SPI serial interface mode by loading the complete representative data-word. Once a desirable position is found, this value can be stored in an EEMEM register. Thereafter, the wiper position is always restored to that position for subsequent power-up.

The storing of EEMEM data takes approximately 25 ms; during this time, the shift register is locked, preventing any changes from taking place. The RDY pin pulses low to indicate the completion of this EEMEM storage.

The following instructions facilitate the user's programming needs (see Table 7 for details):

0. Do nothing.
1. Restore EEMEM content to RDAC.
2. Store RDAC setting to EEMEM.
3. Store RDAC setting or user data to EEMEM.
4. Decrement 6 dB.
5. Decrement 6 dB.
6. Decrement one step.
7. Decrement one step.
8. Reset EEMEM content to RDAC.
9. Read EEMEM content from SDO.
10. Read RDAC wiper setting from SDO.
11. Write data to RDAC.
12. Increment 6 dB.
13. Increment 6 dB.
14. Increment one step.
15. Increment one step.

SCRATCHPAD AND EEMEM PROGRAMMING

The scratchpad RDAC register directly controls the position of the digital potentiometer wiper. For example, when the scratchpad register is loaded with all zeros, the wiper is connected to Terminal B of the variable resistor. The scratchpad register is a standard logic register with no restriction on the number of changes allowed, but the EEMEM registers have a program erase/write cycle limitation (see the Flash/EEMEM Reliability section).

BASIC OPERATION

The basic mode of setting the variable resistor wiper position (programming the scratchpad register) is accomplished by loading the serial data input register with Instruction 11 (0xB), Address 0, and the desired wiper position data. When the proper wiper position is determined, the user can load the serial data input register with Instruction 2 (0x2), which stores the wiper position data in the EEMEM register. After 25 ms, the wiper position is permanently stored in the nonvolatile memory. Table 5 provides a programming example listing the sequence of serial data input (SDI) words with the serial data output appearing at the SDO pin in hexadecimal format.

Table 5. Set and Store RDAC Data to EEMEM Register

SDI	SDO	Action
0xB00100	0xXXXXXX	Writes data 0x100 to the RDAC register, Wiper W moves to 1/4 full-scale position.
0x20XXXX	0xB00100	Stores RDAC register content into the EEMEM register.

At system power-on, the scratchpad register is automatically refreshed with the value previously stored in the EEMEM register. The factory-preset EEMEM value is midscale, but it can be changed by the user thereafter.

During operation, the scratchpad (RDAC) register can be refreshed with the EEMEM register data with Instruction 1 (0x1) or Instruction 8 (0x8). The RDAC register can also be refreshed with the EEMEM register data under hardware control by pulsing the $\overline{PR}$ pin. The $\overline{PR}$ pulse first sets the wiper at midscale when brought to logic zero, and then, on the positive transition to logic high, it reloads the RDAC wiper register with the contents of EEMEM.

Many additional advanced programming commands are available to simplify the variable resistor adjustment process (see Table 7). For example, the wiper position can be changed one step at a time using the increment/decrement instruction or by 6 dB with the shift left/right instruction. Once an increment, decrement, or shift instruction has been loaded into the shift register, subsequent $\overline{CS}$ strobes can repeat this command.

A serial data output SDO pin is available for daisy-chaining and for readout of the internal register contents.

EEMEM PROTECTION

The write protect ($\overline{WP}$) pin disables any changes to the scratchpad register contents, except for the EEMEM setting, which can still be restored using Instruction 1, Instruction 8, and the $\overline{PR}$ pulse. Therefore, $\overline{WP}$ can be used to provide a hardware EEMEM protection feature. To disable $\overline{WP}$, it is recommended to execute a NOP instruction before returning $\overline{WP}$ to logic high.

DIGITAL INPUT/OUTPUT CONFIGURATION

All digital inputs are ESD-protected, high input impedance that can be driven directly from most digital sources. Active at logic low, $\overline{PR}$ and $\overline{WP}$ must be tied to V_{DD} if they are not used. No internal pull-up resistors are present on any digital input pins. The SDO and RDY pins are open-drain digital outputs that need pull-up resistors only if these functions are used. A resistor value in the range of 1 kΩ to 10 kΩ is a proper choice that balances the dissipation and switching speed.

The equivalent serial data input and output logic is shown in Figure 36. The open-drain output SDO is disabled whenever chip-select $\overline{CS}$ is in logic high. ESD protection of the digital inputs is shown in Figure 37 and Figure 38.

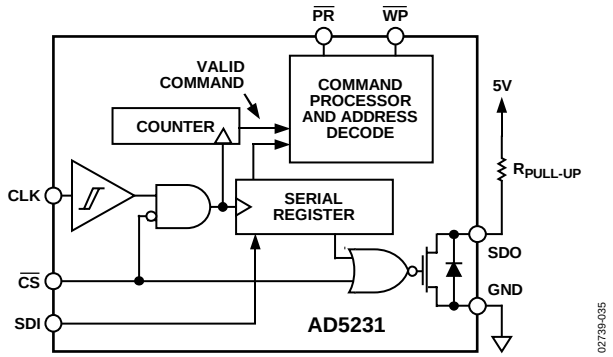

Figure 36. Equivalent Digital Input-Output Logic

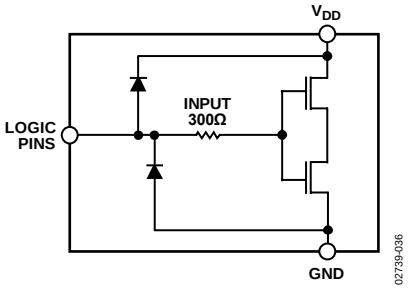

Figure 37. Equivalent ESD Digital Input Protection

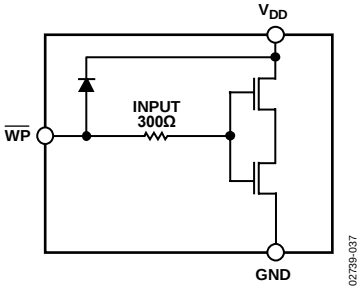

Figure 38. Equivalent $\overline{WP}$ Input Protection

SERIAL DATA INTERFACE

The AD5231 contains a 4-wire SPI-compatible digital interface (SDI, SDO, $\overline{CS}$, and CLK). It uses a 24-bit serial data-word loaded MSB first. The format of the SPI-compatible word is shown in Table 6. The chip-select $\overline{CS}$ pin must be held low until the complete data-word is loaded into the SDI pin. When $\overline{CS}$ returns high, the serial data-word is decoded according to the instructions in Table 7. The command bits (Cx) control the operation of the digital potentiometer. The address bits (Ax) determine which register is activated. The data bits (Dx) are the values that are loaded into the decoded register.

The AD5231 has an internal counter that counts a multiple of 24 bits (a frame) for proper operation. For example, AD5231 works with a 48-bit word, but it cannot work properly with a 23-bit or 25-bit word. In addition, AD5231 has a subtle feature that, if $\overline{CS}$ is pulsed without CLK and SDI, the part repeats the previous command (except during power-up). As a result, care must be taken to ensure that no excessive noise exists in the CLK or $\overline{CS}$ line that might alter the effective number of bits (ENOB) pattern. Also, to prevent data from mislocking (due to noise, for example), the counter resets if the count is not a multiple of four when $\overline{CS}$ goes high.

The SPI interface can be used in two slave modes: CPHA = 1, CPOL = 1 and CPHA = 0, CPOL = 0. CPHA and CPOL refer to the control bits that dictate SPI timing in the following MicroConverters® and microprocessors: ADuC812/ADuC824, M68HC11, and MC68HC16R1/916R1.

DAISY-CHAIN OPERATION

The serial data output pin (SDO) serves two purposes. It can be used to read the contents of the wiper setting and EEMEM values using Instruction 10 and Instruction 9, respectively. The remaining instructions (0 to 8, 11 to 15) are valid for daisy-chaining multiple devices in simultaneous operations. Daisy-chaining minimizes the number of port pins required from the controlling IC (see Figure 39). The SDO pin contains an open-drain N-Ch FET that requires a pull-up resistor if this function is used. As shown in Figure 39, users need to tie the SDO pin of one package to the SDI pin of the next package.

Users might need to increase the clock period, because the pull-up resistor and the capacitive loading at the SDO to SDI interface might require additional time delay between subsequent packages. When two AD5231s are daisy-chained, 48 bits of data are required. The first 24 bits go to U2 and the second 24 bits go to U1. The $\overline{CS}$ should be kept low until all 48 bits are clocked into their respective serial registers. The $\overline{CS}$ is then pulled high to complete the operation.

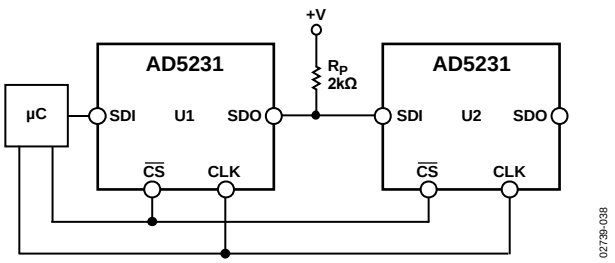

Figure 39. Daisy-Chain Configuration Using SDO

TERMINAL VOLTAGE OPERATION RANGE

The AD5231's positive V_{DD} and negative V_{SS} power supplies define the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on the A, B, and W terminals that exceed V_{DD} or V_{SS} are clamped by the internal forward-biased diodes (see Figure 40).

The ground pin of the AD5231 device is primarily used as a digital ground reference, which needs to be tied to the common ground of the PCB. The digital input control signals to the AD5231 must be referenced to the device ground pin (GND) and satisfy the logic level defined in the Specifications section. An internal level-shift circuit ensures that the common-mode voltage range of the three terminals extends from V_{SS} to V_{DD}, regardless of the digital input level.

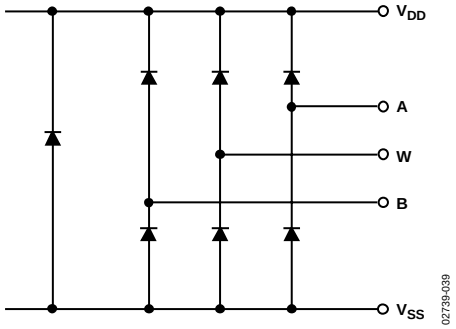

Figure 40. Maximum Terminal Voltages Set by V_{DD} and V_{SS}

POWER-UP SEQUENCE

Because there are diodes to limit the voltage compliance at the A, B, and W terminals (Figure 40), it is important to power V_{DD}/V_{SS} first before applying any voltage to Terminal A, Terminal B, and Terminal W. Otherwise, the diode is forward-biased such that V_{DD}/V_{SS} are powered unintentionally and might affect the rest of the user's circuit. The ideal power-up sequence is GND, V_{DD}, V_{SS}, digital inputs, and $V_A/V_B/V_W$. The order of powering V_A, V_B, V_W, and digital inputs is not important as long as they are powered after V_{DD}/V_{SS}.

Regardless of the power-up sequence and the ramp rates of the power supplies, once V_{DD}/V_{SS} are powered, the power-on preset remains effective, which restores the EEMEM value to the RDAC register.

LATCHED DIGITAL OUTPUTS

A pair of digital outputs, O1 and O2, is available on the AD5231. These outputs provide a nonvolatile Logic 0 or Logic 1 setting. O1 and O2 are standard CMOS logic outputs, shown in Figure 41. These outputs are ideal to replace the functions often provided by DIP switches. In addition, they can be used to drive other standard CMOS logic-controlled parts that need an occasional setting change. Pin O1 and Pin O2 default to Logic 1, and they can drive up to 50 mA of load at 5 V/25°C.

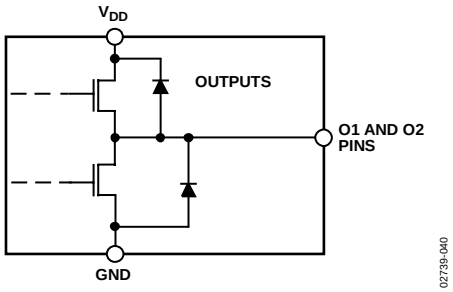

Figure 41. Logic Outputs O1 and O2

In Table 6, command bits are C0 to C3, address bits are A3 to A0, Data Bit D0 to Data Bit D9 are applicable to RDAC, and D0 to D15 are applicable to EEMEM.

Table 6. AD5231 24-Bit Serial Data-Word

	MSB Command Byte 0								Data Byte 1								Data Byte 0							LSB
RDAC	C3	C2	C1	C0	0	0	0	0	X	X	X	X	X	X	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
EEMEM	C3	C2	C1	C0	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Command instruction codes are defined in Table 7.

Table 7. Command/Operation Truth Table[1, 2, 3]

Instruction Number	Command Byte 0								Data Byte 1				Data Byte 0			Operation
	B23							B16	B15			B8	B7		B0	
	C3	C2	C1	C0	A3	A2	A1	A0	X	…	D9	D8	D7	…	D0	
0	0	0	0	0	X	X	X	X	X	…	X	X	X	…	X	NOP: Do nothing. See Table 15.
1	0	0	0	1	0	0	0	0	X	…	X	X	X	…	X	Restore EEMEM(0) contents to RDAC register. This command leaves the device in the read program power state. To return the part to the idle state, perform NOP instruction 0. See Table 15.
2	0	0	1	0	0	0	0	0	X	…	X	X	X	…	X	Store Wiper Setting: Store RDAC setting to EEMEM(0). See Table 14.
3[4]	0	0	1	1	A3	A2	A1	A0	D15	…		D8	D7	…	D0	Store contents of Data Bytes 0 and 1 (total 16 bits) to EEMEM (ADDR 1to ADDR 15). See Table 17.
4[5]	0	1	0	0	0	0	0	0	X	…	X	X	X	…	X	Decrement RDAC by 6 dB.
5[5]	0	1	0	1	X	X	X	X	X	…	X	X	X	…	X	Same as Instruction 4.
6[5]	0	1	1	0	0	0	0	0	X	…	X	X	X	…	X	Decrement RDAC by 1 position.
7[5]	0	1	1	1	X	X	X	X	X	…	X	X	X	…	X	Same as Instruction 6.
8	1	0	0	0	X	X	X	X	X	…	X	X	X	…	X	Reset: Restore RDAC with EEMEM (0) value.
9	1	0	0	1	A3	A2	A1	A0	X	…	X	X	X	…	X	Read EEMEM (ADDR 0 to ADDR 15) from SDO output in the next frame. See Table 18.
10	1	0	1	0	0	0	0	0	X	…	X	X	X	…	X	Read RDAC wiper setting from SDO output in the next frame. See Table 19.
11	1	0	1	1	0	0	0	0	X	…	D9	D8	D7	…	D0	Write contents of Data Bytes 0 and 1 (total 10 bits) to RDAC. See Table 13.
12[5]	1	1	0	0	0	0	0	0	X	…	X	X	X	…	X	Increment RDAC by 6 dB. See Table 16.
13[5]	1	1	0	1	X	X	X	X	X	…	X	X	X	…	X	Same as Instruction 12.
14[5]	1	1	1	0	0	0	0	0	X	…	X	X	X	…	X	Increment RDAC by 1 position. See Table 14.
15[5]	1	1	1	1	X	X	X	X	X	…	X	X	X	…	X	Same as Instruction 14.

[1] The SDO output shifts out the last 24 bits of data clocked into the serial register for daisy-chain operation. Exception: for any instruction following Instruction 9 or Instruction 10, the selected internal register data is present in Data Byte 0 and Data Byte 1. The instruction following 9 and 10 must also be a full 24-bit data-word to completely clock out the contents of the serial register.
[2] The RDAC register is a volatile scratchpad register that is refreshed at power-on from the corresponding nonvolatile EEMEM register.
[3] Execution of these operations takes place when the $\overline{CS}$ strobe returns to logic high.
[4] Instruction 3 writes two data bytes (16 bits of data) to EEMEM. In the case of 0 addresses, only the last 10 bits are valid for wiper position setting.
[5] The increment, decrement, and shift instructions ignore the contents of the shift register Data Byte 0 and Data Byte 1.

ADVANCED CONTROL MODES

The AD5231 digital potentiometer includes a set of user programming features to address the wide number of applications for these universal adjustment devices.

Key programming features include:

- Scratchpad programming to any desirable values
- Nonvolatile memory storage of the scratchpad RDAC register value in the EEMEM register
- Increment and decrement instructions for the RDAC wiper register
- Left and right bit shift of the RDAC wiper register to achieve ±6 dB level changes
- 28 extra bytes of user-addressable nonvolatile memory

Linear Increment and Decrement Instructions

The increment and decrement instructions (14, 15, 6, and 7) are useful for linear step-adjustment applications. These commands simplify microcontroller software coding by allowing the controller to send just an increment or decrement command to the device.

For an increment command, executing Instruction 14 with the proper address automatically moves the wiper to the next resistance segment position. Instruction 15 performs the same function, except that the address does not need to be specified.

Logarithmic Taper Mode Adjustment

Four programming instructions produce logarithmic taper increment and decrement of the wiper. These settings are activated by the 6 dB increment and 6 dB decrement instructions (12, 13, 4, and 5). For example, starting at zero scale, executing the increment Instruction 12 eleven times moves the wiper in 6 dB per step from 0% to full scale, R_{AB}. The 6 dB increment instruction doubles the value of the RDAC register contents each time the command is executed. When the wiper position is near the maximum setting, the last 6 dB increment instruction causes the wiper to go to the full-scale 1023 code position. Further 6 dB per increment instructions do not change the wiper position beyond its full scale.

The 6 dB step increments and 6 dB step decrements are achieved by shifting the bit internally to the left or right, respectively. The following information explains the nonideal ±6 dB step adjustment under certain conditions. Table 8 illustrates the operation of the shifting function on the RDAC register data bits. Each table row represents a successive shift operation. Note that the left-shift 12 and 13 instructions were modified such that, if the data in the RDAC register is equal to zero and the data is shifted left, the RDAC register is then set to Code 1. Similarly, if the data in the RDAC register is greater than or equal to midscale and the data is shifted left, then the data in the RDAC register is automatically set to full scale. This makes the left-shift function as ideal a logarithmic adjustment as possible.

The right-shift 4 and 5 instructions are ideal only if the LSB is 0 (ideal logarithmic = no error). If the LSB is 1, the right-shift function generates a linear half-LSB error, which translates to a number-of-bits dependent logarithmic error, as shown in Figure 42. The plot shows the error of the odd numbers of bits for the AD5231.

Table 8. Detail Left-Shift and Right-Shift Functions for 6 dB Step Increment and Decrement

	Left-Shift	Right-Shift	
	00 0000 0000	11 1111 1111	
	00 0000 0001	01 1111 1111	
	00 0000 0010	00 1111 1111	
	00 0000 0100	00 0111 1111	
	00 0000 1000	00 0011 1111	
Left-Shift	00 0001 0000	00 0001 1111	Right-Shift
(+6 dB/step)	00 0010 0000	00 0000 1111	(–6 dB/step)
	00 0100 0000	00 0000 0111	
	00 1000 0000	00 0000 0011	
	01 0000 0000	00 0000 0001	
	10 0000 0000	00 0000 0000	
	11 1111 1111	00 0000 0000	
	11 1111 1111	00 0000 0000	

Actual conformance to a logarithmic curve between the data contents in the RDAC register and the wiper position for each right-shift 4 and 5 command execution contains an error only for odd numbers of bits. Even numbers of bits are ideal. The graph in Figure 42 shows plots of Log_Error [$20 \times \log_{10}$ (error/code)] for the AD5231. For example, Code 3 Log_Error = $20 \times \log_{10}$ (0.5/3) = −15.56 dB, which is the worst case. The plot of Log_Error is more significant at the lower codes.

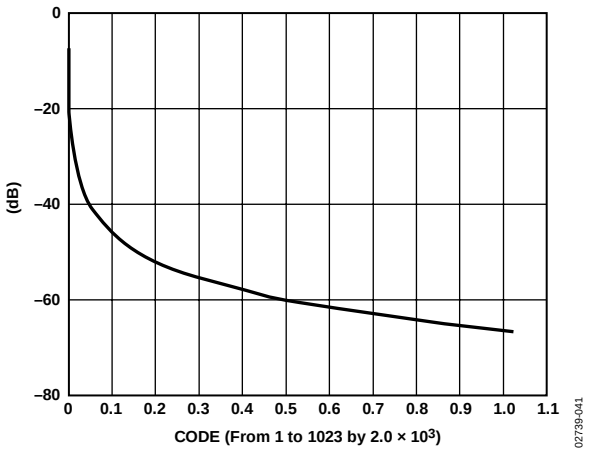

Figure 42. Plot of Log_Error Conformance for Odd Numbers of Bits Only (Even Numbers of Bits Are Ideal)

Using Additional Internal Nonvolatile EEMEM

The AD5231 contains additional user EEMEM registers for storing any 16-bit data such as memory data for other components, look-up tables, or system identification information. Table 9 provides an address map of the internal storage registers shown in the functional block diagram as EEMEM1, EEMEM2, and 28 bytes (14 addresses × 2 bytes each) of user EEMEM.

Table 9. EEMEM Address Map

Address	EEMEM for…
0000	RDAC[1, 2]
0001	O1 and O2[3]
0010	USER1[4]
0011	USER2
…	…
1110	USER13
1111	USER14

[1] RDAC data stored in EEMEM location is transferred to the RDAC register at power-on, or when Instruction 1, Instruction 8, or $\overline{PR}$ are executed.
[2] Execution of Instruction 1 leaves the device in the read mode power consumption state. After the last Instruction 1 is executed, the user should perform a NOP, Instruction 0 to return the device to the low power idling state.
[3] O1 and O2 data stored in EEMEM locations is transferred to the corresponding digital register at power-on, or when Instruction 1 and Instruction 8 are executed.
[4] USERx are internal nonvolatile EEMEM registers available to store 16-bit information using Instruction 3 and restore the contents using Instruction 9.

RDAC STRUCTURE

The patent-pending RDAC contains multiple strings of equal resistor segments with an array of analog switches that act as the wiper connection. The number of positions is the resolution of the device. The AD5231 has 1024 connection points, allowing it to provide better than 0.1% settability resolution. Figure 43 shows an equivalent structure of the connections among the three terminals of the RDAC. The SW_A and SW_B are always on, while the switches SW(0) to SW(2^N–1) are on one at a time, depending on the resistance position decoded from the data bits. Because the switch is not ideal, there is a 15 Ω wiper resistance, R_W. Wiper resistance is a function of supply voltage and temperature. The lower the supply voltage or the higher the temperature, the higher the resulting wiper resistance. Users should be aware of the wiper resistance dynamics if accurate prediction of the output resistance is needed.

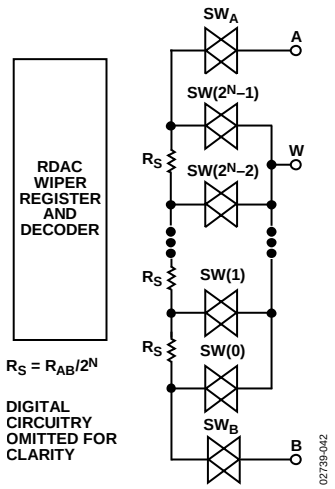

Figure 43. Equivalent RDAC Structure (Patent Pending)

Table 10. Nominal Individual Segment Resistor (R_S)

Device Resolution	10 kΩ Version	50 kΩ Version	100 kΩ Version
10-Bit	9.8 Ω	48.8 Ω	97.6 Ω

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

The nominal resistance of the RDAC between Terminal A and Terminal B, R_{AB}, is available with 10 kΩ, 50 kΩ, and 100 kΩ with 1024 positions (10-bit resolution). The final digit(s) of the part number determine the nominal resistance value, for example, 10 kΩ = 10; 50 kΩ = 50; 100 kΩ = C.

The 10-bit data-word in the RDAC latch is decoded to select one of the 1024 possible settings. The following discussion describes the calculation of resistance R_{WB} at different codes of a 10 kΩ part. For V_{DD} = 5 V, the wiper's first connection starts at Terminal B for data 0x000. R_{WB}(0) is 15 Ω because of the wiper resistance, and because it is independent of the nominal resistance. The second connection is the first tap point where R_{WB} (1) becomes 9.7 Ω + 15 Ω = 24.7 Ω for data 0x001. The third connection is the next tap point representing R_{WB} (2) = 19.4 Ω + 15 Ω = 34.4 Ω for data 0x002 and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at R_{WB} (1023) = 10,005 Ω. See Figure 43 for a simplified diagram of the equivalent RDAC circuit. When R_{WB} is used, Terminal A can be left floating or tied to the wiper.

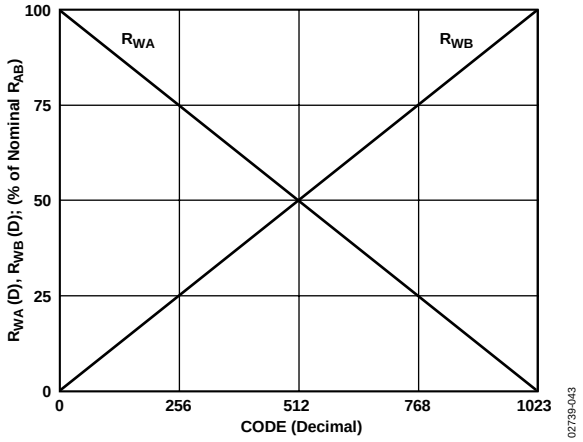

Figure 44. $R_{WA}(D)$ and $R_{WB}(D)$ vs. Decimal Code

The general equation that determines the programmed output resistance between W and B is

$$R_{WB}(D) = \frac{D}{1024} \times R_{AB} + R_W \quad (1)$$

where:

D is the decimal equivalent of the data contained in the RDAC register.
R_{AB} is the nominal resistance between Terminal A and Terminal B.
R_W is the wiper resistance.

For example, the output resistance values in Table 11 are set for the given RDAC latch codes with V_{DD} = 5 V (applies to R_{AB} = 10 kΩ digital potentiometers).

Table 11. R_{WB} (D) at Selected Codes for R_{AB} = 10 kΩ

D (DEC)	R_{WB}(D) (Ω)	Output State
1023	10,005	Full scale
512	50,015	Midscale
1	24.7	1 LSB
0	15	Zero scale (wiper contact resistor)

Note that, in the zero-scale condition, a finite wiper resistance of 15 Ω is present. Care should be taken to limit the current flow between W and B in this state to no more than 20 mA to avoid degradation or possible destruction of the internal switches.

Like the mechanical potentiometer that the RDAC replaces, the AD5231 part is totally symmetrical. The resistance between Wiper W and Terminal A also produces a digitally controlled complementary resistance, R_{WA}. Figure 44 shows the symmetrical programmability of the various terminal connections. When R_{WA} is used, Terminal B can be left floating or tied to the wiper. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch is increased in value.

The general transfer equation for this operation is

$$R_{WB}(D) = \frac{1024 - D}{1024} \times R_{AB} + R_W \quad (2)$$

For example, the output resistance values in Table 12 are set for the RDAC latch codes with V_{DD} = 5 V (applies to R_{AB} = 10 kΩ digital potentiometers).

Table 12. R_{WA}(D) at Selected Codes for R_{AB} = 10 kΩ

D (DEC)	R_{WA}(D) (Ω)	Output State
1023	24.7	Full scale
512	5015	Midscale
1	10005	1 LSB
0	10,015	Zero scale

The typical distribution of R_{AB} from device to device matches tightly when they are processed in the same batch. When devices are processed at a different time, device-to-device matching becomes process-lot dependent and exhibits a −40% to +20% variation. The change in R_{AB} with temperature has a 600 ppm/°C temperature coefficient.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer can be configured to generate an output voltage at the wiper terminal that is proportional to the input voltages applied to Terminal A and Terminal B. For example, connecting Terminal A to 5 V and Terminal B to ground produces an output voltage at the wiper that can be any value from 0 V to 5 V. Each LSB of voltage is equal to the voltage applied across Terminals A–B divided by the 2^N position resolution of the potentiometer divider.

Because AD5231 can also be supplied by dual supplies, the general equation defining the output voltage at V_W with respect to ground for any given input voltages applied to Terminal A and Terminal B is

$$V_W(D) = \frac{D}{1024} \times V_{AB} + V_B \quad (3)$$

Equation 3 assumes that V_W is buffered so that the effect of wiper resistance is minimized. Operation of the digital potentiometer in divider mode results in more accurate operation over temperature. Here, the output voltage is dependent on the ratio of the internal resistors and not the absolute value; therefore, the drift improves to 15 ppm/°C. There is no voltage polarity restriction between Terminal A, Terminal B, and Terminal W as long as the terminal voltage (V_{TERM}) stays within $V_{SS} < V_{TERM} < V_{DD}$.

PROGRAMMING EXAMPLES

The following programming examples illustrate a typical sequence of events for various features of the AD5231. See Table 7 for the instructions and data-word format. The instruction numbers, addresses, and data appearing at SDI and SDO pins are in hexadecimal format.

Table 13. Scratchpad Programming

SDI	SDO	Action
0xB00100	0xXXXXXX	Writes data 0x100 into RDAC register, Wiper W moves to 1/4 full-scale position.

Table 14. Incrementing RDAC Followed by Storing the Wiper Setting to EEMEM

SDI	SDO	Action
0xB00100	0xXXXXXX	Writes data 0x100 into RDAC register, Wiper W moves to 1/4 full-scale position.
0xE0XXXX	0xB00100	Increments RDAC register by one to 0x101.
0xE0XXXX	0xE0XXXX	Increments RDAC register by one to 0x102. Continue until desired wiper position is reached.
0x20XXXX	0xXXXXXX	Stores RDAC register data into EEMEM(0). Optionally tie $\overline{WP}$ to GND to protect EEMEM values.

The EEMEM value for the RDAC can be restored by power-on, by strobing the $\overline{PR}$ pin, or by programming, as shown in Table 15.

Table 15. Restoring the EEMEM Value to the RDAC Register

SDI	SDO	Action
0x10XXXX	0xXXXXXX	Restores the EEMEM(0) value to the RDAC register.
0x00XXXX	0x10XXXX	NOP. Recommended step to minimize power consumption.

Table 16. Using Left-Shift by One to Increment 6 dB Step

SDI	SDO	Action
0xC0XXXX	0xXXXXXX	Moves the wiper to double the present data contained in the RDAC register.

Table 17. Storing Additional User Data in EEMEM

SDI	SDO	Action
0x32AAAA	0xXXXXXX	Stores data 0xAAAA in the extra EEMEM location USER1. (Allowable to address in 14 locations with a maximum of 16 bits of data.)
0x335555	0x32AAAA	Stores data 0x5555 in the extra EEMEM location USER2. (Allowable to address in 14 locations with a maximum of 16 bits of data.)

Table 18. Reading Back Data from Memory Locations

SDI	SDO	Action
0x92XXXX	0xXXXXXX	Prepares data read from EEMEM(2) location.
0x00XXXX	0x92AAAA	NOP Instruction 0 sends a 24-bit word out of SDO, where the last 16 bits contain the contents in the EEMEM(2) location. The NOP command ensures that the device returns to the idle power dissipation state.

Table 19. Reading Back Wiper Settings

SDI	SDO	Action
0xB00200	0xXXXXXX	Writes RDAC to midscale.
0xC0XXXX	0xB00200	Doubles RDAC from midscale to full scale (left-shift instruction).
0xA0XXXX	0xC0XXXX	Prepares reading wiper setting from RDAC register.
0xXXXXXX	0xA003FF	Reads back full-scale value from SDO.

FLASH/EEMEM RELIABILITY

The Flash/EE memory array on the AD5231 is fully qualified for two key Flash/EE memory characteristics, namely Flash/EE memory cycling endurance and Flash/EE memory data retention.

Endurance quantifies the ability of the Flash/EE memory to be cycled through many program, read, and erase cycles. In real terms, a single endurance cycle is composed of four independent, sequential events. These events are defined as

- Initial page erase sequence
- Read/verify sequence
- Byte program sequence
- Second read/verify sequence

During reliability qualification, Flash/EE memory is cycled from 0x000 to 0x3FF until a first fail is recorded signifying the endurance limit of the on-chip Flash/EE memory.

As indicated in the Specifications section, the AD5231 Flash/EE memory endurance qualification has been carried out in accordance with JEDEC Specification A117 over the industrial temperature range of −40°C to +85°C. The results allow the specification of a minimum endurance figure over supply and temperature of 100,000 cycles, with an endurance figure of 700,000 cycles being typical of operation at 25°C.

Retention quantifies the ability of the Flash/EE memory to retain its programmed data over time. Again, the AD5231 has been qualified in accordance with the formal JEDEC Retention Lifetime Specification (A117) at a specific junction temperature (T_J = 55°C). As part of this qualification procedure, the Flash/EE memory is cycled to its specified endurance limit, described previously, before data retention is characterized. This means that the Flash/EE memory is guaranteed to retain its data for its full specified retention lifetime every time the Flash/EE memory is reprogrammed. It should also be noted that retention lifetime, based on an activation energy of 0.6 eV, derates with T_J, as shown in Figure 45. For example, the data is retained for 100 years at 55°C operation, but reduces to 15 years at 85°C operation. Beyond these limits, the part must be reprogrammed so that the data can be restored.

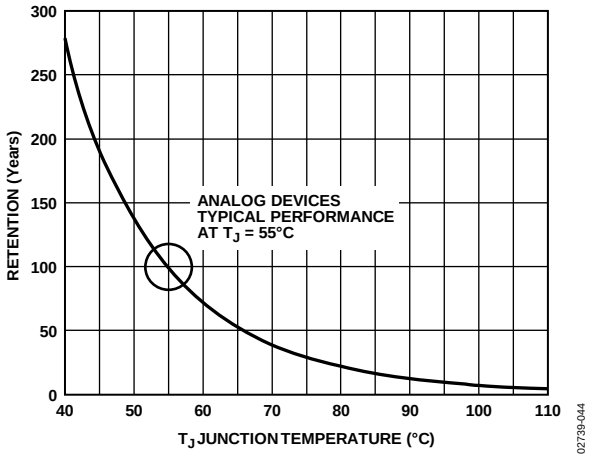

Figure 45. Flash/EE Memory Data Retention

APPLICATIONS

BIPOLAR OPERATION FROM DUAL SUPPLIES

The AD5231 can be operated from dual supplies ±2.5 V, which enables control of ground referenced ac signals or bipolar operation. AC signals as high as V_{DD}/V_{SS} can be applied directly across Terminal A to Terminal B with output taken from Terminal W. See Figure 46 for a typical circuit connection.

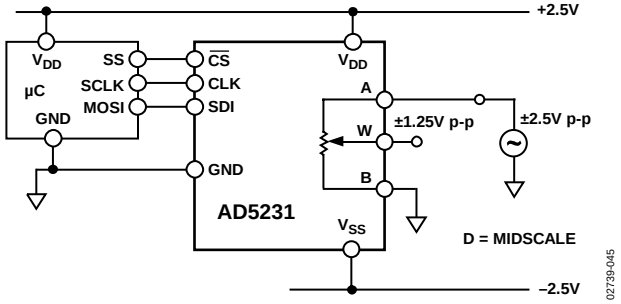

Figure 46. Bipolar Operation from Dual Supplies

HIGH VOLTAGE OPERATION

The digital potentiometer can be placed directly in the feedback or input path of an op amp for gain control, provided that the voltage across Terminals A–B, Terminals W–A, or Terminals W–B does not exceed |5 V|. When high voltage gain is needed, users should set a fixed gain in an op amp operated at a higher voltage and let the digital potentiometer control the adjustable input. Figure 47 shows a simple implementation.

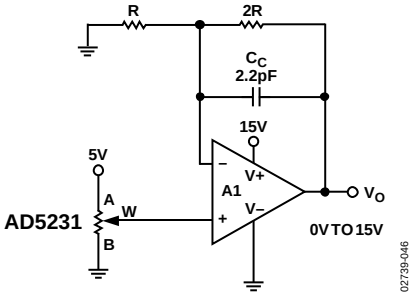

Figure 47. 15 V Voltage Span Control

BIPOLAR PROGRAMMABLE GAIN AMPLIFIER

There are several ways to achieve bipolar gain. Figure 48 shows one versatile implementation. Digital potentiometer U1 sets the adjustment range; the wiper voltage V_{W2} can, therefore, be programmed between V_i and $-KV_i$ at a given U2 setting. For linear adjustment, configure A2 as a noninverting amplifier and the transfer function becomes

$$\frac{V_O}{V_I} = \left(1 + \frac{R2}{R1}\right) \times \left(\frac{D_2}{1024} \times (1 + K) - K\right) \quad (4)$$

where:

K is the ratio of R_{WB}/R_{WA} that is set by U1.
D is the decimal equivalent of the input code.

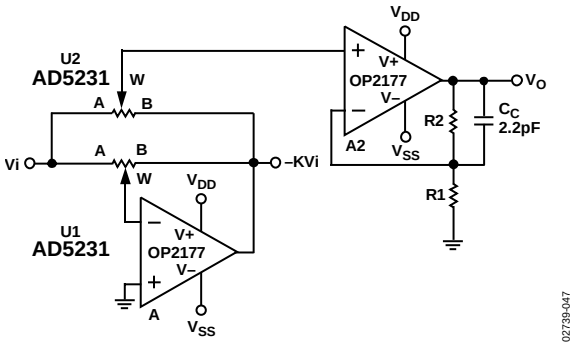

Figure 48. Bipolar Programmable Gain Amplifier

In the simpler (and much more usual) case where K = 1, a pair of matched resistors can replace U1. Equation 4 can be simplified to

$$\frac{V_O}{V_I} = \left(1 + \frac{R2}{R1}\right) \times \left(\frac{2D_2}{1024} - 1\right) \quad (5)$$

Table 20 shows the result of adjusting D with A2 configured as a unity gain, a gain of 2, and a gain of 10. The result is a bipolar amplifier with linearly programmable gain and 1024-step resolution.

Table 20. Result of Bipolar Gain Amplifier

D	R1 = ∞, R2 = 0	R1 = R2	R2 = 9 × R1
0	−1	−2	−10
256	−0.5	−1	−5
512	0	0	0
768	0.5	1	5
1023	0.992	1.984	9.92

10-BIT BIPOLAR DAC

If the circuit in Figure 48 is changed with the input taken from a voltage reference and A2 configured as a buffer, a 10-bit bipolar DAC can be realized. Compared to the conventional DAC, this circuit offers comparable resolution but not the precision because of the wiper resistance effects. Degradation of the nonlinearity and temperature coefficient is prominent near both ends of the adjustment range. On the other hand, this circuit offers a unique nonvolatile memory feature that in some cases outweighs any shortfall in precision.

The output of this circuit is

$$V_O = \left(\frac{2D_2}{1024} - 1\right) \times V_{REF} \quad (6)$$

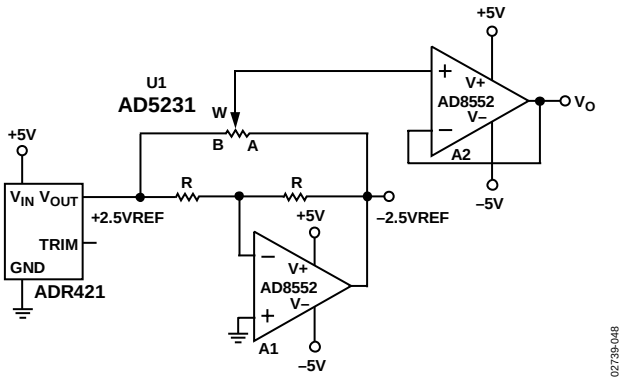

Figure 49. 10-Bit Bipolar DAC

10-BIT UNIPOLAR DAC

Figure 50 shows a unipolar 10-bit DAC using AD5231. The buffer is needed to drive various leads.

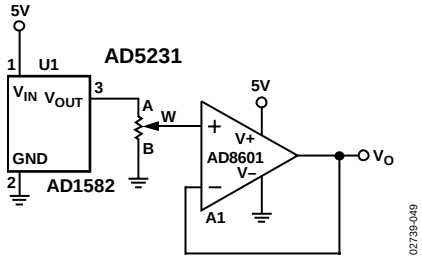

Figure 50. 10-Bit Unipolar DAC

PROGRAMMABLE VOLTAGE SOURCE WITH BOOSTED OUTPUT

For applications that require high current adjustment, such as a laser diode driver or tunable laser, a boosted voltage source can be considered (see Figure 51).

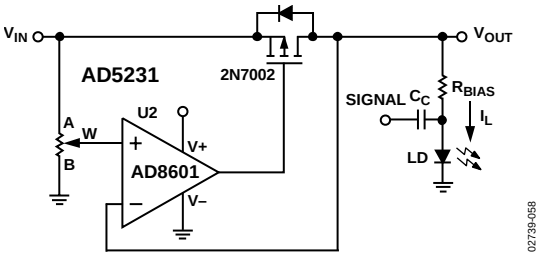

Figure 51. Programmable Booster Voltage Source

In this circuit, the inverting input of the op amp forces the V_{OUT} to be equal to the wiper voltage set by the digital potentiometer. The load current is then delivered by the supply via the N-Ch FET N_1. N_1 power handling must be adequate to dissipate $(V_I - V_O) \times I_L$ power. This circuit can source a maximum of 100 mA with a 5 V supply.

For precision applications, a voltage reference such as ADR421, ADR03, or ADR370 can be applied at Terminal A of the digital potentiometer.

PROGRAMMABLE CURRENT SOURCE

A programmable current source can be implemented with the circuit shown in Figure 52.

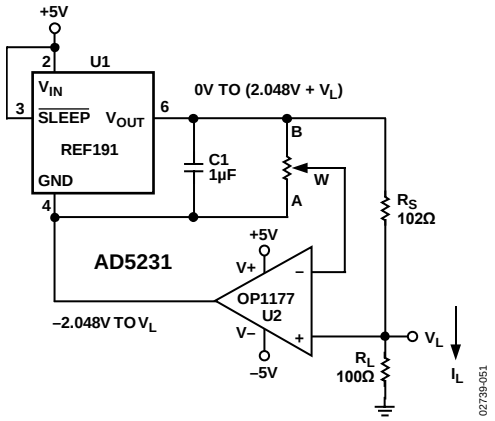

Figure 52. Programmable Current Source

REF191 is a unique low supply, headroom precision reference that can deliver the 20 mA needed at 2.048 V. The load current is simply the voltage across Terminals B–W of the digital potentiometer divided by R_S:

$$I_L = \frac{V_{REF} \times D}{R_S \times 1024} \quad (7)$$

The circuit is simple, but be aware that there are two issues. First, dual-supply op amps are ideal because the ground potential of REF191 can swing from −2.048 V at zero scale to V_L at full scale of the potentiometer setting. Although the circuit works under single-supply, the programmable resolution of the system is reduced. Second, the voltage compliance at V_L is limited to 2.5 V or equivalently a 125 Ω load. Should higher voltage compliance be needed, users can consider digital potentiometers AD5260, AD5280, and AD7376. Figure 53 shows an alternate circuit for high voltage compliance.

To achieve higher current, such as when driving a high power LED, the user can replace the UI with an LDO, reduce R_S, and add a resistor in series with the digital potentiometer's A terminal. This limits the potentiometer's current and increases the current adjustment resolution.

PROGRAMMABLE BIDIRECTIONAL CURRENT SOURCE

For applications that require bidirectional current control or higher voltage compliance, a Howland current pump can be a solution. If the resistors are matched, the load current is

$$I_L = \frac{\frac{(R2A + R2B)}{R1}}{R2B} \times V_W \quad (8)$$

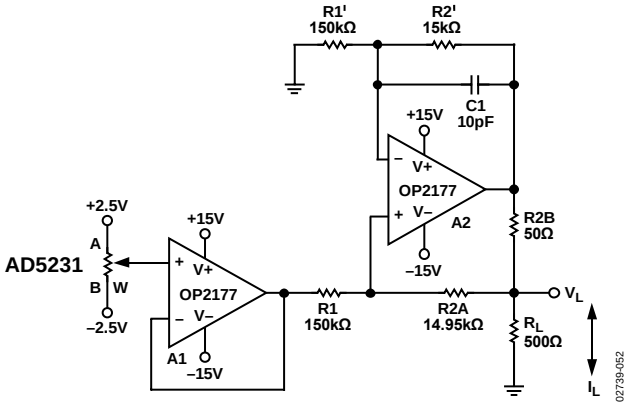

Figure 53. Programmable Bidirectional Current Source

R2B, in theory, can be made as small as necessary to achieve the current needed within the A2 output current-driving capability. In this circuit, OP2177 delivers ±5 mA in both directions, and the voltage compliance approaches 15 V. It can be shown that the output impedance is

$$Z_O = \frac{R1'\ R2B\ (R1 + R2A)}{R1R2' - R1'(R2A + R2B)} \quad (9)$$

Z_O can be infinite if resistors R1 and R2 match precisely with R1 and R2A + R2B, respectively. On the other hand, Z_O can be negative if the resistors are not matched. As a result, C1, in the range of 1 pF to 10 pF, is needed to prevent oscillation from the negative impedance.

RESISTANCE SCALING

The AD5231 offers 10 kΩ, 50 kΩ, and 100 kΩ nominal resistance. For users who need lower resistance but want to maintain the number of adjustment steps, they can parallel multiple devices. For example, Figure 54 shows a simple scheme of paralleling two AD5231s. To adjust half the resistance linearly per step, users need to program both devices coherently with the same settings and tie the terminals as shown.

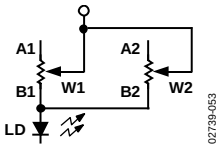

Figure 54. Reduce Resistance by Half with Linear Adjustment Characteristics

In voltage diver mode, by paralleling a discrete resistor as shown in Figure 55, a proportionately lower voltage appears at Terminals A–B. This translates into a finer degree of precision, because the step size at Terminal W is smaller. The voltage can be found as follows:

$$V_W(D) = \frac{(R_{AB}\ //\ R2)}{R3 + R_{AB}\ //\ R2} \times \frac{D}{1024} \times V_{DD} \quad (10)$$

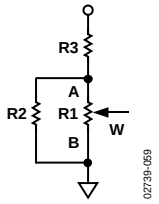

Figure 55. Lowering the Nominal Resistance

Figure 54 and Figure 55 show that the digital potentiometers change steps linearly. On the other hand, pseudo log taper adjustment is usually preferred in applications such as audio control. Figure 56 shows another type of resistance scaling. In this configuration, the smaller the R2 with respect to R1, the more the pseudo log taper characteristic of the circuit behaves.

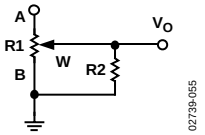

Figure 56. Resistor Scaling with Pseudo Log Adjustment Characteristics

RDAC CIRCUIT SIMULATION MODEL

The internal parasitic capacitances and the external load dominates the ac characteristics of the RDACs. The −3 dB bandwidth of the AD5231BRU10 (10 kΩ resistor) measures 370 kHz at half scale when configured as a potentiometer divider. Figure 15 provides the large signal BODE plot characteristics. A parasitic simulation mode is shown in Figure 57.

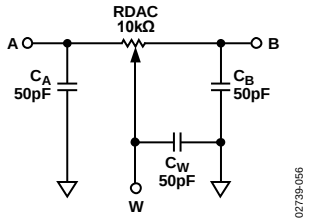

Figure 57. RDAC Circuit Simulation Model for RDAC = 10 kΩ

The following code provides a macro model net list for the 10 kΩ RDAC:

```
.PARAM D = 1024, RDAC = 10E3
*
.SUBCKT DPOT (A, W, B)
*
CA   A   0   50E-12
RWA  A   W   {(1-D/1024)* RDAC + 15}
CW   W   0   50E-12
RWB  W   B   {D/1024 * RDAC + 15}
CB   B   0   50E-12
*
.ENDS DPOT
```

OUTLINE DIMENSIONS

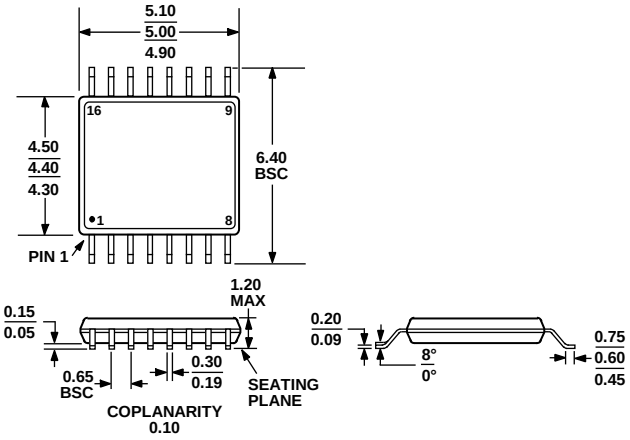

Figure 58. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	R_{AB} (kΩ)	Temperature Range	Package Description	Package Option	Ordering Quantity
AD5231BRU10	10	−40°C to +85°C	16-Lead TSSOP	RU-16	96
AD5231BRU10-REEL7	10	−40°C to +85°C	16-Lead TSSOP	RU-16	1,000
AD5231BRUZ10	10	−40°C to +85°C	16-Lead TSSOP	RU-16	96
AD5231BRUZ10-REEL7	10	−40°C to +85°C	16-Lead TSSOP	RU-16	1,000
AD5231BRUZ50	50	−40°C to +85°C	16-Lead TSSOP	RU-16	96
AD5231BRUZ50-REEL7	50	−40°C to +85°C	16-Lead TSSOP	RU-16	1,000
AD5231BRU100	100	−40°C to +85°C	16-Lead TSSOP	RU-16	96
AD5231BRU100-REEL7	100	−40°C to +85°C	16-Lead TSSOP	RU-16	1,000
AD5231BRUZ100	100	−40°C to +85°C	16-Lead TSSOP	RU-16	96
AD5231BRUZ100-RL7	100	−40°C to +85°C	16-Lead TSSOP	RU-16	1,000

[1] Z = RoHS Compliant Part.

NOTES

Purchase of licensed I²C components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

D02739-0-3/13(D)