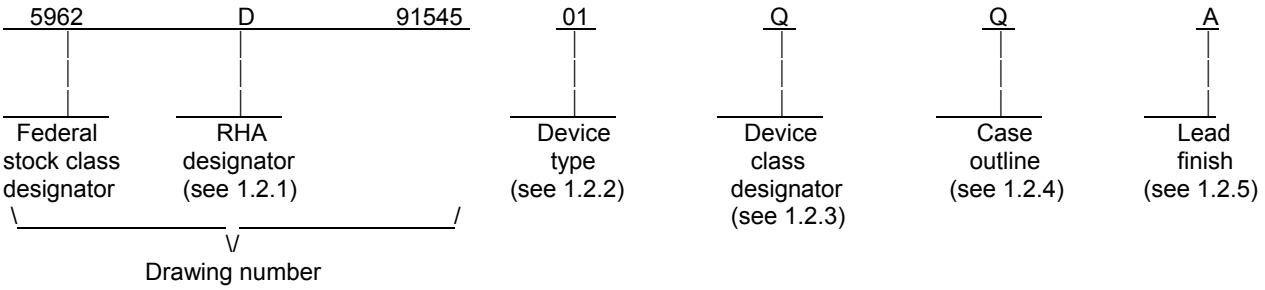
1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M), space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Standby Access time	Supply Current
01	V2500H	38-input, 24-output and-or-logic array	35 ns	
02	V2500H	38-input, 24-output and-or-logic array	25 ns	
03	V2500L	38-input, 24-output and-or-logic array	35 ns	10 mA
04	V2500B	38-input, 24-output and-or-logic array	15 ns	
05	V2500BL	38-input, 24-output and-or-logic array	20 ns	10 mA
06	V2500BQ	38-input, 24-output and-or-logic array	25 ns	
07	V2500BQL	38-input, 24-output and-or-logic array	30 ns	5 mA

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q, V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Q	GDIP1-T40 or CDIP2-T40	40	Dual-in-line 1/
X	CQCC1-N44	44	Square leadless chip carrier 1/
Y	See figure 1	44	J - leaded chip carrier 1/

1/ Lid shall be transparent to permit ultraviolet light erasure.

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 2/ 3/

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-2.0 V dc to +7.0 V dc 4/
Output voltage range applied	-0.5 V dc to +7.0 V dc 4/
Output sink current	8 mA
Thermal resistance, junction-to-case (θJC):	
Cases Q, X	See MIL-STD-1835
Case Y	20°C/W
Maximum power dissipation (P_D) 5/	1.2 W
Maximum junction temperature	+175°C
Lead temperature (soldering, 10 seconds maximum)	+300°C
Endurance	25 erase/write cycles (minimum)
Data retention	10 years (minimum)

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Supply voltage (V_{SS})	0.0 V dc
High level input voltage range (V_{IH}) -	2.0 V dc minimum
Low level input voltage range (V_{IL})	0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3/ All voltages referenced to V_{SS}.

4/ Minimum voltage is -0.6 V dc which may undershoot to -2.0 V dc for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} +0.75 V dc which may overshoot to +7.0 V dc for pulses of less than 20 ns.

5/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-00 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to: ASTM International, PO Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959; http://www.astm.org.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard EIA/JESD78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201; http://www.jedec.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535, and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and on figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 3 herein. When required in screening (see 4.2 herein), or qualification conformance inspection groups A, B, C, or D (see 4.3 herein), the devices shall be programmed by the manufacturer prior to test in a checkerboard or similar pattern (a minimum of 50 percent of the total number of gates programmed).

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I. Unless otherwise specified, the values specified in table I are the preirradiation and postirradiation values. Postirradiation electrical measurements for any RHA level are tested at, T_A = +25°C.

3.5 Verification of erasure or programmed EPLD's. When specified, devices shall be verified as either programmed (see 4.7 herein) to the specified pattern or erased (see 4.6 herein). As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.6 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract.

3.6.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.3.1 and table IIA. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.6.2 Manufacturer programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

3.7 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.7.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.8 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.9 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.10 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.11 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.12 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

3.13 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein, over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request by the preparing or acquiring activity, along with the test data.

3.14 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitor. This reprogrammability test shall be done only for initial characterization and after any design or process changes, which may affect the reprogrammability of the device. The methods and procedures may be vendor specific but shall guarantee the number of program/erase endurance cycles listed in section 1.3 herein. This procedure shall be under document control and shall be made available upon request.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. Devices shall be burned-in containing a pattern that assures all inputs and I/Os are dynamically switched. This pattern must have all cells programmed in a high or low state (not neutralized).

c. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

d. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ V_{SS} = 0 V, -55°C ≤ T_C ≤ +125°C, 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
High level output voltage	V_{OH}	V_{CC} = 4.5 V, V_{IL} = 0.8 V, I_O = -4.0 mA, V_{IH} = 2.0 V	1, 2, 3	All	2.4		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, V_{IL} = 0.8 V, I_O = 6.0 mA, V_{IH} = 2.0 V	1, 2, 3	All		0.5	V
2/ High impedance output leakage current	I_{OZ}	V_{CC} = 5.5 V	1, 2, 3	All	-10	10	µA
High level input current	I_{IH}	V_{IH} = 5.5 V	1, 2, 3	All		25	µA
		V_{IH} = 2.4 V				10	
Low level input current	I_{IL}	V_{IL} = 0.4 V	1, 2, 3	All		-10	µA
		V_{IL} = GND				-10	
Supply current	I_{CC1}	Outputs open, V_{CC} = 5.5 V, V_{IN} = GND or V_{CC}	1, 2, 3	01-03		180	mA
				04,05		210	
				06,07		85	
Standby supply current	I_{CC2}	V_{CC} = 5.5 V, V_{IN} = GND or V_{CC}, Outputs open	1, 2, 3	03,05		10	mA
				07		5	
Output short circuit current 3/ 4/	I_{OS}	V_{CC} = 5.5 V, V_O = 0.5 V	1, 2, 3	01-03	-25	-90	mA
				04-07	-25	-120	
Input capacitance	C_I 4/ 5/	V_I = 0 V, V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz (see 4.4.1e)	4	All		20	pF
Output capacitance	C_O 4/ 5/	V_O = 0 V, V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz (see 4.4.1e)	4	All		12	pF
Functional tests		see 4.4.1c	7,8A,8B	All			
Input to output enable	t_{EA}	V_{CC} = 4.5 V, C_L = 5 pF, see figures 5 and 6 (circuit A)	9, 10, 11	01,03		35	ns
				02,06		25	
				04		15	
				05		20	
				07		30	
Input to output disable	t_{ER}		9, 10, 11	01,03		35	ns
				02,06		25	
				04		15	
				05		20	
				07		30	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ V_{SS} = 0 V, -55°C ≤ T_C ≤ +125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Input or feedback to nonregistered output	t_{PD}	V_{CC} = 4.5 V, C_L = * pF, see figures 4 and 5 (* circuit B or C as applicable)	9, 10, 11	01,03		35	ns
				02,06		25	
				04		15	
				05		20	
				07		30	
Clock to output	t_{CO}		9, 10, 11	01,03		35	ns
				02,06		25	
				04		15	
				05		20	
				07		30	
Clock period (t_{CF} + t_{SF})	t_P	V_{CC} = 4.5 V, C_L = 5 pF, see figures 4 and 5 (circuit A)	9, 10, 11	01,03	35		ns
				02	25		
				04	17		
				05	24		
				06	28		
				07	30		
Clock pulse width	t_W	V_{CC} = 4.5 V, C_L = * pF, see figures 4 and 5 (* circuit B or C as applicable)	9, 10, 11	01	15		ns
				02	10		
				03	17		
				04	7.5		
				05	11		
				06	14		
				07	15		
Setup time 6/ output register	t_{SI1}		9, 10, 11	01	15		ns
				02	10		
				03	22		
				04	5		
				05	10		
				06	15		
				07	19		
Setup time 7/ 8/ buried register	t_{SI2}		9, 10, 11	01,02	5		ns
				03	22		
				04	5		
				05	10		
				06	15		
				07	19		
Clock to feedback 8/	t_{CF}		9, 10, 11	01	15	20	ns
				02	10	18	
				03	15	20	
				04	5	12	
				05	10	16	
				06	12	18	
				07	13	20	
Feedback setup time 8/	t_{SF}		9, 10, 11	01,03	15		ns
				02	7		
				04	5		
				05	8		
				06,07	10		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ V_{SS} = 0 V, -55°C ≤ T_C ≤ +125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Hold time	t_H	V_{CC} = 4.5 V, C_L = * pF, see figures 4 and 5 (* circuit B or C as applicable)	9, 10, 11	01,02, 04	5		ns
				05	10		
				06	12		
				07	13		
Hold time output register	t_{H1}		9, 10, 11	03	15		ns
Hold time 8/ buried register	t_{H2}		9, 10, 11	03	5		ns
Maximum clock frequency 4/ 6/	f_{MAX}		9, 10, 11	01,03		28	MHz
				02		40	
				04		66	
				05		45	
				06		36	
				07		33	
Asynchronous reset pulse width	t_{AW}		9, 10, 11	01,03	20		ns
				02	15		
				04	8		
				05	12		
				06	15		
				07	18		
Asynchronous reset recovery time	t_{AR}		9, 10, 11	01,03	20		ns
				02	15		
				04	8		
				05	12		
				06	15		
				07	18		
Asynchronous reset to registered output reset	t_{AP}		9, 10, 11	01,03		35	ns
				02		25	
				04		18	
				05		22	
				06		28	
				07		30	
Clock to output, input pin clock	t_{COS}		9, 10, 11	04		10	ns
				05		11	
				06		12	
				07		15	
Clock to feedback, input pin clock 8/	t_{CFS}		9, 10, 11	04	0	5	ns
				05	0	6	
				06	0	7	
				07	0	8	
Input setup time, input pin clock	t_{SIS}		9, 10, 11	04	9		ns
				05	14		
				06	20		
				07	23		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ V_{SS} = 0 V, -55°C ≤ T_C ≤ +125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Feedback setup time, input pin clock 8/	t_{SFS}	V_{CC} = 4.5 V, C_L = * pF, see figures 4 and 5 (* circuit B or C as applicable)	9, 10, 11	04	9		ns
				05	14		
				06	20		
				07	23		
Hold time, input pin clock	t_{HS}		9, 10, 11	04	0		ns
				05	0		
				06	0		
				07	0		
Clock width, input pin clock	t_{WS}		9, 10, 11	04	6		ns
				05	7		
				06	8		
				07	9		
Clock period, input pin clock	t_{PS}		9, 10, 11	04	12		ns
				05	14		
				06	16		
				07	18		
Maximum clock frequency input pin clock	f_{MAXS}		9, 10, 11	04		83	MHz
				05		71	
				06		62	
				07		55	
Asynchronous reset/ preset recovery time, input pin clock	t_{ARS}		9, 10, 11	04	12		ns
				05	15		
				06	20		
				07	25		
Feedback to non-registered output 8/	t_{PD2}		9, 10, 11	04		15	ns
				05		20	
				06		25	
				07		30	
Input to nonregistered feedback 8/	t_{PD3}		9, 10, 11	04		11	ns
				05		15	
				06		18	
				07		20	
Feedback to non-registered feedback 8/	t_{PD4}		9, 10, 11	04		11	ns
				05		15	
				06		18	
				07		20	
Feedback to output enable 8/	t_{EA2}	V_{CC} = 4.5 V, C_L = 5 pF see figures 4 and 5 (circuit A)	9, 10, 11	04		15	ns
				05		20	
				06		25	
				07		30	
Feedback to output disable 8/	t_{ER2}		9, 10, 11	04		15	ns
				05		20	
				06		25	
				07		30	

See footnotes at end of table

TABLE I. Electrical performance characteristics - Continued.

1/ All voltages are referenced to ground.
2/ I/O terminal leakage is the worst case of IIX or IOZ.
3/ Only one output shorted at a time.
4/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
5/ All pins not being tested are to be open.
6/ Test applies only to register outputs.
7/ Buried registers include all 24 Q2 registers and any of the 24 Q1 registers in macrocells configured as combinational.
8/ Values guaranteed by design and are not tested.

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7, 8A and 8B tests shall be sufficient to verifying the functionality of the device. These tests form a part of the vendors test tape and shall be maintained and available upon request. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

d. O/V (Latch up) tests shall be measured only for the initial qualification and after any process or design changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V, the procedures and circuit shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD78 may be used for reference.

e. Subgroup 4 (C_I and C_O measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

f. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted for groups B, C, and D testing).

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M.

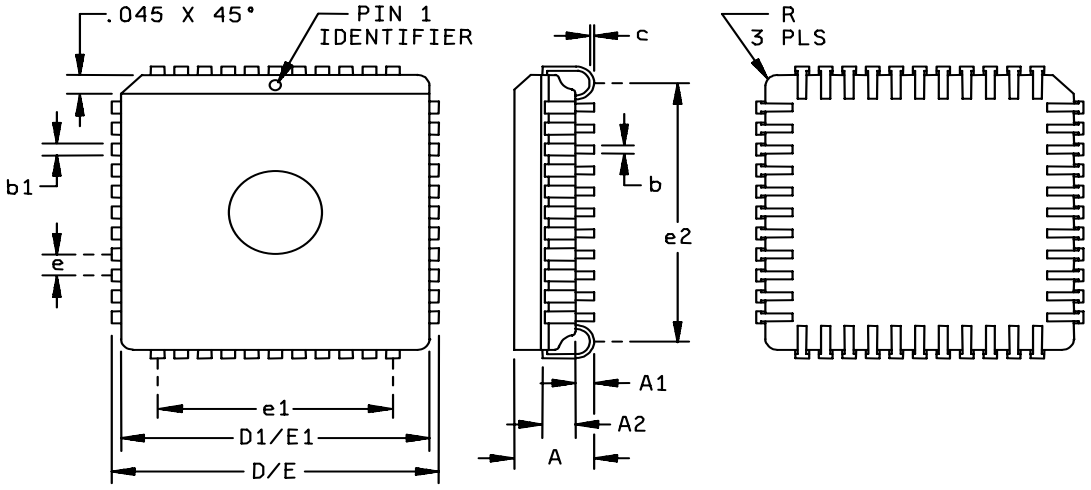
a. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as specified in method 1005 of MIL-STD-883.

Case outline Y



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	3.96	4.57	.156	.180
A1	0.89	1.14	.035	.045
A2	2.29	3.05	.090	.120
b	0.43	0.53	.017	.021
b1	0.71	0.81	.028	.032
c	0.20	0.25	.008	.010
D/E	17.40	17.70	.685	.695
D1/E1	16.40	16.90	.645	.665
e	1.27 BSC		.050 BSC	
e1	12.70 BSC		.500 BSC	
e2	15.00	16.00	.590	.630
N	44			

NOTE: Although dimensions are in inches, the US government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the two, the inch-pound units shall take precedence. Metric equivalents are for general information only.

Coplanarity is .008 inches (8 mil) with lead finish applied.

FIGURE 1. Case outlines.

Device types	All	01,02,03	04, 05, 06, and 07
Case outlines	Q	X, Y	X, Y
Terminal number	Terminal symbol		
1	I	I	I
2	I	I	I
3	I	I	I
4	I/O	NC	GND 1/
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	I/O	I/O	I/O
10	V_{CC}	I/O	I/O
11	I/O	V_{CC}	V_{CC}
12	I/O	V_{CC}	V_{CC}
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	I	I/O	I/O
18	I	I/O	I/O
19	I	I	I
20	I	I	I
21	I	I	I
22	I	I	I
23	I	I	I
24	I/O	I	I
25	I/O	I	I
26	I/O	NC	GND 1/
27	I/O	I/O	I/O
28	I/O	I/O	I/O
29	I/O	I/O	I/O
30	GND	I/O	I/O
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	GND	GND
34	I/O	GND	GND
35	I/O	I/O	I/O
36	I/O	I/O	I/O
37	I	I/O	I/O
38	I	I/O	I/O
39	I	I/O	I/O
40	I	I/O	I/O
41	- - -	I	I
42	- - -	I	I
43	- - -	I	I
44	- - -	I	I

1/ Original draft and revisions A through E showed terminals 4 and 26 for devices 04 through 07 to be a NC vs. the correct GND designation.

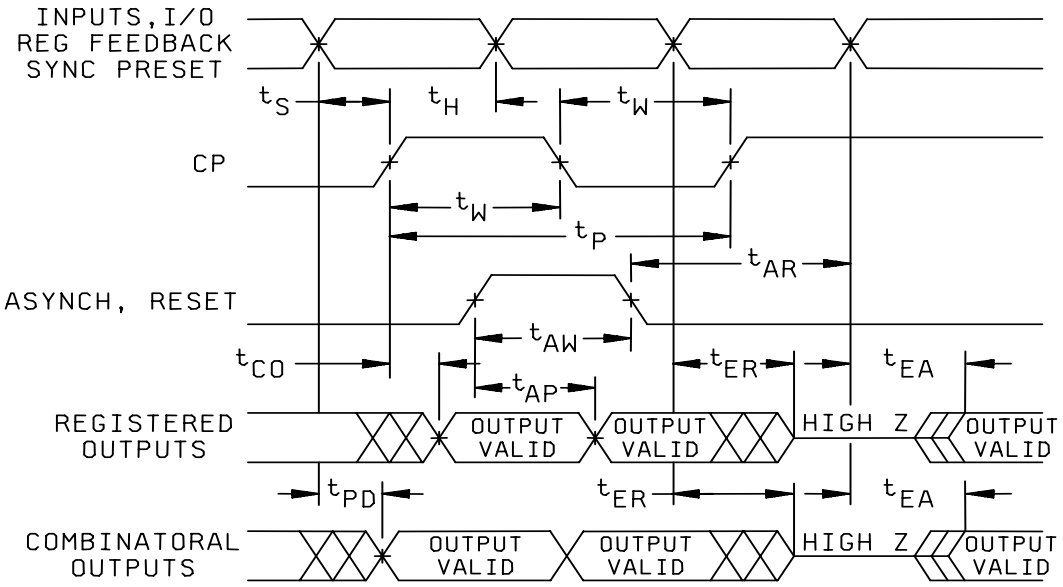
FIGURE 2. Terminal connections.

Input pins														Output pins											
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
X	X	X	X	X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

Output pins - continued											
I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

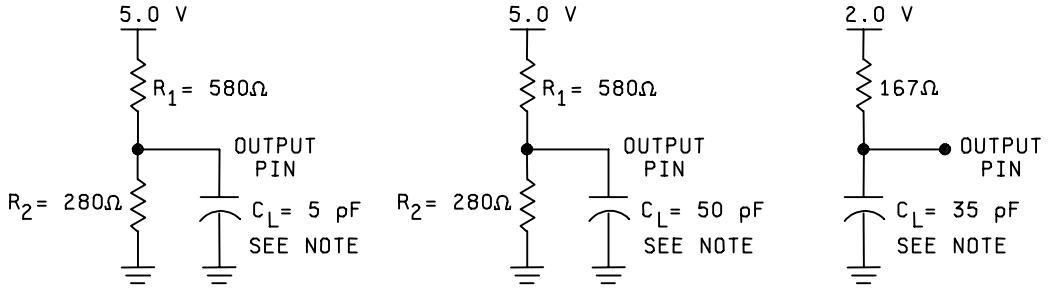
X = Don't care state
Z = Three-state

FIGURE 3. Truth table.



NOTE: Timing measurement reference is 1.5 V. Unless otherwise specified, input ac driving levels are 0.0 V and 3.0 V.

FIGURE 4. Timing waveforms.



NOTE: Including scope and jig (minimum value).

FIGURE 5. Load circuits.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (per method 5005, table I)	Subgroups (per MIL-PRF-38535, table III)	
		Device Class M	Device Class Q	Device Class V
1	Interim electrical parameters (see 4.2)			1,7,9
2	Static burn-in I and II method 1015	Required 8/	Required 8/	Required 8/
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Not Required	Not Required	Not Required
5	Same as line 1			1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11
7	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B	1,2,3,7, 8A,8B,9,10, 11 Δ
9	Group D end-point electrical parameters	2,3, 8A,8B	2,3, 8A,8B	2,3, 8A,8B
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroups 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1). For device classes Q and V performance of delta limits shall be as specified in the manufacturer's QM plan.
7/ See 4.4.1d.
8/ Either static or dynamic burn-in may be performed.

TABLE IIB. Delta limits at +25°C.

Test 1/	All device types
I_{IH}	±1.0 µA of specified value in table I
I_{IL}	±1.0 µA of specified value in table I
I_{OZ}	±1.0 µA of specified value in table I

1/ The above parameters shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after life test perform final electrical parameter tests, subgroups 1, 7, 9.

4.6 Erasing procedures. The recommended erasure procedure is exposure to short-wave ultraviolet light which has a wavelength of 2,537 Angstroms (Ä). The integrated dose (i.e., ultraviolet intensity times exposure time) for erasure should be minimum of 15 Ws/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000 uW/cm^2 power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7,258 ws/cm^2 (1 week at 12,000 uW/cm^2). Exposure of the device to high intensity ultraviolet light for long periods may cause permanent damage.

4.7 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing are intended for use for government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

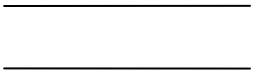
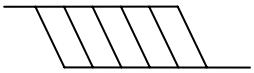
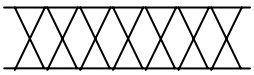
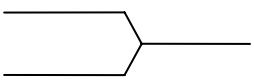
6.3 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-STD-1331, and as follows.

C_I C_O ..... Input and bidirectional output, terminal-to-GND capacitance.
GND ..... Ground zero voltage potential.
I_{CC} ..... Supply current.
I_{LI} ..... Input leakage current.
I_{LO} ..... Output leakage current.
T_C ..... Case temperature.
T_A ..... Ambient temperature.
V_{CC} ..... Positive supply voltage.
O/V ..... Latch-up over-voltage
O/I ..... Latch-up over current

6.5.1 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-08-03

Approved sources of supply for SMD 5962-91545 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE Number	Vendor similar PIN 3/
5962-9154501MQA	2/	ATV2500H-35DM/883
5962-9154501MXA	2/	ATV2500H-35LM/883
5962-9154501MYA	2/	ATV2500H-35KM/883
5962-9154502MQA	2/	ATV2500H-25DM/883
5962-9154502MXA	2/	ATV2500H-25LM/883
5962-9154502MYA	2/	ATV2500H-25KM/883
5962-9154503MQA	2/	ATV2500L-30DM/883
5962-9154503MXA	2/	ATV2500L-30LM/883
5962-9154503MYA	2/	ATV2500L-30KM/883
5962-9154504MXA	2/	ATV2500B-15LM/883
5962-9154504MYA	2/	ATV2500B-15KM/883
5962-9154505MXA	2/	ATV2500BL-20LM/883
5962-9154505MYA	2/	ATV2500BL-20KM/883

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 3/
5962-9154506MQA	0C7V7 2/	QPV2500BQ-25DM/883 ATV2500BQ-25DM/883
5962-9154506MXA	0C7V7 2/	QPV2500BQ-25LM/883 ATV2500BQ-25LM/883
5962-9154506MYA	0C7V7 2/	QPV2500BQ-25KM/883 ATV2500BQ-25KM/883
5962-9154507MQA	2/	ATV2500BQL-30DM/883
5962-9154507MXA	2/	ATV2500BQL-30LM/883
5962-9154507MYA	2/	ATV2500BQL-30KM/883

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Not available from an approved source.

3/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Ct. Santa Clara, CA 95051-0812

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.