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1.0 GENERAL DESCRIPTION

Microchip's USB83340 is a Hi-Speed USB 2.0 transceiver that provides a configurable physical layer (PHY) solution well suited for automotive applications.

The frequency of the reference clock is user selectable. The USB83340 includes an internal oscillator that may be used with either a quartz crystal or a ceramic resonator. Alternatively, the crystal input can be driven by an external clock oscillator. Another option is the use of a 60 MHz external clock when using the ULPI Clock In mode.

Several advanced features make the USB83340 the transceiver of choice by reducing both eBOM part count and printed circuit board (PCB) area. Outstanding ESD robustness eliminates the need for external ESD protection devices in typical applications. The internal Over-Voltage Protection circuit (OVP) protects the USB83340 from voltages up to 30 V on the **VBUS** pin. By using a reference clock from the Link, the USB83340 removes the cost of a dedicated crystal reference from the design, and the integrated USB switch enables unique product features with a single USB port of connection. The USB83340 includes integrated 3.3 V and 1.8 V regulators, making it possible to operate the device from a single power supply.

The USB83340 is optimized for use in applications where a low operating current and standby currents are essential. The USB83340 operates from a single supply and includes integrated regulators for its supplies. The USB83340 also supports the Link Power Management protocol (LPM) to further reduce USB operating currents.

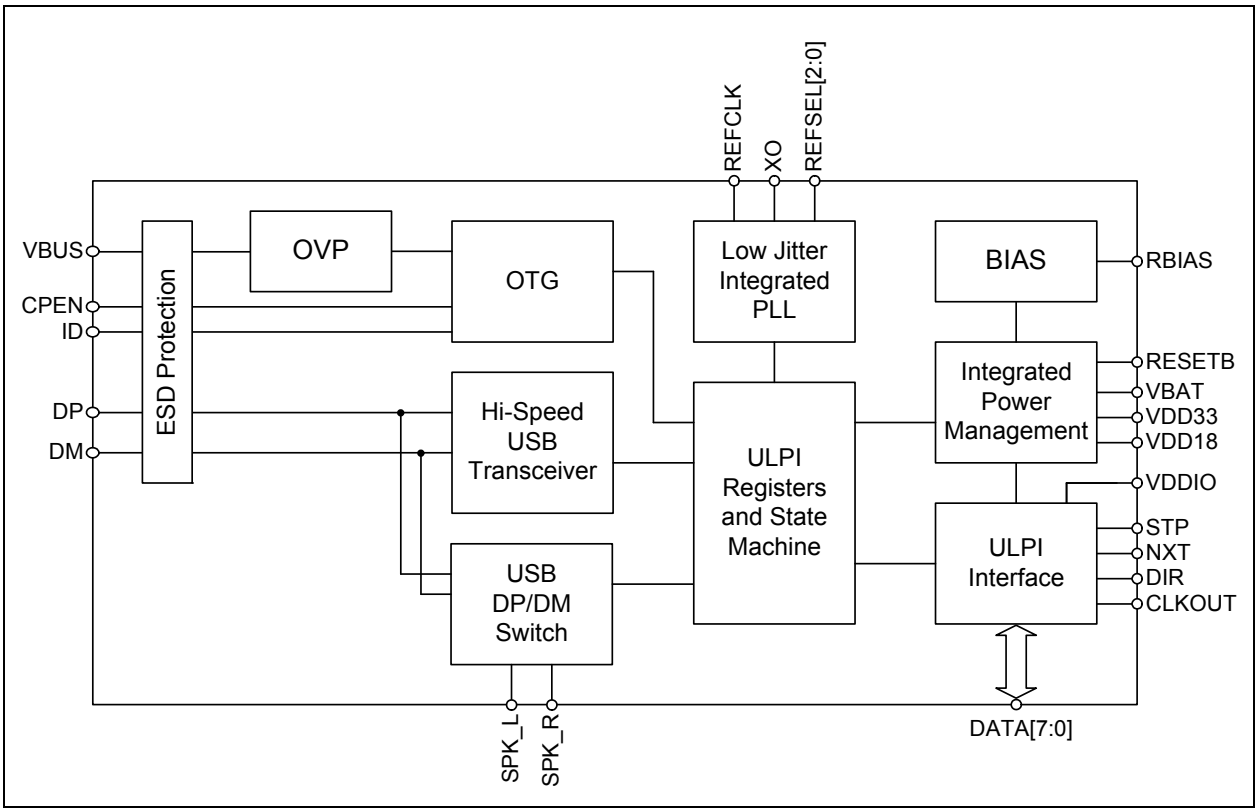
The USB83340 also includes integrated battery charger detection circuitry. These circuits are used to detect the attachment of a USB Charger as described in Section 5.8. By sensing the attachment to a USB Charger, a product using the USB83340 can draw more than 500 mA from the USB connector.

The USB83340 meets all of the electrical requirements for a Hi-Speed USB host, device, or an On-the-Go (OTG) transceiver. In addition to the supporting USB signaling, the USB83340 also provides USB UART Mode and USB Audio Mode.

USB83340 uses the industry standard UTMI+ Low Pin Interface (ULPI) to connect the USB PHY to the Link. ULPI uses a method of in-band signaling and status byte transfers between the Link and PHY to facilitate a USB session with only twelve pins.

The USB83340 uses Microchip's "wrapper-less" technology to implement the ULPI interface. This "wrapper-less" technology allows the PHY to achieve a low latency transmit and receive time. Microchip's low latency transceiver allows an existing UTMI Link to be reused by adding a UTMI to ULPI bridge. By adding a bridge to the ASIC the existing and proven UTMI Link IP can be reused.

FIGURE 1-1: USB83340 BLOCK DIAGRAM



The USB83340 includes an integrated 3.3 V LDO regulator that may optionally be used to generate 3.3 V from power applied to the **VBAT** pin. The voltage on the **VBAT** pin can range from 4.5 to 5.5 V. The **VBAT** and **VDD33** pins should *never* be connected together.

In USB UART Mode, the USB83340 **DP** and **DM** pins are redefined to enable pass-through of asynchronous serial data. The USB83340 will enter UART Mode when programmed, as described in Section 6.7.1.

In USB Audio Mode, a switch connects the **DP** pin to the **SPK_R** pin, and another switch connects he **DM** pin to the **SPK_L** pin. These switches are shown in the lower left-hand corner of Figure 5-1. The USB83340 can be configured to enter USB Audio Mode as described in Section 6.7.2. In addition, these switches are on when the **RESETB** pin of the USB83340 is asserted. The USB Audio Mode enables audio signaling from a single USB port of connection, and the switches may also be used to connect Full-Speed USB from another transceiver to the USB connector.

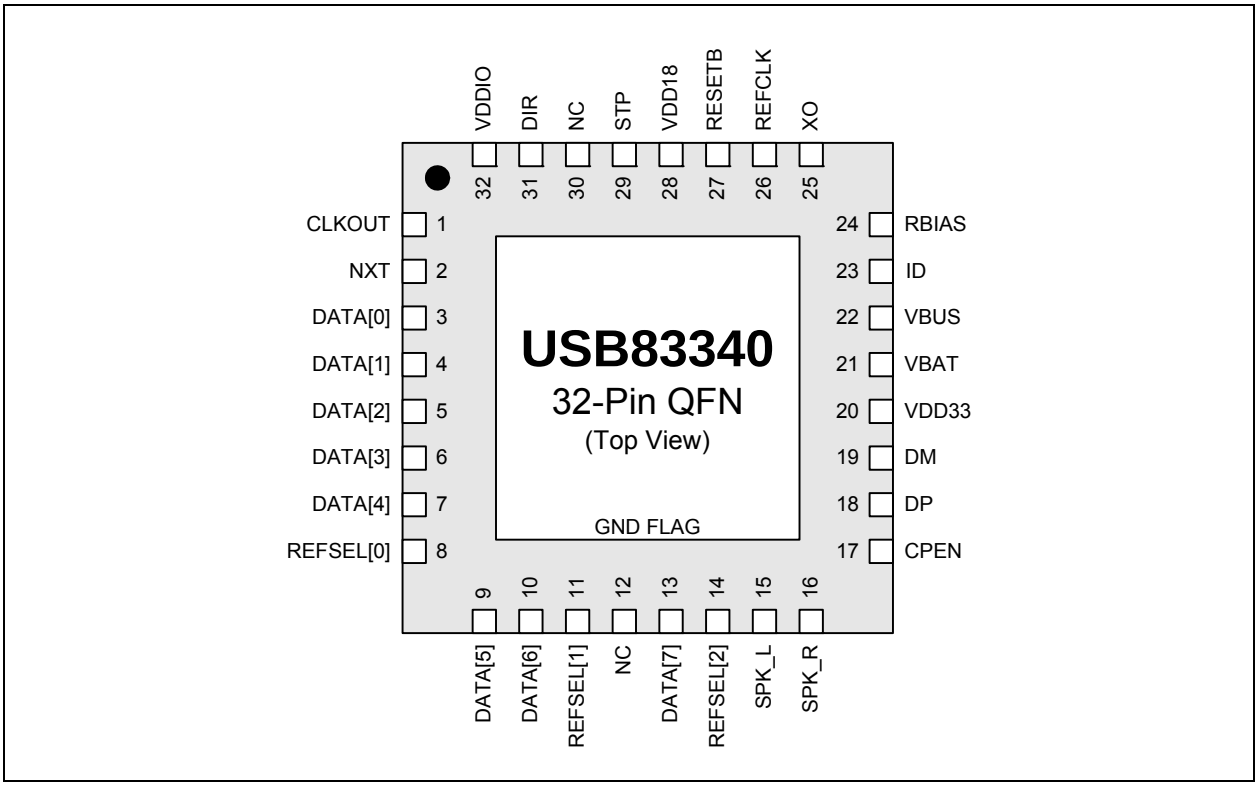
2.0 USB83340 PIN LOCATIONS AND DEFINITIONS

2.1 USB83340 Pin Locations and Descriptions

2.1.1 USB83340 PIN DIAGRAM

The illustration below is viewed from the top of the package.

FIGURE 2-1: USB83340 PIN LOCATIONS (TOP VIEW)



2.1.2 PIN DEFINITIONS

The following table details the pin definitions for the figure above.

TABLE 2-1: USB83340 PIN DESCRIPTIONS

Pin	Name	Direction/ Type	Active Level	Description
1	CLKOUT	Output, CMOS	N/A	**ULPI Clock Out Mode:** 60 MHz ULPI clock output. All ULPI signals are driven synchronously to the rising edge of this clock. **ULPI Clock In Mode:** Connect this pin to **VDDIO** to configure 60 MHz ULPI Clock IN mode as described in Section 5.4.1.
2	NXT	Output, CMOS	High	The PHY asserts **NXT** to throttle the data. When the Link is sending data to the PHY, **NXT** indicates when the current byte has been accepted by the PHY.
3	DATA[0]	I/O, CMOS	N/A	ULPI bi-directional data bus. **DATA[0]** is the LSB.
4	DATA[1]	I/O, CMOS	N/A	ULPI bi-directional data bus.
5	DATA[2]	I/O, CMOS	N/A	ULPI bi-directional data bus.
6	DATA[3]	I/O, CMOS	N/A	ULPI bi-directional data bus.
7	DATA[4]	I/O, CMOS	N/A	ULPI bi-directional data bus.
8	REFSEL[0]	Input	N/A	Used to select xtal/reference frequency. This pad is connected to **VDDIO** or **GND**.
9	DATA[5]	I/O, CMOS	N/A	ULPI bi-directional data bus.
10	DATA[6]	I/O, CMOS	N/A	ULPI bi-directional data bus.
11	REFSEL[1]	Input	N/A	Used to select xtal/reference frequency. This pad is connected to **VDDIO** or **GND**.
12	NC			No connect. Leave pin floating
13	DATA[7]	I/O, CMOS	N/A	ULPI bi-directional data bus. **DATA[7]** is the MSB.
14	REFSEL[2]	Input	N/A	Used to select xtal/reference frequency. This pad is connected to **VDDIO** or **GND**.
15	SPK_L	I/O, Analog	N/A	USB switch in/out for **DM** signals.
16	SPK_R	I/O, Analog	N/A	USB switch in/out for **DP** signals.
17	CPEN	Output, CMOS	High	External 5 V supply enable. This pin is used to enable the external VBUS power supply. The **CPEN** pin is low on POR. This pad uses **VDD33** logic level.

TABLE 2-1: USB83340 PIN DESCRIPTIONS

Pin	Name	Direction/ Type	Active Level	Description
18	DP	I/O, Analog	N/A	D+ pin of the USB cable.
19	DM	I/O, Analog	N/A	D- pin of the USB cable.
20	VDD33	Power	N/A	3.3 V Regulator Output. A 1.0 µF (<1 Ω ESR) bypass capacitor to ground is required for regulator stability. The bypass capacitor should be placed as close as possible to the USB83340.
21	VBAT	Power	N/A	Regulator input. The regulator supply can be from 5.5 V to 4.5 V.
22	VBUS	I/O, Analog	N/A	This pin is used for the VBUS comparator inputs and for VBUS pulsing during session request protocol. An external resistor, R_{VBUS}, is required between this pin and the USB connector.
23	ID	Input, Analog	N/A	For device applications the **ID** pin is connected to **VDD33**. For host applications **ID** is grounded. For OTG applications the **ID** pin is connected to the USB connector.
24	RBIAS	Analog, CMOS	N/A	Bias resistor pin. This pin requires an 8.06 kΩ (±1%) resistor to ground, placed as close as possible to the USB83340. Nominal voltage during ULPI operation is 0.8 V.
25	XO	Output, Analog	N/A	Crystal pin. If using an external clock on XI this pin should be floated.
26	REFCLK	Input, CMOS	N/A	**ULPI Clock Out Mode:** Model-specific reference clock or XI (crystal in) pin. **ULPI Clock In Mode:** 60 MHz ULPI clock input.
27	RESETB	Input, CMOS,	Low	When low, the part is suspended and the 3.3 V and 1.8 V regulators are disabled. When high, the USB83340 will operate as a normal ULPI device, as described in Section 5.5.2. The state of this pin may be changed asynchronously to the clock signals. When asserted for a minimum of 1 microsecond and then de-asserted, the ULPI registers are reset to their default state and all internal state machines are reset.
28	VDD18	Power	N/A	1.8 V regulator output. A 1.0 µF (<1 Ω ESR) bypass capacitor to ground is required for regulator stability. The bypass capacitor should be placed as close as possible to the USB83340.
29	STP	Input, CMOS	High	The Link asserts **STP** for one clock cycle to stop the data stream currently on the bus. If the Link is sending data to the PHY, **STP** indicates the last byte of data was on the bus in the previous cycle.
30	NC	N/A	N/A	No connect.

TABLE 2-1: USB83340 PIN DESCRIPTIONS

Pin	Name	Direction/ Type	Active Level	Description
31	DIR	Output, CMOS	N/A	Controls the direction of the data bus. When the PHY has data to transfer to the Link, it drives **DIR** high to take ownership of the bus. When the PHY has no data to transfer it drives **DIR** low and monitors the bus for commands from the Link.
32	VDDIO	Power	N/A	1.8 V to 3.3 V ULPI interface supply voltage.
FLAG	GND	Ground	N/A	Ground.

3.0 LIMITING VALUES

3.1 Absolute Maximum Ratings

TABLE 3-1: ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VBUS, **VBAT**, **ID**, **DP**, **DM**, **SPK_L**, and **SPK_R** voltage to **GND**	V_{MAX_5V}	Voltage measured at pin. **VBUS** tolerant to 30 V with external R_{VBUS}.	-0.5		+6.0	V
Maximum **VDDIO** voltage to **GND**	V_{MAX_IOV}	**VDD18** = V_{DD18}	-0.5		4.0	V
Maximum **VDDIO** voltage to **GND**	V_{MAX_IOV}	**VDD18** = 0 V	-0.5		0.7	V
Maximum I/O voltage to **GND**	V_{MAX_IN}		-0.5		V_{DDIO} + 0.7	V
Storage Temperature	T_{MAX_STG}		-55		+150	°C

Note: Absolute maximum ratings at 25 °C. Stresses beyond the specified parameters in Table 3-1, "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions may affect device reliability.

3.2 Recommended Operating Conditions

TABLE 3-2: RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VBAT to **GND**	V_{BAT}		4.5		5.5	V
VDDIO to **GND**	V_{DDIO}	Note 1	1.6	1.8-3.3	3.6	V
Input Voltage on Digital Pins (**RESETB**, **STP**, **DIR**, **NXT**, **DATA[7:0]**)	V_I		0.0		V_{DDIO}	V
Voltage on Analog I/O Pins (**DP**, **DM**, **ID**, **CPEN**, **SPK_L**, **SPK_R**)	$V_{I(I/O)}$		0.0		V_{DD33}	V
VBUS to **GND**	V_{VMAX}		0.0		5.5	V
Operating Temperature	T_A	Note 2	-40		+105	°C

Note 1: **VDDIO** must be equal to or greater than **VDD18**(min).

2: Junction temperature must not exceed +125 °C

4.0 ELECTRICAL CHARACTERISTICS

4.1 Operating Current

TABLE 4-1: OPERATING CURRENT

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Synchronous Mode Current (Default configuration)	$I_{VBAT(SYNC)}$	USB Idle		24		mA
	$I_{VIO(SYNC)}$			5		
Synchronous Mode Current (HS USB operation)	$I_{VBAT(HS)}$	Active USB Transfer		56	70	mA
	$I_{VIO(HS)}$			10	20	mA
Synchronous Mode Current (FS/LS USB operation)	$I_{VBAT(FS)}$	Active USB Transfer		30		mA
	$I_{VIO(FS)}$			9		mA
Serial Mode Current (FS/LS USB) Note 1	$I_{VBAT(FS\_S)}$			7.7		mA
	$I_{VIO(FS\_S)}$					
USB UART Current Note 1	$I_{VBAT(UART)}$			7.6		mA
	$I_{VIO(UART)}$					
Low Power Mode Note 2	$I_{VBAT(SUSPEND)}$			48		µA
	$I_{VIO(SUSPEND)}$	VDDIO = 1.6 V		2.8		µA
	$I_{VIO(SUSPEND)}$	VDDIO = 3.6 V		368		µA
RESET Mode	$I_{VBAT(RSTB)}$	**RESETB** = 0 V_{VBAT} = 4.5 to 5.5		5	20	µA
	$I_{VIO(RSTB)}$			3	10	µA

Note 1: *ClockSuspendM* bit = 0.

2: SessEnd, VbusVld, and IdFloat comparators disabled. STP interface protection disabled.

3: Device outputs not loaded.

4.2 Clock Specifications

TABLE 4-2: CLOCK SPECIFICATIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Suspend Recovery Time	T_{START}	LPM Enable = 0	1.0	1.1	1.2	ms
	T_{START_LPM}	LPM Enable = 1	125		150	µs
PHY Preparation Time 60 MHz **REFCLK**	T_{PREP}	LPM Enable = 0	1.0	1.1	1.2	ms
CLKOUT Duty Cycle	DC_{CLKOUT}	ULPI Clock In Mode	40		60	%
REFCLK Duty Cycle	DC_{REFCLK}		25		75	%
REFCLK Frequency Accuracy	F_{REFCLK}		-500		+500	PPM

Note: T_{START} and T_{PREP} are measured from the time when **REFCLK** and **RESETB** are both valid to when the USB83340 de-asserts **DIR**.

Note: The USB83340 uses the *AutoResume* feature, Section 6.4.1.4, to allow a host start-up time of less than 1 ms.

4.3 ULPI Interface Timing

TABLE 4-3: ULPI INTERFACE TIMING

Parameter	Symbol	Conditions	Min	Max	Units
60 MHz ULPI Output Clock Note 4					
Setup Time (**STP**, data in)	T_{SC}, T_{SD}	Model-specific **REFCLK**	5.0		ns
Hold Time (**STP**, data in)	T_{HC}, T_{HD}	Model-specific **REFCLK**	0.0		ns
Output Delay (control out, 8-bit data out)	T_{DC}, T_{DD}	Model-specific **REFCLK**	1.5	9	ns
60 MHz ULPI Input Clock					
Setup Time (**STP**, data in)	T_{SC}, T_{SD}	60 MHz **REFCLK**	1.5		ns
Hold Time (**STP**, data in)	T_{HC}, T_{HD}	60 MHz **REFCLK**	1.5		ns
Output Delay (control out, 8-bit data out)	T_{DC}, T_{DD}	60 MHz **REFCLK**	1.0	6.0	ns

Note: C_{Load} = 10 pF.

4: **REFCLK** does not need to be aligned in any way to the ULPI signals.

4.4 Digital IO Pins

TABLE 4-4: DIGITAL IO CHARACTERISTICS: RESETB, STP, DIR, NXT, DATA[7:0], AND REFCLK PINS

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Low-Level Input Voltage	V_{IL}		V_{SS}		0.57	V
High-Level Input Voltage	V_{IH}		0.77 * V_{DDIO}		V_{DDIO}	V
High-Level Input Voltage **REFCLK** and **RESETB**	V_{IH_REF}		0.68 * V_{DDIO}		V_{DD33}	V
Low-Level Output Voltage	V_{OL}	I_{OL} = 8 mA			0.4	V
High-Level Output Voltage	V_{OH}	I_{OH} = -8 mA	V_{DDIO} - 0.6			V
Output Rise Time	T_{ORISE}	C_{LOAD} = 10 pF		1.3		ns
Output Fall Time	T_{OFALL}	C_{LOAD} = 10 pF		1.3		ns
Input Leakage Current	I_{LI}				±10	µA
Pin Capacitance	Cpin				4	pF
STP Pull-up Resistance	R_{STP}	InterfaceProtectDisable = 0	55	60	80	kΩ
DATA[7:0] Pull-down Resistance	R_{DATA_PD}	ULPI Synchronous Mode	55	73	85	kΩ
CLKOUT External Drive	V_{IH_ED}	At start-up or following reset			0.4 * V_{DDIO}	V

4.5 Analog I/O Pins Characteristics

The Microchip device conforms to all voltage, power, and timing characteristics and specifications as set forth in the USB 2.0 specification including applicable erratas and ECNs. Please refer to the USB 2.0 specification for more information.

4.6 VBUS Electrical Characteristics

The Microchip device conforms to all voltage, power, and timing characteristics and specifications as set forth in the USB 2.0 specification including applicable erratas and ECNs. Please refer to the USB 2.0 specification for more information.

4.7 ID Electrical Characteristics

TABLE 4-5: ID ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Min	Typ	Max	Units
ID Ground Trip Point	V_{IdGnd}		0.4	0.7	0.9	V
ID Float Trip Point	$V_{IdFloat}$		1.6	2.2	2.5	V
ID Pull-up Resistance	R_{ID}	IdPullup = 1	80	100	120	kΩ
ID Weak Pull-up Resistance	R_{IDW}	IdPullup = 0	1			MΩ
ID Pull-down Resistance	R_{IDPD}	IdGndDrv = 1			1000	Ω

4.8 USB Audio Switch Characteristics

TABLE 4-6: USB AUDIO SWITCH CHARACTERISTICS

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Minimum “ON” Resistance	R_{ON_Min}	$0 < V_{switch} < V_{DD33}$	2.7	5	5.8	Ω
Maximum “ON” Resistance	R_{ON_Max}	$0 < V_{switch} < V_{DD33}$	4.5	7	13	Ω
Minimum “OFF” Resistance	R_{OFF_Min}	$0 < V_{switch} < V_{DD33}$	1			MΩ

4.9 USB Charger Detection Characteristics

The Microchip device conforms to all voltage, power, and timing characteristics and specifications as set forth in the USB Battery Charging Specification 1.2. Please refer to the USB Battery Charging Specification 1.2 for more information.

4.10 Regulator Output Voltages and Capacitor Requirement

TABLE 4-7: REGULATOR OUTPUT VOLTAGES AND CAPACITOR REQUIREMENT

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Regulator Output Voltage	V_{DD33}	5.5 V > **VBAT** > 4.5 V	2.97	3.3	3.6	V
		USB UART Mode & UART RegOutput[1:0] = 01 5.5 V > VBAT > 4.5 V	2.7	3.0	3.3	V
		USB UART Mode & UART RegOutput[1:0] = 10 5.5 V > VBAT > 4.5 V	2.47	2.75	3.03	V
		USB UART Mode & UART RegOutput[1:0] = 11 5.5 V > VBAT > 4.5 V	2.25	2.5	2.75	V
Regulator Bypass Capacitor	C_{OUT33}		1.0		10	µF
Bypass Capacitor ESR	C_{ESR33}				1	Ω
Regulator Output Voltage	V_{DD18}	3.6 V > **VBAT** > 2.25 V	1.62	1.8	1.98	V
Regulator Bypass Capacitor	C_{OUT18}		1.0		10	µF
Bypass Capacitor ESR	C_{ESR18}				1	Ω

4.11 Piezoelectric Resonator for Internal Oscillator

The internal oscillator may be used with an external quartz crystal or ceramic resonator as described in Section 5.4.1.2. See Table 4-8 for the recommended crystal specifications.

TABLE 4-8: USB83340 QUARTZ CRYSTAL SPECIFICATIONS

Parameter	Symbol	Min	Nom	Max	Units	Notes
Crystal Cut	AT, typ					
Crystal Oscillation Mode	Fundamental Mode					
Crystal Calibration Mode	Parallel Resonant Mode					
Frequency	Ffund		Table 5-2		MHz	
Total Allowable PPM Budget				±500	PPM	Note 5
Drive Level	P_W	0.5			mW	
Equivalent Series Resistance	R_1			30	Ω	
Operating Temperature Range		-40		105	°C	
USB83340 **REFCLK** Pin Capacitance			3 typ		pF	Note 6
USB83340 **XO** Pin Capacitance			3 typ		pF	Note 6
Crystal Load Capacitance	C_L			18	pF	Note 7

5: The required bit rate accuracy for Hi-Speed USB applications is ±500 ppm as provided in the USB 2.0 Specification. This range takes into account the effect of voltage, temperature, aging, etc. For design purposes the crystal should be within ±50 ppm of the target frequency with crystal manufacturer's specified load capacitance at room temperature.

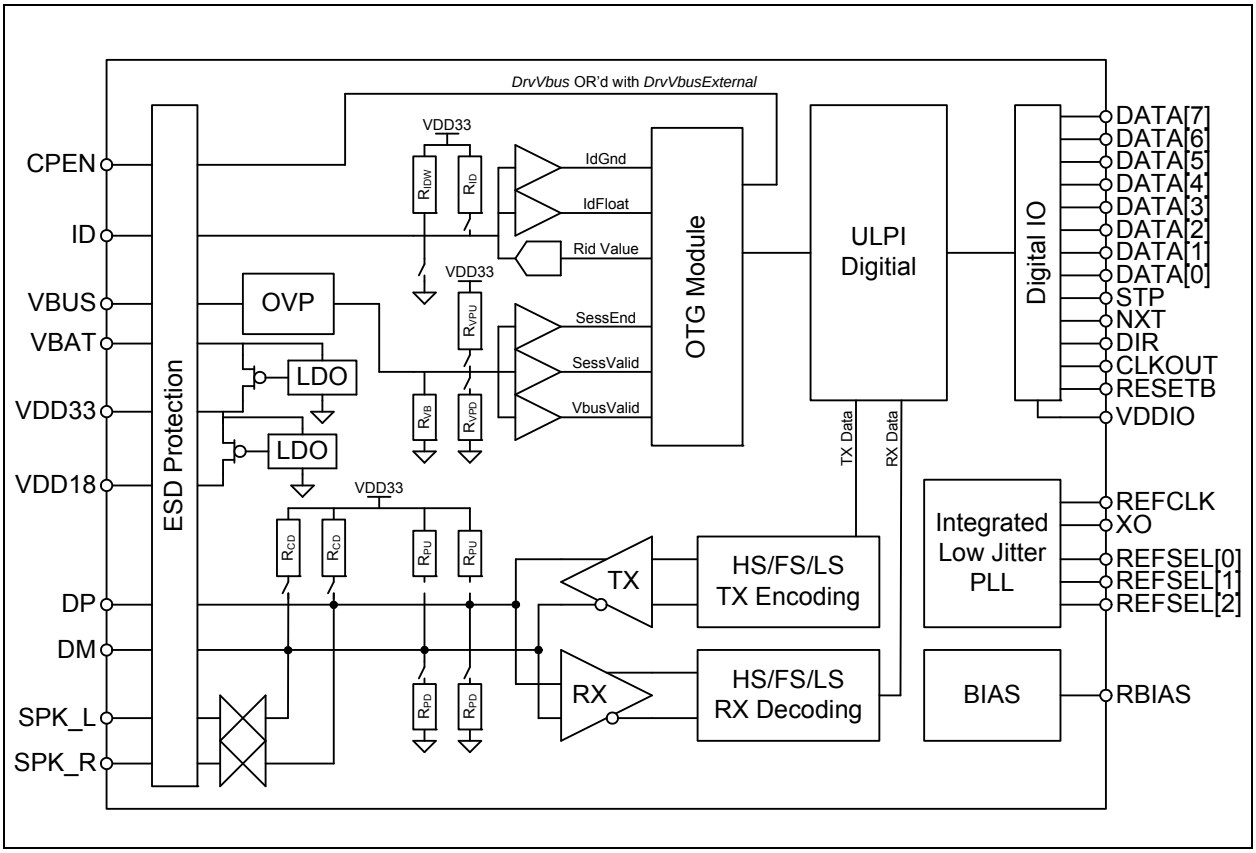
6: This number includes the pad, the bond wire and the lead frame. Printed Circuit Board (PCB) capacitance is not included in this value. The PCB capacitance value and the capacitance value of the XO and REFCLK pins are required to accurately calculate the value of the two external load capacitors.

7: The value of on-board capacitors must account for chip pin capacitance and PCB trace/pad capacitance. As an example, a crystal that requires 18 pF load would need two capacitors of 36 pF on each end of crystal. This capacitance will include the pin capacitance, and the PCB trace capacitance (typical value is 7 pF). Therefore the actual capacitors that must be installed on board to meet the 18 pF load requirement should be approximately 36-7-3 = 26 pF each. Given the relatively low tolerance requirement for USB base clock (+-500 ppm), the accuracy of this capacitor is not essential.

5.0 ARCHITECTURE OVERVIEW

The USB83340 consists of the blocks shown in the diagrams below

FIGURE 5-1: USB83340 SYSTEM DIAGRAM



5.1 ULPI Digital Operation and Interface

This section of the USB83340 is covered in detail in Chapter 6.0, ULPI Operation.

5.2 USB 2.0 Hi-Speed Transceiver

The blocks in the lower left-hand corner of Figure 5-1 interface to the DP/DM pins.

5.2.1 USB TRANSCEIVER

The USB83340 transceiver includes a Universal Serial Bus Specification Rev 2.0 compliant receiver and transmitter. The DP/DM signals in the USB cable connect directly to the receivers and transmitters.

The receiver consists of receivers for HS and FS/LS mode. Depending on the mode, the selected receiver provides the serial data stream through the multiplexer to the RX logic block. For HS mode support, the HS RX block contains a squelch circuit to insure that noise is not interpreted as data. The RX block also includes a single-ended receiver on each of the data lines to determine the correct FS linestate.

Data from the Link is encoded, bit stuffed, serialized and transmitted onto the USB cable by the transmitter. Separate differential FS/LS and HS transmitters are included to support all modes.

The USB83340 TX block meets the HS signaling level requirements in the USB 2.0 specification when the PCB traces from the **DP** and **DM** pins to the USB connector are correctly designed. In some systems the proper 90 ohm differential impedance cannot be maintained and it may be desirable to compensate for loss by adjusting the HS transmitter amplitude and this HS squelch threshold. The *PHYBoost* bits in the HS Compensation and LPM Register may be configured to adjust the HS transmitter amplitude at the **DP** and **DM** pins. The *VariSense* bits in the HS Compensation and LPM Register can also be used to lower the squelch threshold to compensate for losses on the PCB.

To ensure proper operation of the USB transceiver the settings of Table 5-1 must be followed.

5.2.2 TERMINATION RESISTORS

The USB83340 transceiver fully integrates all of the USB termination resistors on both **DP** and **DM**. This includes 1.5 kΩ pull-up resistors, 15 kΩ pull-down resistors and the 45 Ω high-speed termination resistors. These resistors require no tuning or trimming by the Link. The state of the resistors is determined by the operating mode of the transceiver when operating in Synchronous Mode.

The *XcvrSelect[1:0]*, *TermSelect* and *OpMode[1:0]* bits in the Function Control register, and the *DpPulldown* and *DmPulldown* bits in the OTG Control register control the configuration of the termination resistors. All possible valid resistor combinations are shown in Table 5-1, and operation is guaranteed in only the configurations shown. If a ULPI Register Setting is configured that does not match a setting in the table, the transceiver operation is not guaranteed and the settings in the last row of Table 5-1 will be used.

- RPU_DP_EN activates the 1.5 kΩ DP pull-up resistor.
- RPU_DM_EN activates the 1.5 kΩ DM pull-up resistor.
- RPD_DP_EN activates the 15 kΩ DP pull-down resistor.
- RPD_DM_EN activates the 15 kΩ DM pull-down resistor.
- HSTERM_EN activates the 45 Ω DP and DM high-speed termination resistors.

TABLE 5-1: DP/DM TERMINATION VS. SIGNALING MODE

Signaling Mode	ULPI Register Settings					USB83340 Termination Resistor Settings				
	XcvrSelect[1:0]	*TermSelect*	*OpMode[1:0]*	*DpPulldown*	*DmPulldown*	RPU_DP_EN	RPU_DM_EN	RPD_DP_EN	RPD_DM_EN	HSTERM_EN
General Settings										
Tri-State Drivers, Note 1	XXb	Xb	01b	Xb	Xb	0b	0b	0b	0b	0b
Power-up or VBUS < $V_{SESSEND}$	01b	0b	00b	1b	1b	0b	0b	1b	1b	0b
Host Settings										
Host Chirp	00b	0b	10b	1b	1b	0b	0b	1b	1b	1b
Host High-Speed	00b	0b	00b	1b	1b	0b	0b	1b	1b	1b
Host Full-Speed	X1b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host HS/FS Suspend	01b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host HS/FS Resume	01b	1b	10b	1b	1b	0b	0b	1b	1b	0b
Host Low-Speed	10b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host LS Suspend	10b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host LS Resume	10b	1b	10b	1b	1b	0b	0b	1b	1b	0b
Host Test J/Test K	00b	0b	10b	1b	1b	0b	0b	1b	1b	1b
Peripheral Settings										
Peripheral Chirp	00b	1b	10b	0b	0b	1b	0b	0b	0b	0b
Peripheral HS	00b	0b	00b	0b	0b	0b	0b	0b	0b	1b
Peripheral FS	01b	1b	00b	0b	0b	1b	0b	0b	0b	0b
Peripheral HS/FS Suspend	01b	1b	00b	0b	0b	1b	0b	0b	0b	0b
Peripheral HS/FS Resume	01b	1b	10b	0b	0b	1b	0b	0b	0b	0b
Peripheral LS	10b	1b	00b	0b	0b	0b	1b	0b	0b	0b
Peripheral LS Suspend	10b	1b	00b	0b	0b	0b	1b	0b	0b	0b
Peripheral LS Resume	10b	1b	10b	0b	0b	0b	1b	0b	0b	0b
Peripheral Test J/Test K	00b	0b	10b	0b	0b	0b	0b	0b	0b	1b
OTG device, Peripheral Chirp	00b	1b	10b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral HS	00b	0b	00b	0b	1b	0b	0b	0b	1b	1b
OTG device, Peripheral FS	01b	1b	00b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral HS/FS Suspend	01b	1b	00b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral HS/FS Resume	01b	1b	10b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral Test J/Test K	00b	0b	10b	0b	1b	0b	0b	0b	1b	1b
Charger Detection										
Connect Detect	01b	0b	00b	0b	1b	0b	0b	0b	1b	0b
Any combination not defined above, Note 2						0b	0b	1b	1b	0b

Note: This is equivalent to Table 40, Section 4.4 of the ULPI 1.1 specification.

Note: USB83340 does not support operation as an upstream hub port. See Section 6.4.1.3.

Note 1: When **RESETB** = 0 the HS termination will tri-state the USB drivers.

2: The transceiver operation is not guaranteed in a combination that is not defined.

The USB83340 uses the 27% resistor ECN resistor tolerances. The resistor values are stated in the USB 2.0 specification.

5.3 Bias Generator

This block consists of an internal band gap reference circuit used for generating the driver current and the biasing of the analog circuits. This block requires an external 8.06 kΩ, 1% tolerance, reference resistor connected from **RBIAS** to ground. This resistor should be placed as close as possible to the USB83340 to minimize the trace length. The nominal voltage at **RBIAS** is 0.8 V +/- 10% and therefore the resistor will dissipate approximately 80 µW of power.

5.4 Integrated Low Jitter PLL

The USB83340 uses an integrated low jitter Phase-Locked Loop (PLL) to provide a clean 480 MHz clock required for HS USB signal quality. This clock is used by the PHY during both transmit and receive. The USB83340 PLL requires an accurate frequency reference to be driven on the **REFCLK** pin.

5.4.1 REFCLK FREQUENCY SELECTION

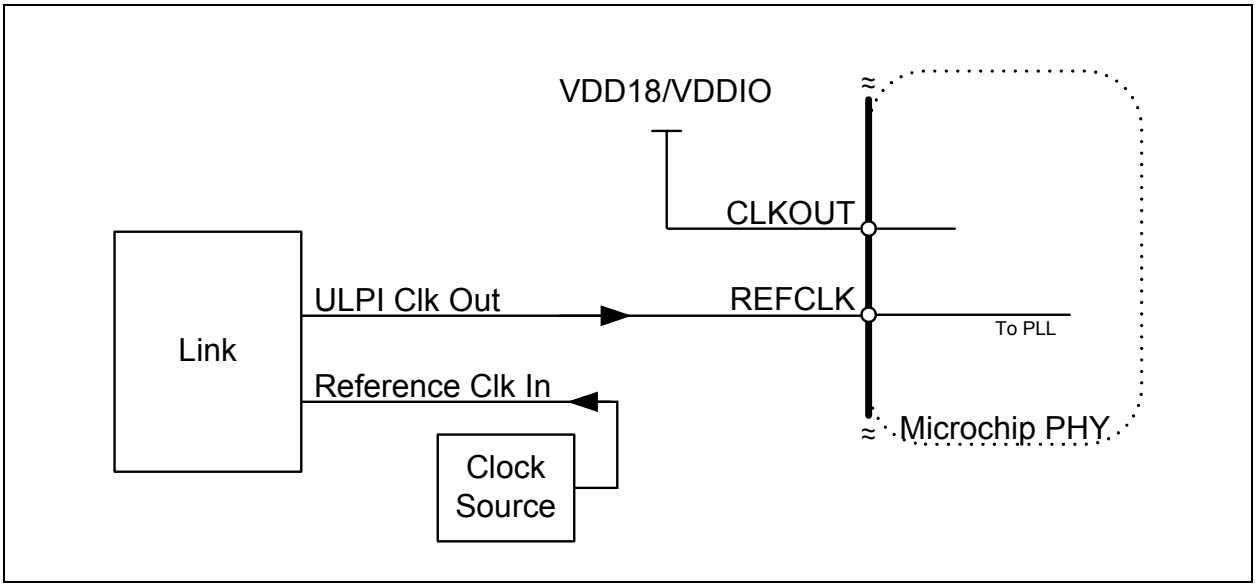
The USB83340 PLL is designed to operate in one of two reference clock modes. In the first mode, the 60 MHz ULPI clock is driven on the **REFCLK** pin. In the second mode a reference clock is driven on the **REFCLK** pin. The Link is driving the ULPI clock, in the first mode, and this is referred to as **ULPI Clock In Mode**. In the second mode, the USB83340 generates the ULPI clock, and this is referred to as **ULPI Clock Out Mode**.

During start-up, the USB83340 monitors the **CLKOUT** pin. If a connection to **VDDIO** is detected, the USB83340 is configured for a 60 MHz ULPI reference clock driven on the **REFCLK** pin. Section 5.4.1.1 and Section 5.4.1.2 describe how to configure the USB83340 for either ULPI Clock In Mode or ULPI Clock Out Mode.

5.4.1.1 ULPI Clock In Mode (60 MHz REFCLK Mode)

When using ULPI Clock In Mode, the Link must supply the 60 MHz ULPI clock to the USB83340. In this mode the 60 MHz ULPI clock is connected to the **REFCLK** pin, and the **CLKOUT** pin is tied high to **VDDIO**. An example of ULPI Clock In Mode is shown in Figure 8-2. After the PLL has locked to the correct frequency, the USB83340 will de-assert **DIR** and the Link can begin using the ULPI interface. The USB83340 is guaranteed to start the clock within the time specified in Table 4-2. For host applications, the ULPI *AutoResume* bit should be enabled. This is described in Section 6.4.1.4.

FIGURE 5-2: CONFIGURING THE USB83340 FOR ULPI CLOCK IN MODE (60 MHZ)



5.4.1.2 ULPI Clock Out Mode

When using ULPI Clock Out Mode, the USB83340 generates the 60 MHz ULPI clock used by the Link. In this mode, the **REFCLK** pin must be driven with the model-specific frequency, and the **CLKOUT** pin sources the 60 MHz ULPI clock to the Link. When using ULPI Clock Out Mode, the system must not drive the **CLKOUT** pin following POR or hardware reset with a voltage that exceeds the value of V_{IH_ED} provided in Table 4-4. An example of ULPI Clock Out Mode is shown in Figure 8-1.

After the PLL has locked to the correct frequency, the USB83340 generates the 60 MHz ULPI clock on the **CLKOUT** pin, and de-asserts **DIR** to indicate that the PLL is locked. The USB83340 is guaranteed to start the clock within the time specified in Table 4-2, and it will be accurate to within ±500 ppm. For host applications the ULPI *AutoResume* bit should be enabled. This is described in Section 6.4.1.4.

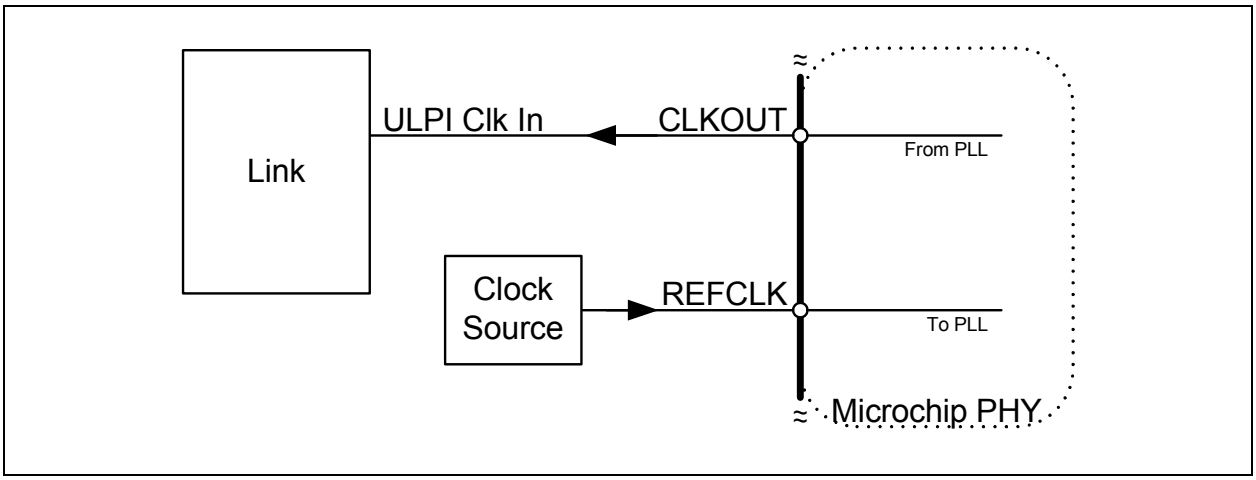
When using ULPI Clock Out Mode, the edges of the reference clock do not need to be aligned in any way to the ULPI interface signals. There is no need to align the phase of the **REFCLK** and the **CLKOUT**.

For the USB83340, the reference clock frequency required is determined by the settings of the REFSEL[2:0] pins. The pins should either be connected to **VDDIO** or **GND**. The reference frequency use is shown in Table 5-2.

TABLE 5-2: REFSEL[2:0] VS. REQUIRED FREQUENCY AT REFCLK (USB83340)

REFSEL[2:0]	REFCLK FREQUENCY
000	52 MHz
001	38.4 MHz
010	12 MHz
011	27 MHz
100	13 MHz
101	19.2 MHz
110	26 MHz
111	24 MHz

FIGURE 5-3: CONFIGURING THE USB83340 FOR ULPI CLOCK OUT MODE



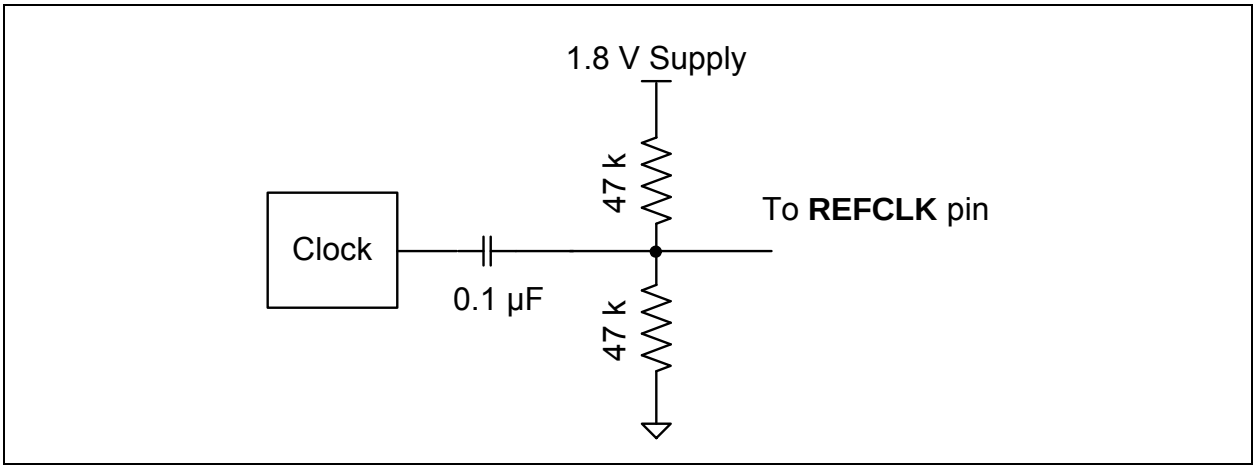
5.4.2 REFCLK AMPLITUDE

The reference clock should be connected to the **REFCLK** pin as shown in the application diagrams, Figure 8-1 and Figure 8-3. The **REFCLK** pin is designed to be driven with a square wave from 0 V to V_{DDIO}, but can be driven with a square wave from 0 V to as high as 3.6 V. The USB83340 uses only the positive edge of the **REFCLK**.

If a digital reference is not available, the **REFCLK** pin can be driven by an analog sine wave that is AC coupled into the **REFCLK** pin. If using an analog clock the DC bias should be set at the mid-point of the **VDD18** supply using a bias circuit as shown in Figure 5-4. The amplitude must be greater than 300 mV peak to peak. The component values provided in Figure 5-4 are for example only. The actual values should be selected to satisfy system requirements.

The **REFCLK** amplitude must comply with the signal amplitudes shown in Table 4-4 and the duty cycle in Table 4-2.

FIGURE 5-4: EXAMPLE OF CIRCUIT USED TO SHIFT A REFERENCE CLOCK COMMON-MODE VOLTAGE LEVEL



5.4.3 REFCLK JITTER

The USB83340 is tolerant to jitter on the reference clock. The **REFCLK** jitter should be limited to a peak to peak jitter of less than 1 ns over a 10 µs time interval. If this level of jitter is exceeded when configured for either ULPI Clock In Mode or ULPI Clock Out Mode, the USB83340 high-speed eye diagram may be degraded.

The frequency accuracy of the REFCLK must meet the +/- 500 ppm requirement as shown in Table 4-2.

5.4.4 REFCLK ENABLE/DISABLE

The **REFCLK** should be enabled when the **RESETB** pin is brought high. The ULPI interface will start running after the time specified in Table 4-2. If the reference clock-enable is delayed relative to the **RESETB** pin, the ULPI interface will start operation delayed by the same amount. The reference clock can be run at anytime the **RESETB** pin is low without causing the USB83340 to start-up or draw current.

When the USB83340 is placed in Low Power Mode or Carkit Mode, the reference clock can be stopped after the final ULPI register write is complete. The **STP** pin is asserted to bring the USB83340 out of Low Power Mode. The reference clock should be started at the same time **STP** is asserted to minimize the USB83340 start-up time.

If the reference clock is stopped while in ULPI Synchronous Mode the PLL will come out of lock and the frequency of oscillation will decrease to the minimum allowed by the PLL design. If the reference clock is stopped during a USB session, the session may drop.

5.5 Internal Regulators and POR

The USB83340 includes integrated power management functions, including a low-dropout regulator that can be used to generate the 3.3 V USB supply, an integrated 1.8 V regulator, and a POR generator described in Section 5.5.2.

5.5.1 INTEGRATED LOW-DROPOUT REGULATORS

The USB83340 includes two integrated linear regulators. Power sourced at the **VBAT** pin is regulated to 3.3 V and 1.8 V output on the **VDD33** and **VDD18** pins. To ensure stability, both regulators require an external bypass capacitor as specified in Table 4-7 placed as close to the pin as possible.

The USB83340 regulators are designed to generate the 3.3 V and 1.8 V supplies for the USB83340 only. Using the regulators to provide current for other circuits is not recommended and Microchip does not guarantee USB performance or regulator stability.

During USB UART Mode the 3.3 V regulator output voltage can be changed to allow the USB83340 to work with UARTs operating at different operating voltages. The 3.3 V regulator output is configured to the voltages shown in Table 4-7 with the *UART RegOutput[1:0]* bits in the USB IO & Power Management register.

The regulators are enabled by the **RESETB** pin. When **RESETB** pin is low both regulators are disabled and the regulator outputs are pulled low by weak pull-down. The **RESETB** pin must be brought high to enable the regulators.

For peripheral-only or host-only bus-powered applications, the input to **VBAT** may be derived from the VBUS pin of the USB connector. In this configuration, the supply must be capable of withstanding any transient voltage present at the VBUS pin of the USB connector. Microchip does not recommend connecting the **VBAT** pin to the VBUS terminal of the USB connector.

5.5.2 POWER ON RESET (POR)

The USB83340 provides a POR circuit that generates an internal reset pulse after the **VDD18** supply is stable. After the internal POR goes high the USB83340 will release from reset and begin normal ULPI operation as described in Section 5.5.4.

The ULPI registers will power up in their default state summarized in Table 7-1 when the 1.8 V supply comes up. Cycling the **RESETB** pin can also be used to reset the ULPI registers to their default state (and reset all internal state machines) by bringing the pin low for a minimum of 1 ms and then high. It is not necessary to wait for the **VDD33** and **VDD18** pins to discharge to 0 V to reset the part.

The **RESETB** pin must be pulled high to enable the 3.3 V and 1.8 V regulators. A pull-down resistor is not present on the **RESETB** pin and therefore the system should drive the **RESETB** pin to the desired state at all times. If the system does not need to place the USB83340 into reset mode the **RESETB** pin can be connected to a supply between 1.8 V and 3.3 V.

5.5.3 RECOMMENDED POWER SUPPLY SEQUENCE

For USB operation, the USB83340 requires a valid voltage on the **VBAT** and **VDDIO** pins. The **VDD33** and **VDD18** regulators are automatically enabled when the **RESETB** pin is brought high. Table 5-3 presents the power supply configurations in more detail.

The **RESETB** pin can be held low until the **VBAT** supply is stable. If the Link is not ready to interface the USB83340, the Link may choose to hold the **RESETB** pin low until it is ready to control the ULPI interface.

Power supplies must ramp from 10 % to 90 % of their final value in less than 400 ms.

TABLE 5-3: OPERATING MODE VS. POWER SUPPLY CONFIGURATION

VBAT	VDDIO	RESETB	Operating Modes Available
0	0	0	Powered Off
1	X	0	RESET Mode (Note 3)
1	1	1	Full USB operation as described in Chapter 6.0.

3: VDDIO must be present for ULPI pins to tri-state.

5.5.4 START-UP

The power on default state of the USB83340 is ULPI Synchronous Mode. The USB83340 requires the following conditions to begin operation:

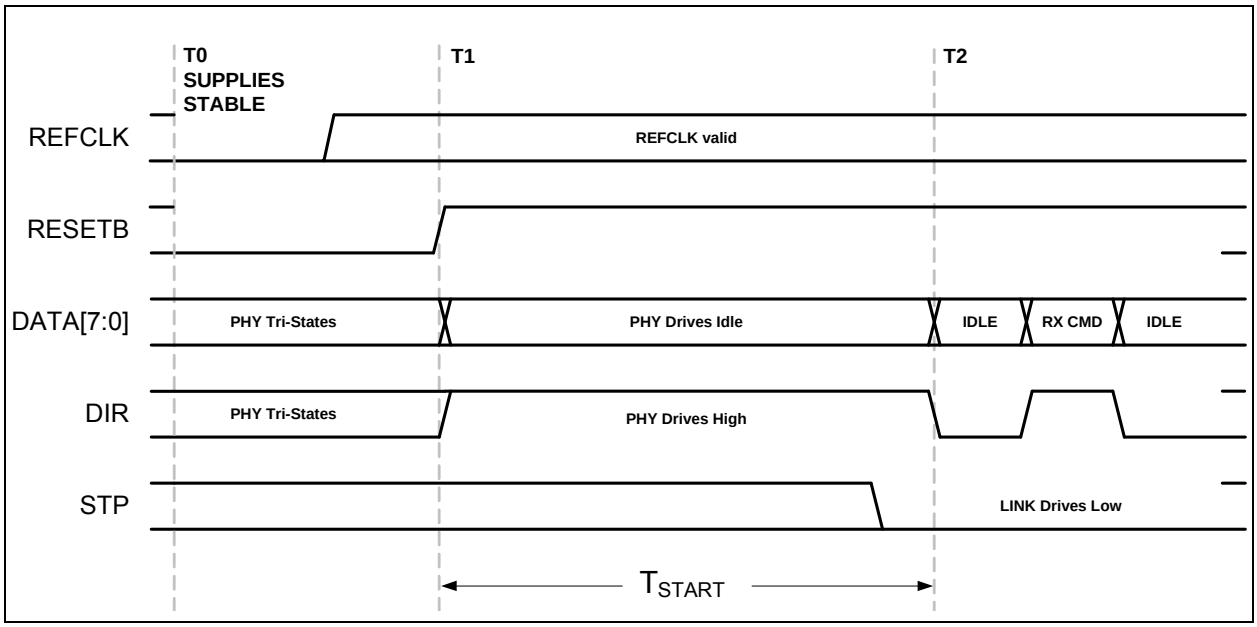
- The power supplies must be stable.
- The **REFCLK** must be present.
- The **RESETB** pin must be high.

After these conditions are met, the USB83340 will begin ULPI operation that is described in Chapter 6.0.

Figure 5-5 below shows a timing diagram to illustrate the start-up of the USB83340. At T0, the supplies are stable and the USB83340 is held in reset mode. At T1, the Link drives **RESETB** high after the **REFCLK** has started. The **RESETB** pin may be brought high asynchronously to **REFCLK**. Once, the 3.3 V and 1.8 V internal supplies become stable the USB83340 will apply the 15 kΩ pull downs to the data bus and assert **DIR** until the internal PLL has locked. After the PLL has locked, the USB83340 will check that the Link has de-asserted **STP** and at T2 it will de-assert **DIR** and begin ULPI operation.

The ULPI bus will be available as shown in Figure 5-5 in the time defined as T_{START} given in Table 4-2. If the **REFCLK** signal starts after the **RESETB** pin is brought high, then time T0 will begin when **REFCLK** starts. T_{START} also assumes that the Link has de-asserted **STP**. If the Link has held **STP** high the USB83340 will hold **DIR** high until **STP** is de-asserted. When the Link de-asserts **STP**, it must be ready drive the ULPI data bus to idle (00h) for a minimum of one clock cycle after **DIR** de-asserts.

FIGURE 5-5: ULPI START-UP TIMING



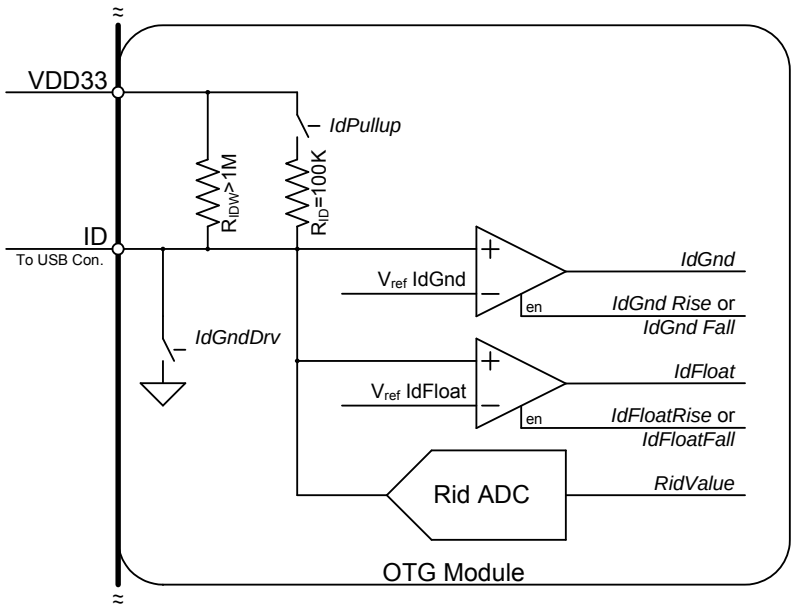
5.6 USB On-The-Go (OTG)

The USB83340 provides support for the USB OTG protocol. OTG allows the USB83340 to be dynamically configured as a host or peripheral depending on the type of cable inserted into the Micro-AB receptacle. When the Micro-A plug of a cable is inserted into the Micro-AB receptacle, the USB device becomes the A-device. When a Micro-B plug is inserted, the device becomes the B-device. The OTG A-device behaves similar to a host while the B-device behaves similar to a peripheral. The differences are covered in the “On-The-Go Supplement to the USB 2.0 Specification”. In applications where only USB host or USB peripheral is required, the OTG module is unused.

5.6.1 ID RESISTOR DETECTION

The ID pin of the USB connector is monitored by the **ID** pin of the USB83340 to detect the attachment of different types of USB devices and cables. For device only applications that do not use the ID signal the **ID** pin should be connected to **VDD33**. The block diagram of the ID detection circuitry is shown in Figure 5-6 and the related parameters are given in Table 4-5.

FIGURE 5-6: USB83340 ID RESISTOR DETECTION CIRCUITRY



5.6.1.1 USB OTG Operation

The USB83340 can detect **ID** grounded and **ID** floating to determine if an A or B cable has been inserted. The A plug will ground the **ID** pin while the B plug will float the **ID** pin. These are the only two valid states allowed in the OTG Protocol.

To monitor the status of the **ID** pin, the Link activates the *IdPullup* bit in the OTG Control register, waits 50 ms and then reads the status of the *IdGnd* bit in the USB Interrupt Status register. If an A cable has been inserted the *IdGnd* bit will read 0. If a B cable is inserted, the **ID** pin is floating and the *IdGnd* bit will read 1.

The USB83340 provides an integrated weak pull-up resistor on the **ID** pin, R_{IDW}. This resistor is present to keep the **ID** pin in a known state when the *IdPullup* bit is disabled and the **ID** pin is floated. In addition to keeping the **ID** pin in a known state, it enables the USB83340 to generate an interrupt to inform the link when a cable with a resistor to ground has been attached to the **ID** pin. The weak pull-up is small enough that the largest valid R_{ID} resistor pulls the **ID** pin low and causes the IdGnd comparator to go low.

After the Link has detected an **ID** pin state change, the R_{ID} converter can be used to determine the resistor value as described in Section 5.6.1.2.

5.6.1.2 Measuring ID Resistance to Ground

The Link can use the integrated resistance measurement capabilities of the USB83340 to determine the value of an ID resistance to ground. The following table details the valid values of resistance to ground that the USB83340 can detect.

TABLE 5-4: VALID VALUES OF ID RESISTANCE TO GROUND

ID Resistance to Ground	R_{ID} Value
Ground	000
75 Ω +/-1%	001
102 kΩ +/-1%	010
200 kΩ+/-1%	011
440 kΩ +/-1%	100
Floating	101

Note: IdPullUp = 0

The ID resistance to ground can be read while the USB83340 is in Synchronous Mode. When a resistor to ground is attached to the **ID** pin, the state of the IdGnd comparator will change. After the Link has detected **ID** transition to ground, it can use the methods described in Section 6.8 to operate the R_{ID} converter.

5.6.1.3 Using IdFloat Comparator (Not Recommended)

Note:	The ULPI specification details a method to detect a 102 kΩ resistance to ground using the IdFloat comparator. This method can only detect 0 Ω, 102 kΩ, and floating terminations of the **ID** pin. Due to this limitation it is recommended to use the R_{ID} converter as described in Section 5.6.1.2.

The **ID** pin can be either grounded, floated, or connected to ground with a 102 kΩ external resistor. To detect the 102 kΩ resistor, set the *idPullup* bit in the OTG Control register, causing the USB83340 to apply the 100 kΩ internal pull-up connected between the **ID** pin and VDD33. Set the *idFloatRise* and *idFloatFall* bits in the Carkit Interrupt Enable register to enable the IdFloat comparator to generate an RX CMD to the Link when the state of the IdFloat changes. As described in Figure 6-3, the alt_int bit of the RX CMD will be set. The values of IdGnd and IdFloat are shown for the three types cables that can attach to the USB Connector in Table 5-5.

TABLE 5-5: IdGnd AND IdFloat VS. ID RESISTANCE TO GROUND

ID Resistance	IdGnd	IdFloat
Float	1	1
102 kΩ	1	0
GND	0	0

Note:	The ULPI register bits *IdPullUp*, *IdFloatRise,* and *IdFloatFall* should be enabled.

To save current when an A plug is inserted, the internal 102 kΩ pull-up resistor can be disabled by clearing the *IdPullUp* bit in the OTG Control register and the *IdFloatRise* and *IdFloatFall* bits in both the USB Interrupt Enable Rising and USB Interrupt Enable Falling registers. If the cable is removed the weak R_{IDW} will pull the **ID** pin high.

The *IdGnd* value can be read using the ULPI USB Interrupt Status register, bit 4. In host mode, it can be set to generate an interrupt when *IdGnd* changes by setting the appropriate bits in the USB Interrupt Enable Rising and USB Interrupt Enable Falling registers. The *IdFloat* value can be read by reading the ULPI Carkit Interrupt Status register, bit 0.

Note:	The IdGnd switch has been provided to ground the **ID** pin for future applications.

5.6.2 VBUS MONITORING AND VBUS PULSING

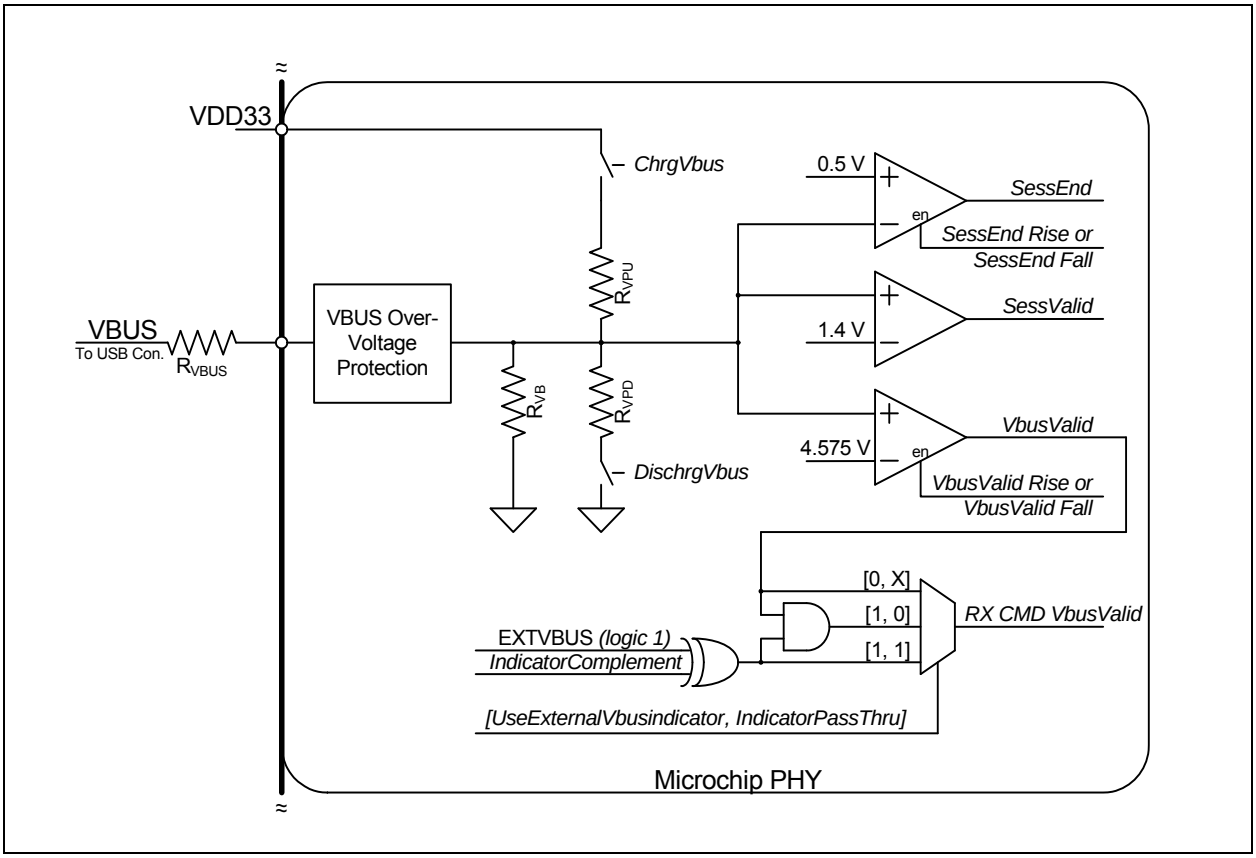
The USB83340 includes all of the VBUS comparators required for OTG. The VbusVld, SessVld, and SessEnd comparators shown in Figure 5-7 are fully integrated into the USB83340. These comparators are used to monitor changes in the VBUS voltage, and the state of each comparator can be read from the USB Interrupt Status register.

The VbusVld comparator is used by the Link, when configured as an A-device, to ensure that the VBUS voltage on the cable is valid. The SessVld comparator is used by the Link when configured as both an A- or B-device to indicate a session is requested or valid. Finally the SessEnd comparator is used by the B-device to indicate a USB session has ended.

Also included in the VBUS Monitor and Pulsing block are the resistors used for VBUS pulsing in SRP. The resistors used for VBUS pulsing include a pull-down to ground and a pull-up to **VDD33**.

In some applications, voltages much greater than 5.5 V may be present at the VBUS pin of the USB connector. The USB83340 includes an over-voltage protection circuit that protects the **VBUS** pin of the USB83340 from excessive voltages as shown in Figure 5-7.

FIGURE 5-7: USB83340 OTG VBUS BLOCK



5.6.2.1 SessEnd Comparator

The SessEnd comparator is used during the Session Request Protocol (SRP). The comparator is used by the B-device to detect when a USB session has ended and it is safe to start VBUS Pulsing to request a USB session from the A-device. When VBUS goes below the threshold specified in the USB 2.0 specification, the USB session is considered to be ended, and SessEnd will transition from 0 to 1. The SessEnd comparator can be disabled by clearing this bit in both the USB Interrupt Enable Rising and USB Interrupt Enable Falling registers. When disabled, the SessEnd bit in the USB Interrupt Status register will read 0.

The SessEnd comparator is only used when configured as an OTG device. If the USB83340 is used as a host or device only the SessEnd Comparator should be disabled, using the method described above.

5.6.2.2 SessVld Comparator

The SessVld comparator is used when the PHY is configured as both an A- and B-device. When configured as an A-device, the SessVld is used to detect Session Request Protocol (SRP). When configured as a B-device, SessVld is used to detect the presence of VBUS. The SessVld comparator output can also be read from the USB Interrupt Status register. The SessVld comparator will also generate an RX CMD, as detailed in Section 6.3.1, anytime the comparator changes state. The SessVld interrupts can be disabled by clearing this bit in both the USB Interrupt Enable Rising and USB Interrupt Enable Falling registers. When the interrupts are disabled, the SessVld comparator is still operational and will generate RX CMDs. The SessVld comparator trip point is detailed in Table 4-5.

Note:	The OTG Supplement specifies a voltage range for A-Device Session Valid and B-Device Session Valid comparator. The USB83340 PHY combines the two comparators into one and uses the narrower threshold range.

5.6.2.3 VbusVld Comparator

The VbusVld comparator is only used when the USB83340 is configured as a host that can supply less than 100 mA VBUS current. In the USB protocol, the A-device supplies the VBUS voltage and is responsible to ensure it remains within a specified voltage range. The VbusVld comparator can be disabled by clearing this bit in both the USB Interrupt Enable Rising and USB Interrupt Enable Falling registers. When disabled, bit 1 of the USB Interrupt Status register will return a 0. The VbusVld comparator threshold values are detailed in Table 4-5.

If the USB83340 is used as a device only the VbusValid comparator should be disabled, using the method described above.

The USB83340 includes the external VbusVld indicator logic as detailed in the ULPI specification. The external VbusVld indicator is tied to a logic one. The decoding of this logic is shown in Table 5-6 below. By default this logic is disabled.

TABLE 5-6: EXTERNAL VBUS INDICATOR LOGIC

Typical Application	Use External VBus Indicator	Indicator Pass Thru	Indicator Complement	RX CMD VBus Valid Encoding Source
OTG Device	0	X	X	Internal VbusVld comparator (Default)
	1	1	0	Fixed 1
	1	1	1	Fixed 0
	1	0	0	Internal VbusVld comparator.
	1	0	1	Fixed 0
Standard Host	1	1	0	Fixed 1
	1	1	1	Fixed 0
Standard Peripheral	0	X	X	Internal VbusVld comparator. This information should not be used by the Link (Note 4).

4: A peripheral should not use VbusVld to begin operation. The peripheral should use SessVld to detect the presence of VBUS on the USB connector. VbusVld should only be used for USB host and OTG A-device applications.

5.6.2.4 VBUS Pulsing with Pull-up and Pull-down Resistors

In addition to the internal VBUS comparators, the USB83340 also includes the integrated VBUS pull-up and pull-down resistors used for VBUS Pulsing during OTG Session Request Protocol. To discharge the VBUS voltage so that a Session Request can begin, the USB83340 provides a pull-down resistor from **VBUS** to **GND**. This resistor is controlled by the *DischargeVbus* bit 3 of the OTG Control register. The pull-up resistor is connected between VBUS and VDD33. This resistor is used to pull VBUS above 2.1 V so that the A-device knows that a USB session has been requested. The state of the pull-up resistor is controlled by the bit 4 *ChargeVbus* of the OTG Control register. The Pull-Up and pull-down resistor values are detailed in Table 4-5.

The internal VBUS pull-up and pull-down resistors are designed to include the R_{VBUS} external resistor in series. This external resistor is used by the VBUS over-voltage protection described below.

5.6.2.5 VBUS Input Impedance

The OTG Supplement requires an A-device that supports Session Request Protocol to have a VBUS input impedance less than 100 kΩ and greater than 40 kΩ to ground. The USB83340 provides a 75 kΩ resistance to ground, R_{VB}. The R_{VB} resistor tolerance is detailed in Table 4-5.

5.6.2.6 VBUS Over-Voltage Protection (OVP)

The USB83340 provides an integrated over-voltage protection circuit to protect the **VBUS** pin from excessive voltages that may be present at the USB connector. The over-voltage protection circuit works with an external resistor (R_{VBUS}) by drawing current across the resistor to reduce the voltage at the **VBUS** pin.

When voltage at the **VBUS** pin exceeds 5.5 V, the over-voltage protection block will sink current to ground until VBUS is below 5.5 V. The current drops the excess voltage across R_{VBUS} and protects the USB83340 **VBUS** pin. The required R_{VBUS} value is dependent on the operating mode of the USB83340 as shown in Table 5-7.

TABLE 5-7: REQUIRED R_{VBUS} RESISTOR VALUE

Operating Mode	R_{VBUS}
Device only	20 kΩ ±5%
OTG host capable of less than 100 mA of current on VBUS	1 kΩ ±5%
Host or OTG Host capable of > 100 mA UseExternalVbusIndicator = 1	20 kΩ ±5%

The over-voltage protection circuit is designed to protect the USB83340 from continuous voltages up to 30 V on the R_{VBUS} resistor.

The R_{VBUS} resistor must be sized to handle the power dissipated across the resistor. The resistor power can be found using the equation below:

$$P_{RVBUS} = \frac{(Vprotect - 5{,}0)^2}{R_{VBUS}}$$

Where:

- Vprotect is the VBUS protection required.
- R_{VBUS} is the resistor value, 1 kΩ or 20 kΩ.
- P_{RVBUS} is the required power rating of R_{VBUS}.

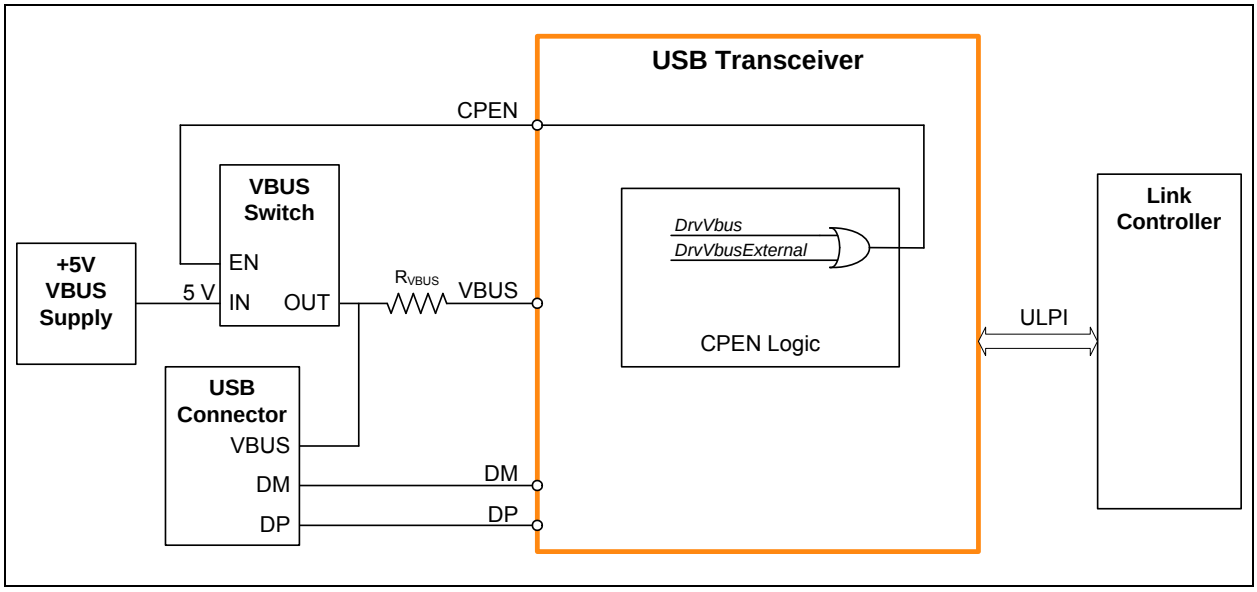
For example, protecting a peripheral or device only application to 15 V would require a 20 kΩ R_{VBUS} resistor with a power rating of 0.01 W. To protect an OTG product to 15 V would require a 1 kΩ R_{VBUS} resistor with a power rating of 0.1 W.

5.6.3 DRIVING EXTERNAL VBUS

The USB83340 monitors VBUS as described in VBUS Monitoring and VBUS Pulsing. For OTG and host applications, the system is required to source 5 V on VBUS. The USB83340 fully supports VBUS power control using an external VBUS switch as shown in Figure 8-3. The USB83340 provides an active high control signal, **CPEN**, that is dedicated to controlling the Vbus supply when configured as an A-device.

CPEN is asserted by setting the *DrvVbus* or *DrvVbusExternal* bit of the OTG Control register. To be compatible with Link designs that support both internal and external Vbus supplies the *DrvVbus* and *DrvVbusExternal* bits in the OTG Control register are OR'd together. This enables the Link to set either bit to access the external Vbus enable (**CPEN**). This logic is shown in Figure 5-8. *DrvVbus* and *DrvVbusExternal* are set to 0 on Power On Reset (POR) as shown in Section 7.1.1.7.

FIGURE 5-8: USB83340 DRIVES CONTROL SIGNAL (CPEN) TO EXTERNAL VBUS SWITCH



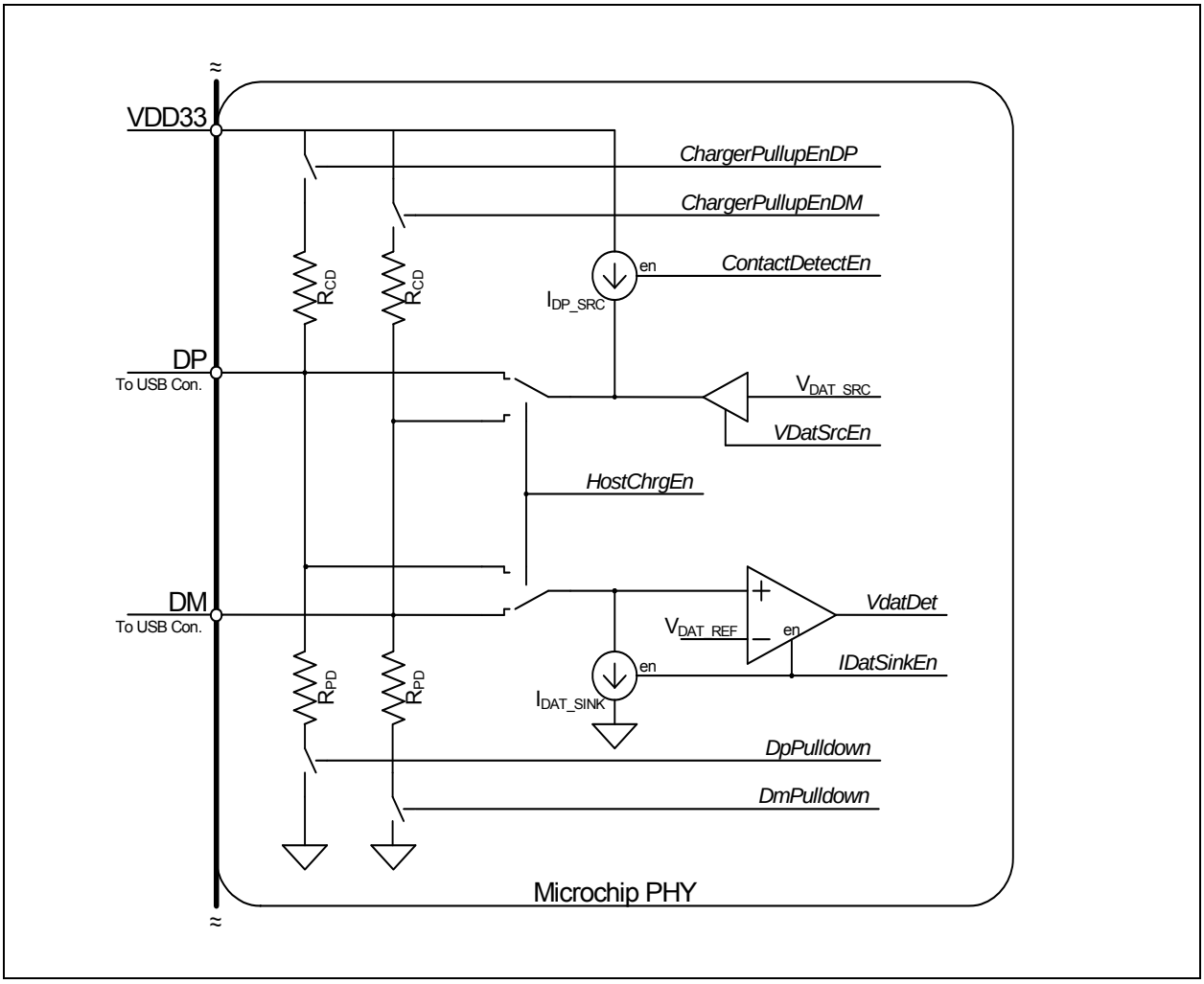
5.7 USB UART Support

The USB83340 provides support for the USB UART interface as detailed in the ULPI specification and the former CEA-936A specification. The USB83340 can be placed in UART Mode using the method described in Section 6.7, and the regulator output will automatically switch to the value configured by the *UART RegOutput bits in the* USB IO & Power Management register. While in UART Mode, the Linestate signals cannot be monitored on the DATA[0] and DATA[1] pins.

5.8 USB Charger Detection Support

The following blocks allow the USB83340 to detect when a battery charger, charging host port, or a USB host is attached to the USB connector. The USB83340 can also be configured to appear as a charging host port. The charger detection circuitry should be disabled during USB operation.

FIGURE 5-9: USB CHARGER DETECTION BLOCK DIAGRAM



Note: The *italic names* in the Figure 5-9 correspond to bits in the ULPI register set.

The charger detection circuitry runs from the **VDD33** supply and requires that the **VDD33** supply to be present to run the charger detection circuitry. The **VDD33** supply is present anytime the **RESETB** pin is pulled high and **VBAT** is present. The charger detection circuits are fully functional while in Low Power Mode (*Suspendm* = 0). The status of the *VdatDet* can be relayed back to the Link through the ULPI interrupts in both Synchronous Mode and Low Power Mode.

5.8.1 ACTIVE ANALOG CHARGER DETECTION

The USB83340 includes the active analog charger detection specified in the USB-IF Battery Charging Specification. The additional analog circuitry will allow the USB83340 to:

1. Detect a USB charger that has shorted DP and DM together
2. Detect a USB host/charger
3. Behave as a USB host/charger

The charger detection circuitry is shown in Figure 5-9.

The *VdatDet* output is qualified with the Linestate[1:0] value. If the Linestate is not equal to 00 the *VdatDet* signal will not assert.

TABLE 5-8: USB CHARGER SETTING VS. MODES

Charger Detection Modes	*VDatSrcEn*	*IDatSinkEn*	*ContactDetEn*	*HostChrgEn*	*DpPulldown*	*DmPulldown*
Device Connect Detect (The Connect Detect setting in Table 5-1 must be followed)	0	0	1	0	0	1
Device Charger Detection	1	1	0	0	0	0
Device USB Operation	0	0	0	0	0	0
Charging Host Port, no charging device attached and SE0 (*VdatDet* = 0)	0	1	0	1	1	1
Charging Host Port, charging device attached (*VdatDe*t = 1)	1	1	0	1	1	1
Charging Host Port USB Operation	0	0	0	1	1	1

5.8.2 RESISTIVE CHARGER DETECTION

Note: The Resistive Charger Detection has been superseded by the Active Analog Charger Detection detailed above. It is recommended that new designs use the Active Analog Charger Detection.

To support the detection and identification of different types of USB chargers the USB83340 provides integrated pull-up resistors, R_{CD}, on both **DP** and **DM**. These pull-up resistors along with the single-ended receivers can be used to determine the type of USB charger attached. Reference information on implementing charger detection is provided in Section 8.2.

TABLE 5-9: USB WEAK PULL-UP ENABLE

RESETB	DP Pullup Enable	DM Pullup Enable
0	0	0
1	*ChargerPullupEnableDP*	*ChargerPullupEnableDM*

Note: *ChargerPullupEnableDP* and *ChargerPullupEnableDM* are enabled in the USB IO & Power Management register.

5.9 USB Audio Support

Note: The USB83340 supports “USB Digital Audio” through the USB protocol in ULPI and USB Serial modes described in Chapter 6.0.

The USB83340 provides two low resistance analog switches that allow analog audio to be multiplexed over the DP and DM terminals of the USB connector. The audio switches are shown in Figure 5-1. The electrical characteristics of the USB audio switches are provided in the USB Battery Charging Specification, Revision 1.2.

During normal USB operation the switches are off. When USB audio is desired the switches can be turned “on” by enabling the *SpkLeftEn, SpkRightEn,* or *MicEn* bits in the Carkit Control register as described in Section 6.7.2. These bits are disabled by default.

The **RESETB** pin must be high when using the analog switches so that the **VDD33** supply is present. If the **VDD33** supply is applied externally and **RESETB** is held low the switches will be off.

In addition to USB audio support the switches could also be used to multiplex a second full-speed USB PHY to the USB connector. The signal quality will be degraded slightly due to the “on” resistance of the switches. The USB83340 single-ended receivers described in Section 5.2.1 are enabled while in Synchronous Mode and are disabled when Carkit Mode is entered.

The USB83340 does not provide the DC bias for the audio signals. The **SPK_R** and **SPK_L** pins should be biased to 1.65 V when audio signals are routed through the USB83340. This DC bias is necessary to prevent the audio signal from swinging below ground and being clipped by ESD Diodes.

When the system is not using the USB audio switches, the **SPK_R** and **SPK_L** switches should be disabled.

6.0 ULPI OPERATION

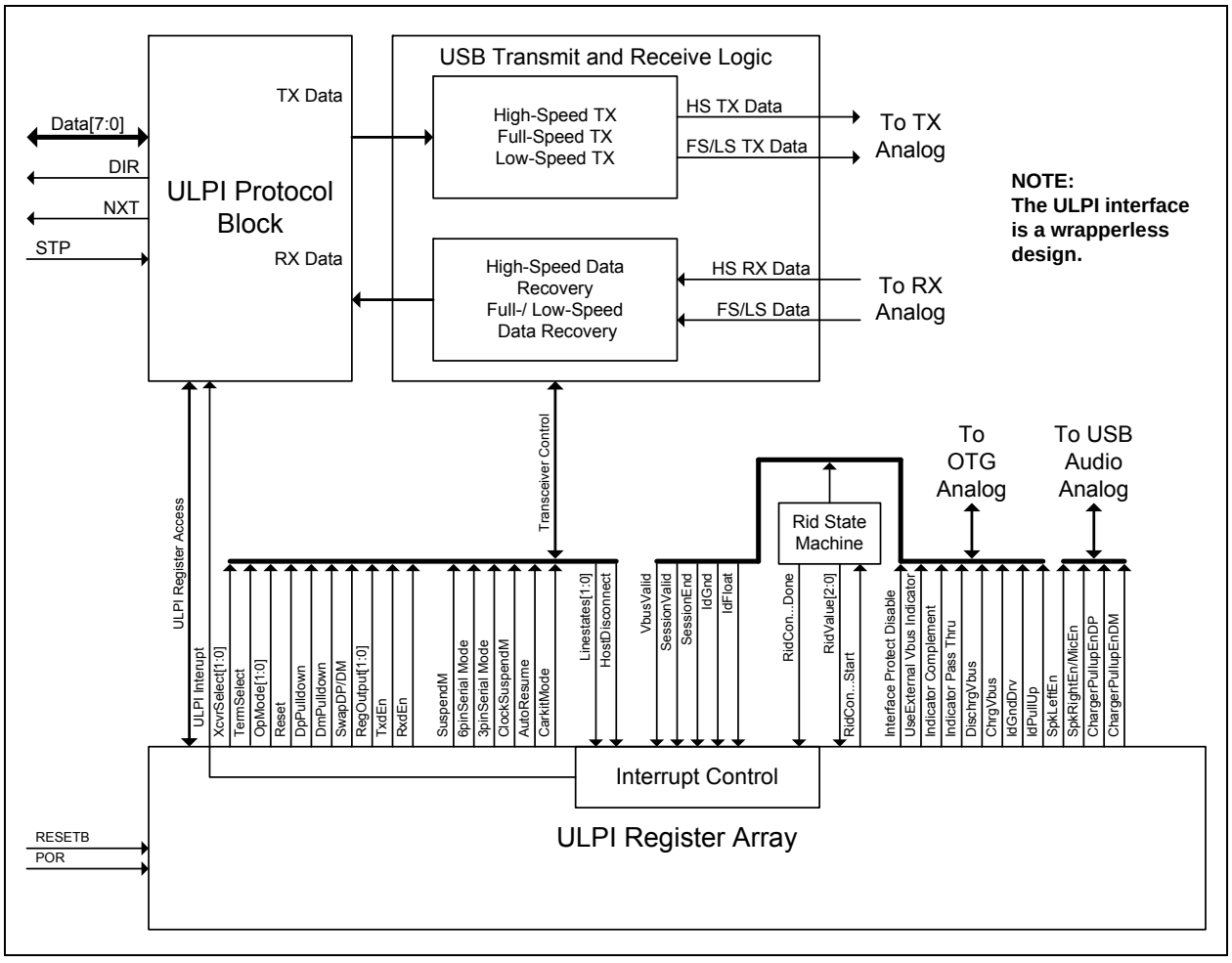
6.1 ULPI Introduction

The USB83340 uses the industry standard ULPI digital interface for communication between the transceiver and Link (device controller). The ULPI interface is designed to reduce the number of pins required to connect a discrete USB transceiver to an ASIC or digital controller. For example, a full UTMI+ Level 3 OTG interface requires 54 signals while a ULPI interface requires only 12 signals.

The ULPI interface is documented completely in the “UTMI+ Low Pin Interface (ULPI) Specification, Revision 1.1”. The following sections describe the operating modes of the USB83340 digital interface.

Figure 6-1 illustrates the block diagram of the ULPI digital functions. It should be noted that this USB83340 does not use a “ULPI wrapper” around a UTMI+ PHY core as the ULPI specification implies.

FIGURE 6-1: ULPI DIGITAL BLOCK DIAGRAM



The advantage of a “wrapper-less” architecture is that the USB83340 has a lower USB latency than a design, which must first register signals into the PHY’s wrapper before the transfer to the transceiver core. A low latency PHY allows a wrapper around a UTMI Link to be used and still make the required USB turn-around timing required by the USB 2.0 specification.

RxEndDelay maximum allowed by the UTMI+/ULPI for 8-bit data is 63 high-speed clocks. USB83340 uses a low latency high-speed receiver path to lower the RxEndDelay to 43 high-speed clocks. This low latency design gives the Link more cycles to make decisions and reduces the Link complexity. This is the result of the “wrapper less” architecture of the USB83340. This low RxEndDelay should allow legacy UTMI Links to use a “wrapper” to convert the UTMI+ interface to a ULPI interface.

In Figure 6-1, a single ULPI Protocol Block decodes the ULPI 8-bit bi-directional bus when the Link addresses the PHY. The Link must use the **DIR** output to determine direction of the ULPI data bus. The USB83340 is the “bus arbitrator”. The ULPI Protocol Block will route data/commands to the transmitter or the ULPI register array.

6.1.1 ULPI INTERFACE SIGNALS

The UTMI+ Low Pin Interface (ULPI) uses a 12-pin interface to connect a USB transceiver to an external Link. The reduction of external pins, relative to UTMI+, is accomplished implementing the relatively static configuration pins (i.e., xcvrselect[1:0], termselect, opmode[1:0], and DpPullDown DmPulldown) as an internal register array.

An 8-bit bi-directional data bus clocked at 60 MHz allows the Link to access this internal register array and transfer USB packets to and from the PHY. The remaining 3 pins function to control the data flow and arbitrate the data bus.

Direction of the 8-bit data bus is controlled by the **DIR** output from the PHY. Another output, **NXT**, is used to control data flow into and out of the device. Finally, **STP**, which is in input to the PHY, terminates transfers and is used to start up and resume from Low Power Mode.

The ULPI interface signals are described below in Table 6-1.

TABLE 6-1: ULPI INTERFACE SIGNALS

Signal	Direction	Description
CLK	I/O	60 MHz ULPI clock. All ULPI signals are driven synchronously to the rising edge of this clock. This clock can be either driven by the PHY or the Link as described in Section 5.4.1
DATA[7:0]	I/O	8-bit bi-directional data bus. Bus ownership is determined by DIR. The Link and PHY initiate data transfers by driving a non-zero pattern onto the data bus. ULPI defines interface timing for a single-edge data transfers with respect to rising edge of the ULPI clock.
DIR	OUT	Controls the direction of the data bus. When the PHY has data to transfer to the Link, it drives **DIR** high to take ownership of the bus. When the PHY has no data to transfer it drives **DIR** low and monitors the bus for commands from the Link. The PHY will pull **DIR** high whenever the interface cannot accept data from the Link, such as during PLL start-up.
STP	IN	The Link asserts **STP** for one clock cycle to stop the data stream currently on the bus. If the Link is sending data to the PHY, **STP** indicates the last byte of data that was on the bus in the previous cycle.
NXT	OUT	The PHY asserts **NXT** to throttle the data. When the Link is sending data to the PHY, **NXT** indicates when the current byte has been accepted by the PHY. The Link places the next byte on the data bus in the following clock cycle.

USB83340 implements a Single Data Rate (SDR) ULPI interface with all data transfers happening on the rising edge of the 60 MHz ULPI clock while operating in Synchronous Mode. The direction of the data bus is determined by the state of **DIR**. When **DIR** is high, the PHY is driving **DATA[7:0]**. When **DIR** is low, the Link is driving **DATA[7:0]**.

Each time DIR changes, a “turn-around” cycle occurs where neither the Link nor PHY drive the data bus for one clock cycle. During the “turn-around“ cycle, the state of **DATA[7:0]** is unknown and the PHY will not read the data bus.

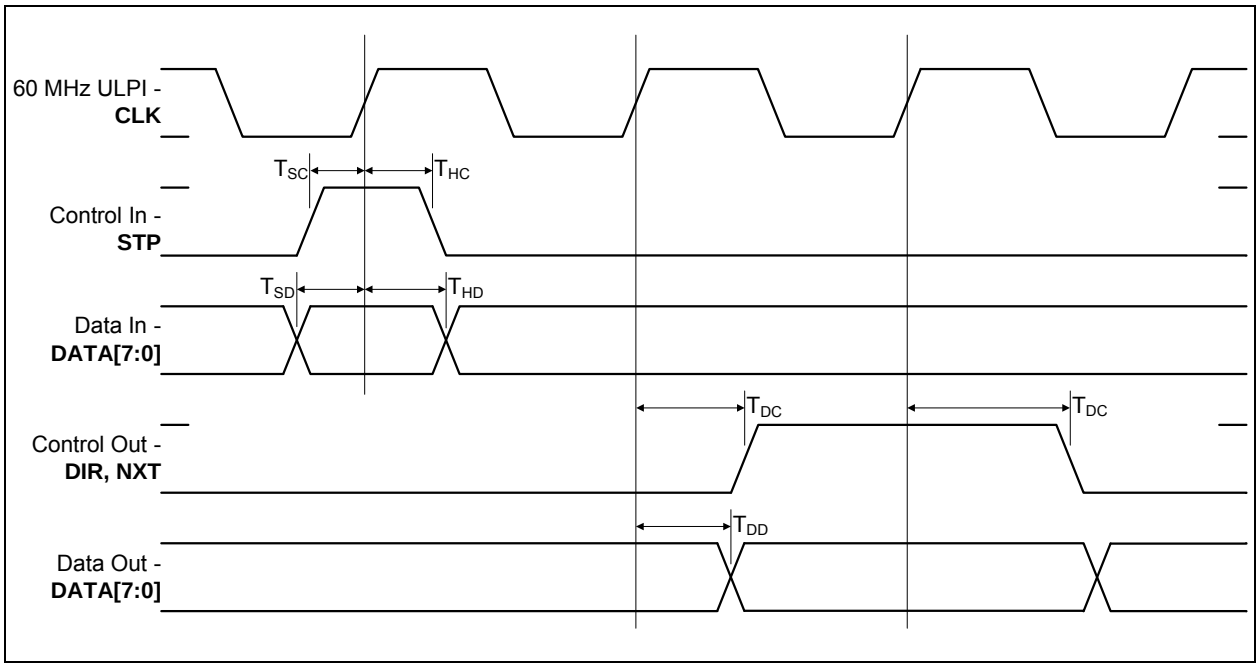
Because USB uses a bit-stuffing encoding, some means of allowing the PHY to throttle the USB transmit data is needed. The ULPI signal **NXT** is used to request the next byte to be placed on the data bus by the Link.

The ULPI interface supports the two basic modes of operation: Synchronous Mode and Asynchronous Mode. Asynchronous Mode includes Low Power Mode, the Serial Modes, and Carkit Mode. In Synchronous Mode, all signals change synchronously with the 60 MHz ULPI clock. In Asynchronous Modes the clock is off and the ULPI bus is redefined to bring out the signals required for that particular mode of operations. The description of Synchronous Mode is described in the following sections while the descriptions of the Asynchronous Modes are described in Section 6.5, Section 6.6, and Section 6.7.

6.1.2 ULPI INTERFACE TIMING IN SYNCHRONOUS MODE

The control and data timing relationships are given in Figure 6-2 and Table 4-3. All timing is relative to the rising clock edge of the 60 MHz ULPI clock.

FIGURE 6-2: ULPI SINGLE DATA RATE TIMING DIAGRAM IN SYNCHRONOUS MODE



6.2 ULPI Register Access

The following section details the steps required to access registers through the ULPI interface. At any time **DIR** is low the Link may access the ULPI registers set using the Transmit Command byte. The ULPI registers retain their contents when the PHY is in Low Power Mode, Full-Speed/Low-Speed Serial Mode, or Carkit Mode.

6.2.1 TRANSMIT COMMAND BYTE (TX CMD)

A command from the Link begins a ULPI transfer from the Link to the USB83340. Before reading a ULPI register, the Link must wait until **DIR** is low, and then send a Transmit Command (TX CMD) byte. The TX CMD byte informs the USB83340 of the type of data being sent. The TX CMD is followed by a data transfer to or from the USB83340. Table 6-2 gives the TX command byte (TX CMD) encoding for the USB83340. The upper two bits of the TX CMD instruct the PHY as to what type of packet the Link is transmitting.

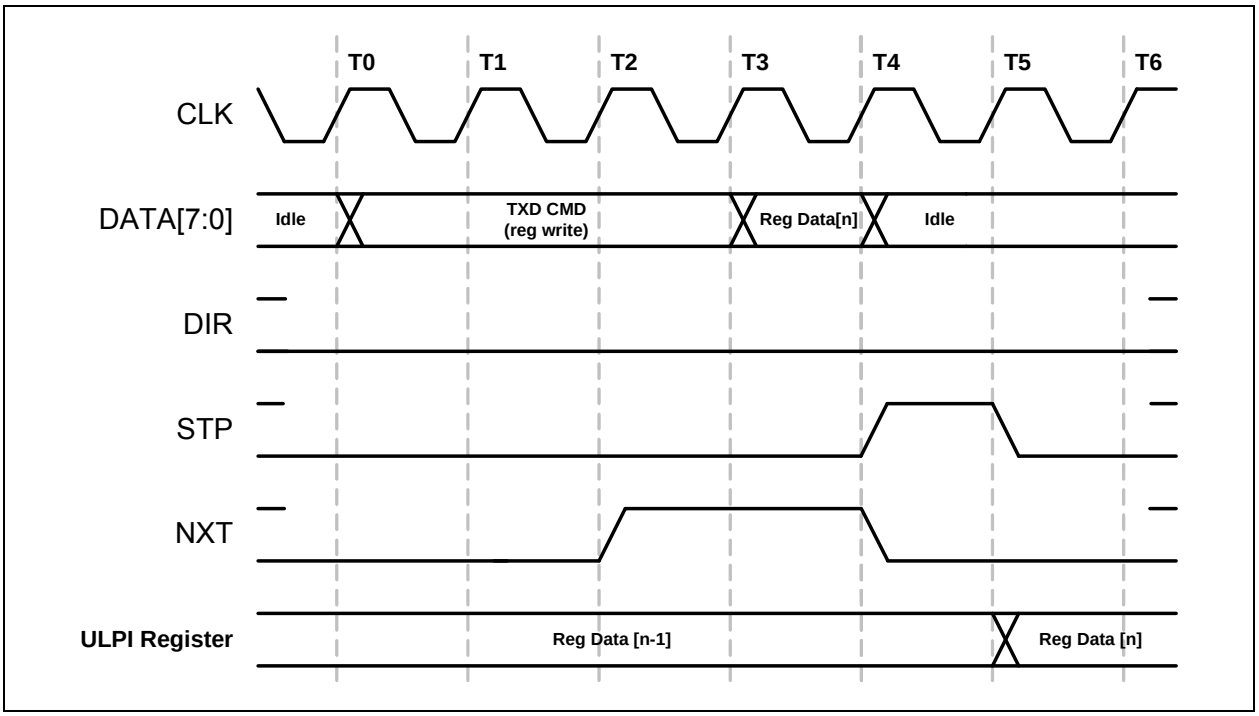
TABLE 6-2: ULPI TX CMD BYTE ENCODING

Command Name	Cmd Bits[7:6]	Cmd Bits[5:0]	Command Description
Idle	00b	000000b	ULPI Idle
Transmit	01b	000000b	USB Transmit Packet with No Packet Identifier (NOPID)
		00XXXXb	USB Transmit Packet Identifier (PID) where DATA[3:0] is equal to the 4-bit PID. $P_3P_2P_1P_0$ where P_3 is the MSB.
Register Write	10b	XXXXXXb	Immediate Register Write Command where: **DATA[5:0]** = 6-bit register address
		101111b	Extended Register Write Command where the 8-bit register address is available on the next cycle.
Register Read	11b	XXXXXXb	Immediate Register Read Command where: **DATA[5:0]** = 6-bit register address
		101111b	Extended Register Read Command where the 8-bit register address is available on the next cycle.

6.2.2 ULPI REGISTER WRITE

A ULPI register write operation is given in Figure 6-3. The TX command with a register write **DATA[7:6]** = 10b is driven by the Link at T0. The register address is encoded into **DATA[5:0]** of the TX CMD byte.

FIGURE 6-3: ULPI REGISTER WRITE IN SYNCHRONOUS MODE

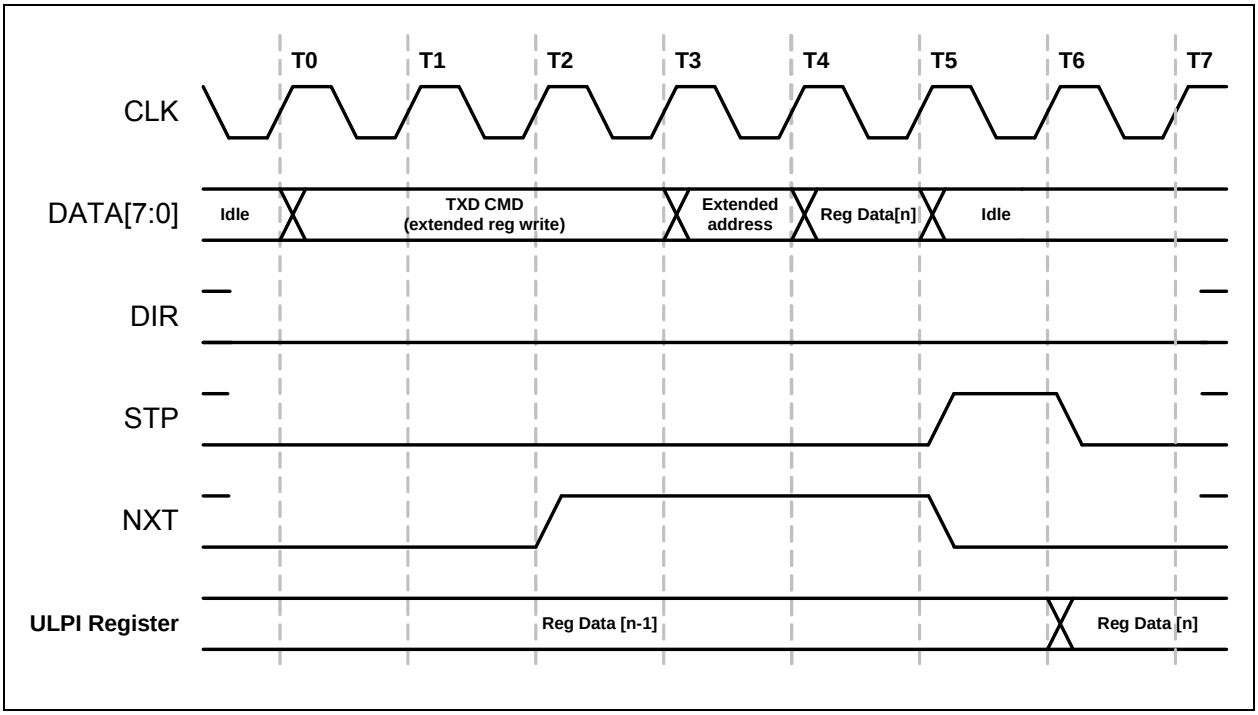


To write a register, the Link will wait until **DIR** is low, and at T0, drive the TX CMD on the data bus. At T2 the PHY will drive **NXT** high. On the next rising clock edge, T3, the Link will write the register data. At T4, the PHY will accept the register data and drive **NXT** low. The Link will drive an Idle on the bus and drive **STP** high to signal the end of the data packet. Finally, at T5, the PHY will latch the data into the register and the Link will pull **STP** low.

NXT is used to throttle when the Link drives the register data on the bus. **DIR** is low throughout this transaction since the PHY is receiving data from the Link. **STP** is used to end the transaction and data is registered after the de-assertion of **STP**. After the write operation completes, the Link must drive a ULPI Idle (00h) on the data bus. If the data bus is not driven to idle the USB83340 may decode the non-zero bus value as an RX Command.

A ULPI extended register write operation is shown in Figure 6-4. To write an extended register, the Link will wait until **DIR** is low, and at T0, drive the TX CMD on the data bus. At T2 the PHY will drive **NXT** high. On the next clock T3 the Link will drive the extended address. On the next rising clock edge, T4, the Link will write the register data. At T5, the PHY will accept the register data and drive **NXT** low. The Link will drive an Idle on the bus and drive **STP** high to signal the end of the data packet. At T5, the PHY will latch the data into the register. Finally, at T6, the Link will drive **STP** low.

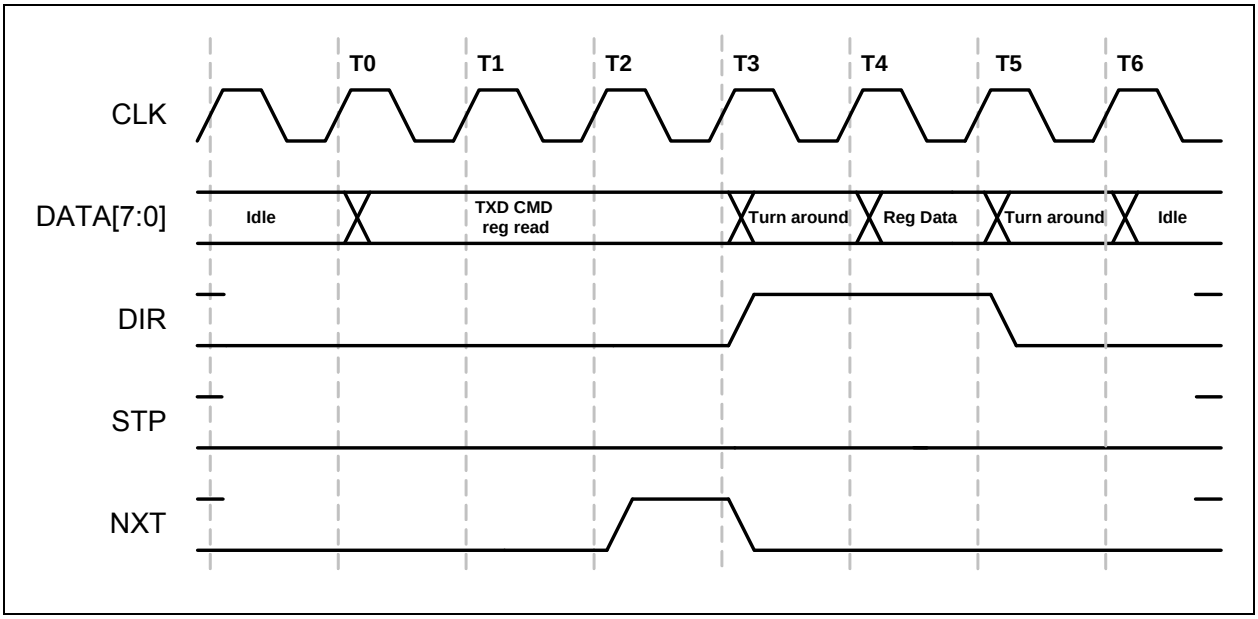
FIGURE 6-4: ULPI EXTENDED REGISTER WRITE IN SYNCHRONOUS MODE



6.2.3 ULPI REGISTER READ

A ULPI register read operation is given in Figure 6-5. The Link drives a TX CMD byte with **DATA[7:6] =** 11h for a register read. **DATA[5:0]** of the ULPI TX command bye contain the register address.

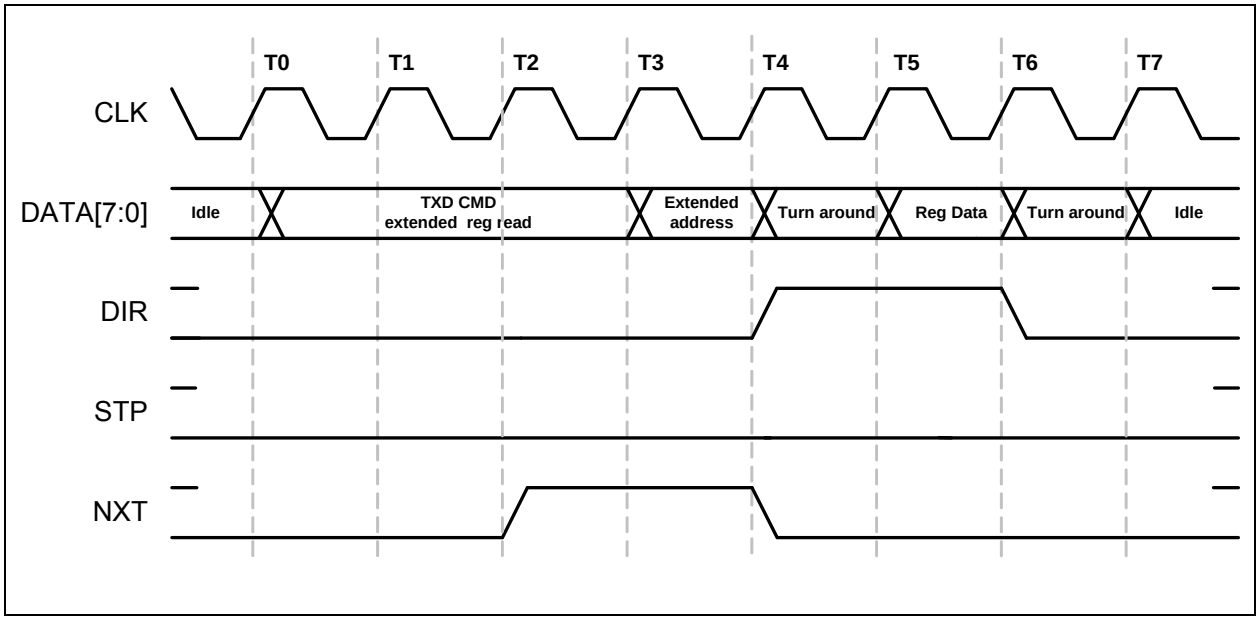
FIGURE 6-5: ULPI REGISTER READ IN SYNCHRONOUS MODE



At T0, the Link will place the TX CMD on the data bus. At T2, the PHY will bring **NXT** high, signaling the Link it is ready to accept the data transfer. At T3, the PHY reads the TX CMD, determines it is a register read, and asserts **DIR** to gain control of the bus. The PHY will also de-assert **NXT**. At T4, the bus ownership has transferred back to the PHY and the PHY drives the requested register onto the data bus. At T5, the Link will read the data bus and the PHY will drop **DIR** low returning control of the bus back to the Link. After the turn around cycle, the Link must drive a ULPI Idle command at T6.

A ULPI extended register read operation is shown in Figure 6-6. To read an extended register, the Link writes the TX CMD with the address set to 2Fh. At T2, the PHY will assert **NXT**, signaling the Link it is ready to accept the extended address. At T3, the Link places the extended register address on the bus. At T4, the PHY reads the extended address, and asserts **DIR** to gain control of the bus. The PHY will also de-assert **NXT**. At T5, the bus ownership has transferred back to the PHY and the PHY drives the requested register onto the data bus. At T6, the Link will read the data bus and the PHY will de-assert **DIR** returning control of the bus back to the Link. After the turn around cycle, the Link must drive a ULPI Idle command at T6.

FIGURE 6-6: ULPI EXTENDED REGISTER READ IN SYNCHRONOUS MODE



6.3 USB83340 Receiver

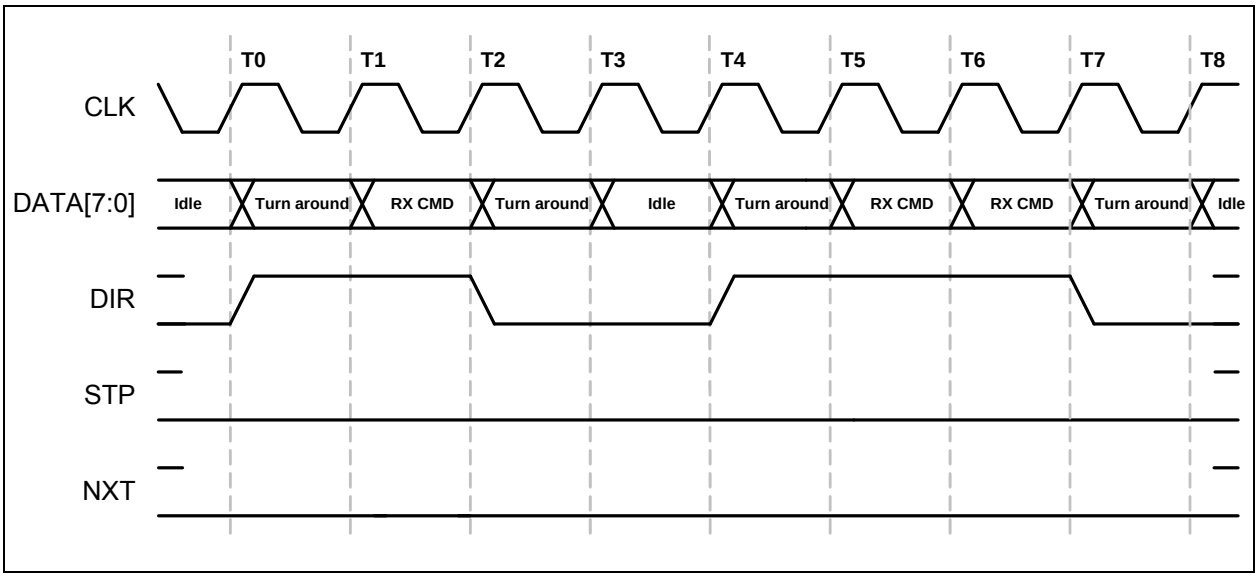
The following section describes how the USB83340 uses the ULPI interface to receive USB signaling and transfer status information to the Link. This information is communicated to the Link using RX Commands to relay bus status and received USB packets.

6.3.1 ULPI RECEIVE COMMAND (RX CMD)

The ULPI Link needs information, which was provided by the following pins in a UTMI implementation: linestate[1:0], rxactive, rxvalid, rxerror, and VbusValid. When implementing the OTG functions, the **VBUS** and **ID** pin states must also be transferred to the Link. ULPI defines a Receive Command (RX CMD) byte that contains this information.

An RX CMD can be sent at any time the bus is idle. The RX CMD is initiated when the USB83340 asserts **DIR** to take control of the bus. The timing of RX CMD is shown in the figure below. The USB83340 can send single or back to back RX CMDs as required. The encoding of the RX CMD byte is given in the Table 6-3.

FIGURE 6-7: ULPI RX CMD TIMING



Transfer of the RX CMD byte occurs in Synchronous Mode when the PHY has control of the bus. The ULPI Protocol Block shown in Figure 6-1 determines when to send an RX CMD. A RX CMD will occur:

- When a linestate change occurs.
- When VBUS or ID comparators change state.
- During a USB receive when **NXT** is low.
- After the USB83340 de-asserts **DIR** and **STP** is low during start-up
- After the USB83340 exits Low Power Mode, Serial Modes, or Carkit Mode after detecting that the Link has de-asserted **STP**, and **DIR** is low.

When a USB Receive is occurring, RX CMDs are sent whenever **NXT** = 0 and **DIR** = 1. During a USB transmit, the RX CMDs are returned to the Link after **STP** is asserted.

If an RX CMD event occurs during a high-speed USB transmit, the RX CMD is blocked until **STP** de-asserts at the end of the transmit. The RX CMD contains the status that is current at the time the RX CMD is sent.

TABLE 6-3: ULPI RX CMD ENCODING

<table>
<tr><th>Data[7:0]</th><th>Name</th><th colspan="5">Description and Value</th></tr>
<tr><td>[1:0]</td><td>Linestate</td><td colspan="5">UTMI Linestate Signals. See Section 6.3.1.1</td></tr>
<tr><td rowspan="5">[3:2]</td><td rowspan="5">Encoded VBUS State</td><td colspan="5">Encoded VBUS Voltage States</td></tr>
<tr><td>Value</td><td>VBUS Voltage</td><td>Sessend</td><td>Sessvld</td><td>Vbusvld(2)</td></tr>
<tr><td>00</td><td>$V_{VBUS} < V_{SESS\_END}$</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>01</td><td>$V_{SESS\_END} < V_{VBUS} < V_{SESS\_VLD}$</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>10</td><td>$V_{SESS\_VLD} < V_{VBUS} < V_{VBUS\_VLD}$</td><td>X</td><td>1</td><td>0</td></tr>
<tr><td></td><td></td><td>11</td><td>$V_{VBUS\_VLD} < V_{VBUS}$</td><td>X</td><td>X</td><td>1</td></tr>
<tr><td rowspan="5">[5:4]</td><td rowspan="5">RX Event Encoding</td><td colspan="5">Encoded UTMI Event Signals</td></tr>
<tr><td>Value</td><td>RXACTIVE</td><td>RXERROR</td><td colspan="2">HostDisconnect</td></tr>
<tr><td>00</td><td>0</td><td>0</td><td colspan="2">0</td></tr>
<tr><td>01</td><td>1</td><td>0</td><td colspan="2">0</td></tr>
<tr><td>11</td><td>1</td><td>1</td><td colspan="2">0</td></tr>
<tr><td></td><td></td><td>10</td><td>X</td><td>X</td><td colspan="2">1</td></tr>
<tr><td>[6]</td><td>State of ID pin</td><td colspan="5">Set to the logic state of the ID pin. A logic low indicates an A-device. A logic high indicates a B-device.</td></tr>
<tr><td>[7]</td><td>alt_int</td><td colspan="5">Asserted when a non-USB interrupt occurs. This bit is set when an unmasked event occurs on any bit in the Carkit Interrupt Latch register. The Link must read the Carkit Interrupt Latch register to determine the source of the interrupt. Section 6.8 describes how an interrupt can be generated when the RidConversionDone bit is set.</td></tr>
</table>

Note 1: An ‘X’ is a do not care and can be either a logic 0 or 1.

2: The value of VbusValid is defined in Table 5-6.

6.3.1.1 Definition of Linestate

The Linestate information is used to relay information back to the Link on the current status of the USB data lines, **DP** and **DM**. The definition of Linestate changes as the USB83340 transitions between LS/FS mode, HS mode, and HS chirp.

6.3.1.1.1 LS/FS Linestate Definitions

In LS and FS operating modes the Linestate is defined by the outputs of the LS/FS single-ended receivers (SE RX). The logic thresholds for single-ended receivers, V_{ILSE} and V_{ILSE} are specified in the USB 2.0 specification.

TABLE 6-4: USB LINESTATE DECODING IN FS AND LS MODE

Linestate[1:0]		DP SE RX	DM SE RX	State
00	SE0	0	0	USB Reset
01	J (FS Idle)	1	0	J State
10	K (LS Idle)	0	1	K State
11	SE1	1	1	SE1

Low-speed uses the same Linestate decoding threshold as full-speed. Low-speed re-defines the Idle state as an inversion of the full-speed Idle to account for the inversion which occurs in the hub repeater path. Linestates are decoded exactly as in Table 6-4 with the Idle as a K state.

6.3.1.1.2 HS Linestate Definition

In HS mode the data transmission is too fast for Linestate to be transmitted with each transition in the data packet. In HS operation the Linestate is redefined to indicate activity on the USB interface. The Linestate will signal the assertion and de-assertion of squelch in HS mode.

TABLE 6-5: USB LINESTATE DECODING IN HS MODE

Linestate[1:0]		DP SE RX	DM SE RX	State
00	SE0	0	0	HS Squelch asserted
01	J	1	0	HS Squelch de-asserted
10	K	0	1	Invalid State
11	SE1	1	1	Invalid State

6.3.1.1.3 HS CHIRP Linestate Definition

There is also a third use of Linestate in HS chirp where when the host and peripheral negotiate the from FS mode to HS mode. While the transitions from K to J or SE0 are communicated to the Link through the Linestate information.

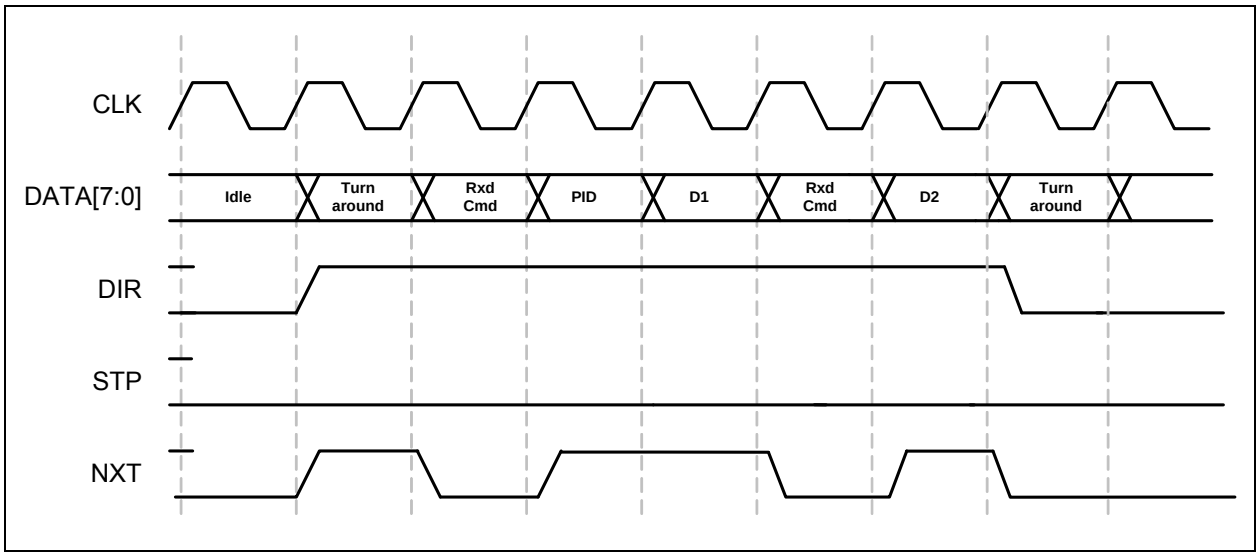
TABLE 6-6: USB LINESTATE DECODING IN HS CHIRP MODE

Linestate[1:0]		DP SE RX	DM SE RX	State
00	SE0	0	0	HS Squelch asserted
01	J	1	0	HS Squelch de-asserted & HS differential Receiver = 1
10	K	0	1	HS Squelch de-asserted & HS differential Receiver = 0
11	SE1	1	1	Invalid State

6.3.2 USB RECEIVER

The USB83340 ULPI receiver fully supports HS, FS, and LS transmit operations. In all three modes the receiver detects the start of packet and synchronizes to the incoming data packet. In the ULPI protocol, a received packet has the priority and will immediately follow register reads and RX CMD transfers. Figure 6-8 shows a basic USB packet received by the USB83340 over the ULPI interface.

FIGURE 6-8: ULPI RECEIVE IN SYNCHRONOUS MODE



In Figure 6-8 the PHY asserts **DIR** to take control of the data bus from the Link. The assertion of **DIR** and **NXT** in the same cycle contains additional information that Rxactive has been asserted. When **NXT** is de-asserted and **DIR** is asserted, the RX CMD data is transferred to the Link. After the last byte of the USB receive packet is transferred to the PHY, the Linestate will return to idle.

The ULPI full-speed receiver operates according to the UTMI / ULPI specification. In the full-speed case, the **NXT** signal will assert only when the data bus has a valid received data byte. When **NXT** is low with **DIR** high, the RX CMD is driven on the data bus.

In full-speed, the USB83340 will not issue an Rxactive de-assertion in the RX CMD until the DP/DM Linestate transitions to idle. This prevents the Link from violating the two full-speed bit times minimum turn around time.

6.3.2.1 Disconnect Detection

A high-speed host must detect a disconnect by sampling the transmitter outputs during the long EOP transmitted during an SOF packet. The USB83340 only looks for a high-speed disconnect during the long EOP where the period is long enough for the disconnect reflection to return to the host PHY. When a high-speed disconnect occurs, the USB83340 will return an RX CMD and set the host disconnect bit in the USB Interrupt Status register.

When in FS or LS modes, the Link is expected to handle all disconnect detection.

6.3.2.2 Link Power Management (LPM) Token Receive

The USB83340 is fully capable of receiving the extended PID in the LPM token. When the LPM 0000b PID is received, this information is passed to the Link as a normal receive packet. If the Link chooses to enter LPM suspend, the procedure detailed in Section 6.5.3 can be followed.

6.4 USB83340 Transmitter

The USB83340 ULPI transmitter fully supports HS, FS, and LS transmit operations. Figure 6-1 shows the High-Speed, Full-Speed, and Low-Speed transmitter block controlled by ULPI Protocol Block. Encoding of the USB packet follows the bit-stuffing and NRZI outlined in the USB 2.0 specification. Many of these functions are reused between the HS and FS/LS transmitters. When using the USB83340, Table 5-1 should always be used as a guideline on how to configure for various modes of operation. The transmitter decodes the inputs of *XcvrSelect[1:0]*, *TermSelect*, *OpMode[1:0]*, *DpPulldown,* and *DmPulldown* to determine what operation is expected. Users must strictly adhere to the modes of operation given in Table 5-1.

Several important functions for a device and host are designed into the transmitter blocks.

The USB83340 transmitter will transmit a 32-bit long high-speed sync before every high-speed packet. In full- and low-speed modes an 8-bit sync is transmitted.

When the device or host needs to chirp for high-speed port negotiation, the *OpMode* = 10 setting will turn off the bit-stuffing and NRZI encoding in the transmitter. At the end of a chirp, the USB83340 *OpMode* register bits should be changed only after the RX CMD Linestate encoding indicates that the transmitter has completed transmitting. Should the operation mode be switched to normal bit-stuffing and NRZI encoding before the transmit pipeline is empty, the remaining data in the pipeline may be transmitted in an bit-stuff encoding format.

Please refer to the ULPI specification for a detailed discussion of USB reset and HS chirp.

6.4.1 USB83340 HOST FEATURES

The USB83340 can also support USB host operation and includes the following features that are required for host operation.

6.4.1.1 High-Speed Long EOP

When operating as a high-speed host, the USB83340 will automatically generate a 40-bit long End-of-Packet (EOP) after a SOF PID (A5h). The USB83340 determines when to send the 40-bit long EOP by decoding the ULPI TX CMD bits [3:0] for the SOF. The 40-bit long EOP is only transmitted when the *DpPulldown* and *DmPulldown* bits in the OTG Control register are asserted. The high-speed 40-bit long EOP is used to detect a disconnect in mode.

In device mode, the USB83340 will not send a long EOP after a SOF PID.

6.4.1.2 Low-Speed Keep-Alive

Low-speed keep alive is supported by the USB83340. When in low-speed mode, the USB83340 will send out two low-speed bit times of SE0 when a SOF PID is received.

6.4.1.3 UTMI+ Level 3

Pre-amble is supported for UTMI+ Level 3 compatibility. When *XcvrSelect* is set to (11b) in host mode, (*DpPulldown* and *DmPulldown* both asserted) the USB83340 will prepend a full-speed pre-amble before the low-speed packet. Full-speed rise and fall times are used in this mode. The pre-amble consists of the following: full-speed sync, the encoded pre-PID (C3h) and then full-speed idle (DP= 1 and DM = 0). A low-speed packet follows with a sync, data and a LS EOP.

The USB83340 will only support UTMI+ Level 3 as a host. The USB83340 does not support UTMI+ Level 3 as a peripheral. A UTMI+ Level 3 peripheral is an upstream hub port. The USB83340 will not decode a pre-amble packet intended for a LS device when the USB83340 is configured as the upstream port of a FS hub, *XcvrSelect* = 11b, *DpPulldown* = 0b, *DmPulldown* =0b.

6.4.1.4 Host Resume K

Resume K generation is supported by the USB83340. At the end of a USB Suspend the PHY will drive a K back to the downstream device. When the USB83340 exits from Low Power Mode, when operating as a host, it will automatically transmit a Resume K on DP/DM. The transmitters will end the K with SE0 for two low-speed bit times. If the USB83340 was operating in high-speed mode before the suspend, the host must change to high-speed mode before the SE0 ends. SE0 is two low-speed bit times which is about 1.2 µs. For more details please see sections 7.1.77 and 7.9 of the USB specification.

In device mode, the resume K will not append an SE0, but release the bus to the correct idle state, depending upon the operational mode as shown in Table 5-1.

The ULPI specification includes a detailed discussion of the resume sequence and the order of operations required. To support host start-up of less than 1 ms the USB83340 implements the ULPI *AutoResume* bit in the Interface Control register. The default *AutoResume* state is 0 and this bit should be enabled for host applications.

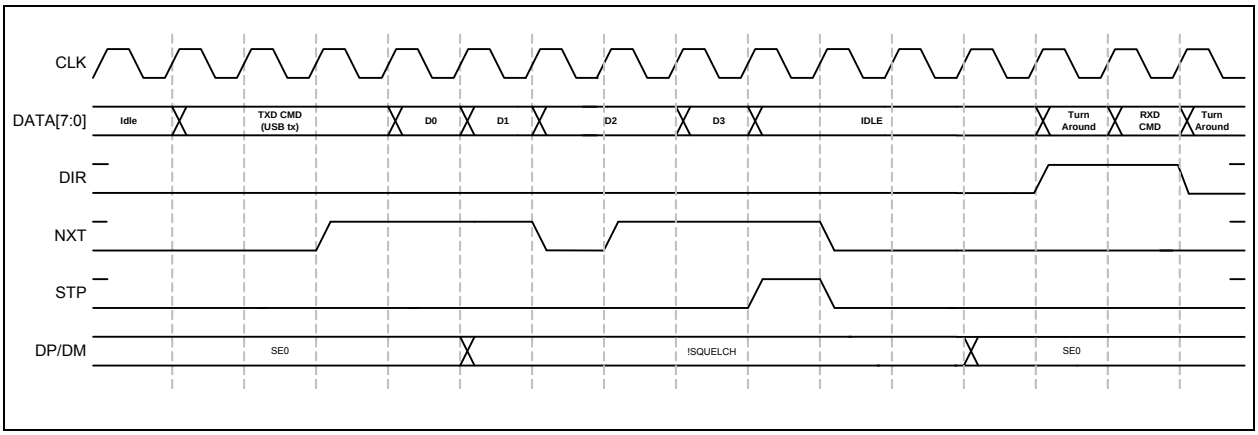
6.4.1.5 No SYNC and EOP Generation (*OpMode* = 11)

UTMI+ defines O*pMode* = 11 where no sync and EOP generation occurs in high-speed operation. This is an option to the ULPI specification and not implemented in the USB83340.

6.4.2 TYPICAL USB TRANSMIT WITH ULPI

Figure 6-9 shows a typical USB transmit sequence. A transmit sequence starts by the Link sending a TX CMD where **DATA[7:6]** = 01b, **DATA[5:4]** = 00b, and **Data[3:0]** = PID. The TX CMD with the PID is followed by transmit data.

FIGURE 6-9: ULPI TRANSMIT IN SYNCHRONOUS MODE



During transmit the PHY will use **NXT** to control the rate of data flow into the PHY. If the USB83340 pipeline is full or bit-stuffing causes the data pipeline to overfill **NXT** is de-asserted and the Link will hold the value on data until **NXT** is asserted. The USB transmit ends when the Link asserts **STP** while **NXT** is asserted.

Note:	The Link cannot assert **STP** with **NXT** de-asserted since the USB83340 is expecting to fetch another byte from the Link.

After the USB83340 completes transmitting, the **DP** and **DM** lines return to idle and an RX CMD is returned to the Link so the inter-packet timers may be updated by linestate.

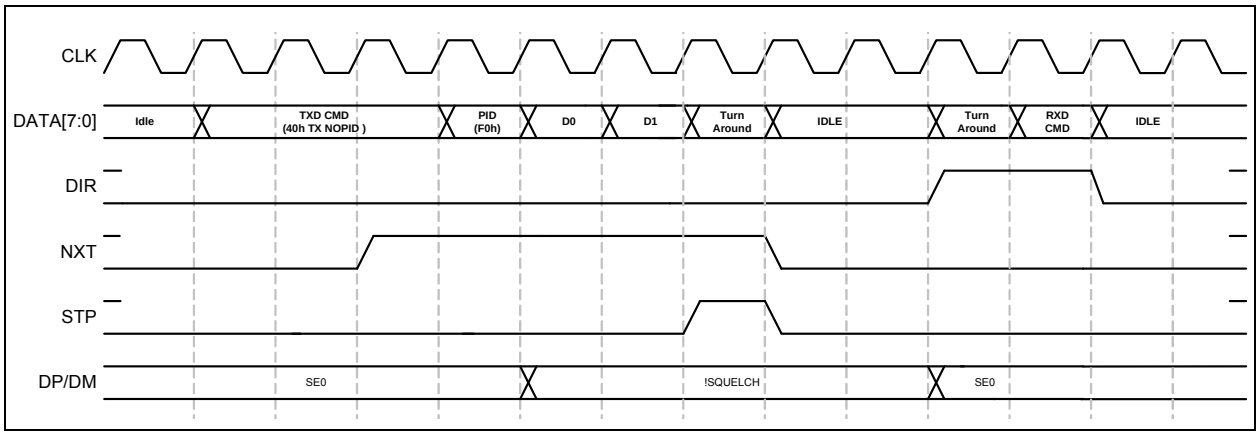
While operating in full-speed or low-speed, an End-of-Packet (EOP) is defined as SE0 for approximately two bit times, followed by J for one bit time. The transceiver drives a J state for one bit time following the SE0 to complete the EOP. The Link must wait for one bit time following linestate indication of the SE0 to J transition to allow the transceiver to complete the one bit time J state. All bit times are relative to the speed of transmission.

In the case of full-speed or low-speed, after **STP** is asserted each FS/LS bit transition will generate an RX CMD since the bit times are relatively slow.

6.4.2.1 Link Power Management Token Transmit

A host Link can send a LPM command using the USB83340. When sending the LPM token the normal transmit method is not used. Sending a LPM token requires the USB83340 to send a 0000b or ‘F0’ PID. When the ULPI specification was defined the ‘F0’ PID was not defined. The ULPI specification used the “Reserved” ‘F0’ PID to signal chirp and resume signaling while using *OpMode* 10b. While in *OpMode* 00b the USB83340 is able to generate the ‘F0’ PID as shown below.

FIGURE 6-10: LPM TOKEN TRANSMIT



To send the ‘F0’ PID, the Link will be required to use the TX CMD with NOPID to initiate the transmit and then follow up the TX CMD with the ‘F0’ PID. The data bytes follow as in a normal transmit, in *OpMode* 00b. The key difference is in that the link will have to send the PID the same as it would send a data packet. The USB83340 is able to recognize the LPM transmit and correctly send the PID information.

6.5 Low Power Mode

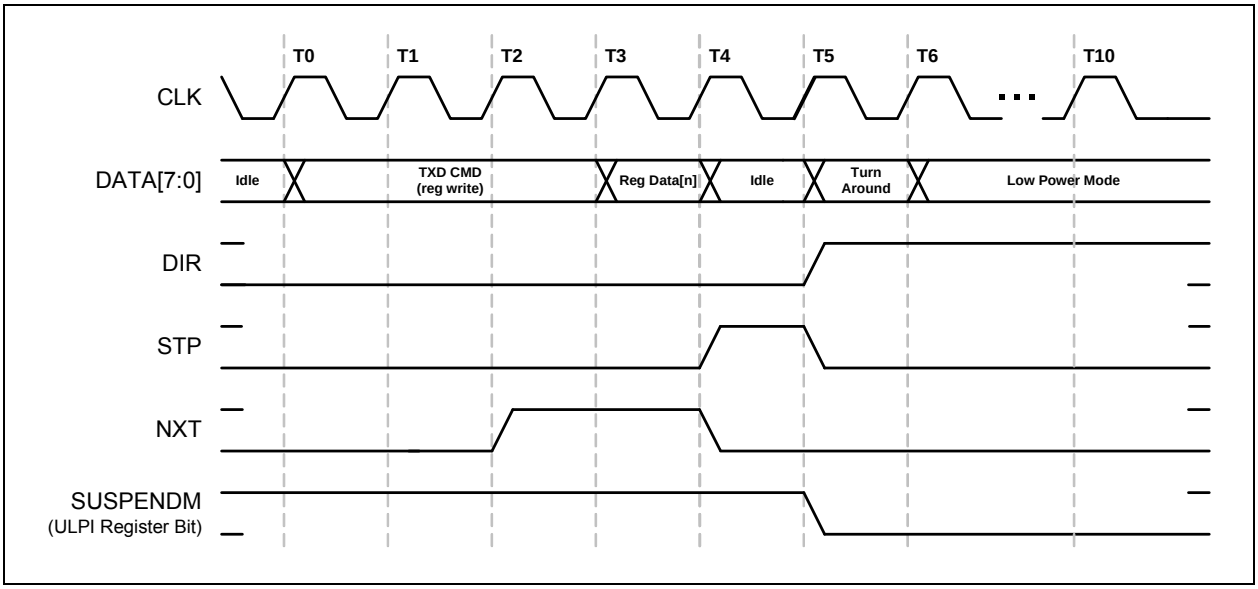
Low Power Mode is a power down state to save current when the USB session is suspended. The Link controls when the PHY is placed into or out of Low Power Mode. In Low Power Mode all of the circuits are powered down except the interface pins, full-speed receiver, VBUS comparators, and IdGnd comparator. The VBUS and ID comparators can optionally be powered down to save current as shown in Section 6.5.5.

Before entering Low Power Mode, the USB83340 must be configured to set the desired state of the USB transceiver. The *XcvrSelect[1:0]*, *TermSelect* and *OpMode[1:0]* bits in the Function Control register, and the *DpPulldown* and *DmPulldown* bits in the OTG Control register control the configuration as shown in Table 5-1. The **DP** and **DM** pins are configured to a high impedance state by configuring *OpMode[1:0]* = 01 as shown in the programming example in Table 6-8. Pull-down resistors with a value of approximately 2 MΩ are present on the **DP** and **DM** pins to avoid false linestate indications that could result if the pins were allowed to float.

6.5.1 ENTERING LOW POWER/SUSPEND MODE

To enter Low Power Mode, the Link will write a 0 or clear the *SuspendM* bit in the Function Control register. After this write is complete, the PHY will assert **DIR** high and after a minimum of five rising edges of **CLKOUT**, drive the clock low. After the clock is stopped, the PHY will enter a low power state to conserve current. Placing the PHY in Suspend Mode is not related to USB Suspend. To clarify this point, USB Suspend is initiated when a USB host stops data transmissions and enters full-speed mode with 15 kΩ pull-down resistors on **DP** and **DM**. The suspended device goes to full-speed mode with a pull-up on **DP**. Both the host and device remain in this state until one of them drives **DM** high (this is called a resume).

FIGURE 6-11: ENTERING LOW POWER MODE FROM SYNCHRONOUS MODE



While in Low Power Mode, the data interface is redefined so that the Link can monitor Linestate and the VBUS voltage. In Low Power Mode **DATA[3:0]** are redefined as shown in Table 6-7. Linestate[1:0] is the combinational output of the single-ended receivers. The “int” or interrupt signal indicates an unmasked interrupt has occurred. When an unmasked interrupt or Linestate change has occurred, the Link is notified and can determine if it should wake-up the PHY.

TABLE 6-7: INTERFACE SIGNAL MAPPING DURING LOW POWER MODE

Signal	Maps to	Direction	Description
Linestate[0]	**DATA[0]**	OUT	Combinatorial Linestate[0] driven directly by the full-speed single-ended receiver. Note 3
Linestate[1]	**DATA[1]**	OUT	Combinatorial Linestate[1] driven directly by the full-speed single-ended receiver. Note 3
Reserved	**DATA[2]**	OUT	Driven low
Int	**DATA[3]**	OUT	Active high interrupt indication. Must be asserted whenever any unmasked interrupt occurs.
Reserved	**DATA[7:4]**	OUT	Driven low

3: Linestate: These signals reflect the current state of the full-speed single-ended receivers. Linestate[0] directly reflects the current state of **DP**. Linestate[1] directly reflects the current state of **DM**. When **DP=DM=**0 this is called "Single-Ended Zero" (SE0). When **DP=DM=**1, this is called "Single-Ended One" (SE1).

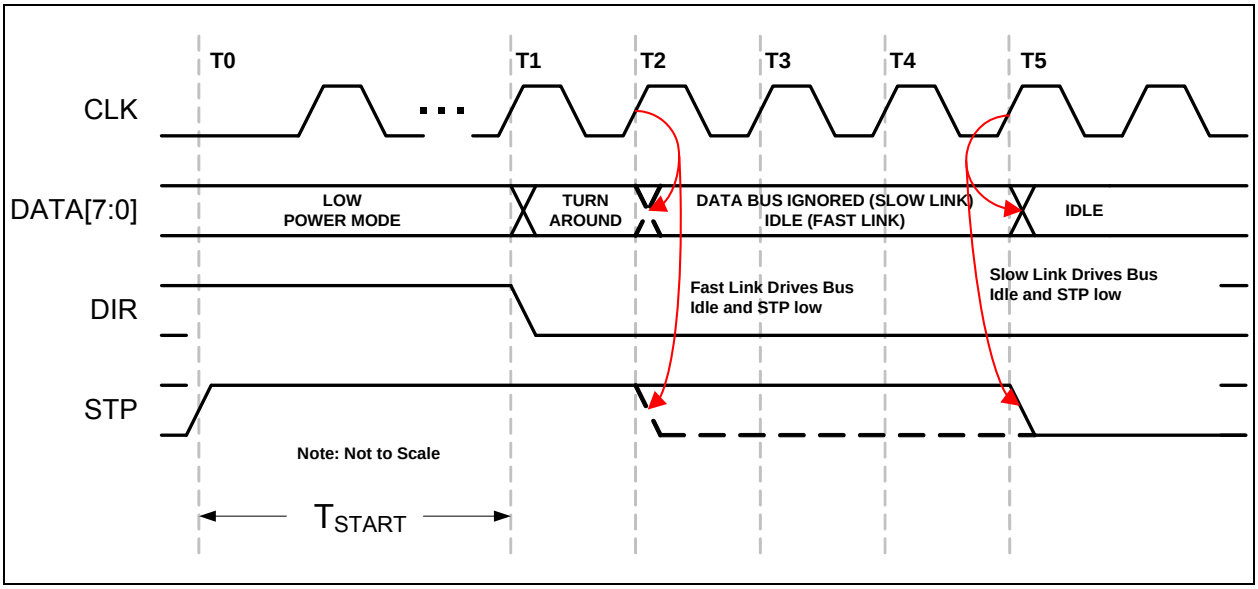
An unmasked interrupt can be caused by the following comparators changing state: VbusVld, SessVld, SessEnd, and IdGnd. If any of these signals change state during Low Power Mode and the bits are enabled in either the USB Interrupt Enable Rising or USB Interrupt Enable Falling registers, **DATA[3]** will assert. During Low Power Mode, the VbusVld and SessEnd comparators can have their interrupts masked to lower the suspend current as described in Section 6.5.5.

While in Low Power Mode, the data bus is driven asynchronously because all of the PHY clocks are stopped during Low Power Mode.

6.5.2 EXITING LOW POWER MODE

To exit Low Power Mode, the Link will assert **STP**. Upon the assertion of **STP**, the USB83340 will begin its start-up procedure. After the PHY start-up is complete, the PHY will start the clock on **CLKOUT** and de-assert **DIR**. After **DIR** has been de-asserted, the Link can de-assert **STP** when ready and start operating in Synchronous Mode. The PHY will automatically set the *SuspendM* bit to a 1 in the Function Control register.

FIGURE 6-12: EXITING LOW POWER MODE



The value for T_{START} is given in Table 4-2.

Should the Link de-assert **STP** before **DIR** is de-asserted, the USB83340 will detect this as a false resume request and return to Low Power Mode. This is detailed in Section 3.9.4 of the UTMI+ Low Pin Interface (ULPI) Specification, Revision 1.1.

6.5.3 LINK POWER MANAGEMENT (LPM)

When the USB83340 is operating with a Link capable of Link Power Management, the Link will place the USB83340 in and out of suspend rapidly to conserve power. The USB83340 provides a fast suspend recovery that allows the USB83340 to meet the suspend recovery time detailed in the Link Power Management ECN to the USB 2.0 specification.

When the Link places the USB83340 into suspend during Link Power Management, the *LPM Enable* bit of the HS Compensation and LPM Register must be set to 1. This allows the USB83340 to start-up in the time specified in Table 4-2.

6.5.4 INTERFACE PROTECTION

ULPI protocol assumes that both the Link and PHY will keep the ULPI data bus driven by either the Link when **DIR** is low or the PHY when **DIR** is high. The only exception is when **DIR** has changed state and a turn around cycle occurs for 1 clock period.

In the design of a USB system, there can be cases where the Link may not be driving the ULPI bus to a known state while **DIR** is low. Two examples where this can happen is because of a slow Link start-up or a hardware reset.

6.5.4.1 Start-up Protection

Upon start-up, when the PHY de-asserts **DIR**, the Link must be ready to receive commands and drive Idle on the data bus. If the Link is not ready to receive commands or drive Idle, it must assert **STP** before **DIR** is de-asserted. The Link can then de-assert **STP** when it has completed its start-up. If the Link doesn't assert **STP** before it can receive commands, the **PHY** may interpret the data bus state as a TX CMD and transmit invalid data onto the **USB** bus, or make invalid register writes.

When the USB83340 sends an RX CMD the Link is required to drive the data bus back to idle at the end of the turn around cycle. If the Link does not drive the databus to idle the USB83340 may take the information on the data bus as a TX CMD and transmit data on **DP** and **DM** until the Link asserts stop. If the **ID** pin is floated the last RX CMD from the USB83340 will remain on the bus after **DIR** is de-asserted and the USB83340 will take this in as a TX CMD.

A Link should be designed to have the default POR state of the **STP** output high and the data bus tri-stated. The USB83340 has weak pull-downs on the data bus to prevent these inputs from floating when not driven. These resistors are only used to prevent the ULPI interface from floating during events when the link ULPI pins may be tri-stated. The strength of the pull-down resistors can be found in Table 4-4. The pull-downs are not strong enough to pull the data bus low after a ULPI RX CMD, the Link must drive the data bus to idle after **DIR** is de-asserted.

In some cases, a Link may be software configured and not have control of its **STP** pin until after the PHY has started. In this case, the USB83340 has an internal pull-up on the **STP** input pad which will pull **STP** high while the Link's **STP** output is tri-stated. The **STP** pull-up resistor is enabled on POR and can be disabled by setting the *InterfaceProtectDisable* bit 7 of the Interface Control register.

The **STP** pull-up resistor will pull-up the Link's **STP** input high until the Link configures and drives **STP** high. After the Link completes its start-up, **STP** can be synchronously driven low.

A Link design which drives **STP** high during POR can disable the pull-up resistor on **STP** by setting *InterfaceProtectDisable* bit to 1. A motivation for this is to reduce the suspend current. In Low Power Mode, **STP** is held low, which would draw current through the pull-up resistor on **STP**.

6.5.4.2 Warm Reset

Designers should also consider the case of a warm restart of a Link with a PHY in Low Power Mode. After the PHY enters Low Power Mode, **DIR** is asserted and the clock is stopped. The USB83340 looks for **STP** to be asserted to re-start the clock and then resume normal synchronous operation.

Should the USB83340 be suspended in Low Power Mode, and the Link receives a hardware reset, the PHY must be able to recover from Low Power Mode and start its clock. If the Link asserts **STP** on reset, the PHY will exit Low Power Mode and start its clock.

If the Link does not assert **STP** on reset, the interface protection pull-up can be used. When the Link is reset, its **STP** output will tri-state and the pull-up resistor will pull **STP** high, signaling the PHY to restart its clock.

6.5.5 MINIMIZING CURRENT IN LOW POWER MODE

In order to minimize the suspend current in Low Power Mode, the VBUS and ID comparators can be disabled to reduce suspend current. In Low Power Mode, the VbusVld and SessEnd comparators are not needed and can be disabled by clearing the associated bits in both the USB Interrupt Enable Rising and USB Interrupt Enable Falling registers. By disabling the interrupt in BOTH the rise and fall registers, the SessEnd and VbusVld comparators are turned off. The *IdFloatRise* and *IdFloatFall* bits in Carkit Interrupt Enable register should also be disabled if they were set. When exiting Low Power Mode, the Link should immediately re-enable the VbusVld and SessEnd comparators if host or OTG functionality is required.

In addition to disabling the OTG comparators in Low Power Mode, the Link may choose to disable the Interface Protect Circuit. By setting the *InterfaceProtectDisable* bit high in the Interface Control register, the Link can disable the pull-up resistor on **STP**. When **RESETB** is low the Interface Protect Circuit will be disabled.

6.6 Full-Speed/Low-Speed Serial Modes

The USB83340 includes two serial modes to support legacy Links which use either the 3-pin or 6-pin serial format. To enter either serial mode, the Link will need to write a 1 to the *6-pin FsLsSerialMode* or the *3-pin FsLsSerialMode* bits in the Interface Control register. Serial mode may be used to conserve power when attached to a device that is not capable of operating in high-speed.

The serial modes are entered in the same manner as the entry into Low Power Mode. The Link writes the Interface Control register bit for the specific serial mode. The USB83340 will assert **DIR** and shut off the clock after at least five clock cycles. Then the data bus goes to the format of the serial mode selected. Before entering serial mode the Link must set the ULPI transceiver to the appropriate mode as defined in Table 5-1.

In ULPI Clock Out Mode, the PHY will shut off the 60 MHz clock to conserve power. Should the Link need the 60 MHz clock to continue during the serial mode of operation, the *ClockSuspendM* bit[3] of the Interface Control register should be set before entering a serial mode. If set, the 60 MHz clock will be present during serial modes.

In serial mode, interrupts are possible from unmasked sources. The state of each interrupt source is sampled prior to the assertion of **DIR** and this is compared against the asynchronous level from interrupt source.

Exiting the serial modes is the same as exiting Low Power Mode. The Link must assert **STP** to signal the PHY to exit serial mode. When the PHY can accept a command, **DIR** is de-asserted and the PHY will wait until the Link de-asserts **STP** to resume synchronous ULPI operation. The **RESETB** pin can also be pulsed low to reset the USB83340 and return it to Synchronous Mode.

6.6.1 3-PIN FS/LS SERIAL MODE

Three pin serial mode utilizes the data bus pins for the serial functions shown in Table 6-8.

TABLE 6-8: PIN DEFINITIONS IN 3-PIN SERIAL MODE

Signal	Connected To	Direction	Description
tx_enable	**DATA[0]**	IN	Active high transmit enable.
data	**DATA[1]**	I/O	TX differential data on DP/DM when tx_enable is high. RX differential data from DP/DM when tx_enable is low.
SE0	**DATA[2]**	I/O	TX SE0 on DP/DM when tx_enable is high. RX SE0_b from DP/DM when tx_enable is low.
interrupt	**DATA[3]**	OUT	Asserted when any unmasked interrupt occurs. Active high.
Reserved	**DATA[7:4]**	OUT	Driven low.

6.6.2 6-PIN FS/LS SERIAL MODE

Six pin serial mode utilizes the data bus pins for the serial functions shown in Table 6-9.

TABLE 6-9: PIN DEFINITIONS IN 6-PIN SERIAL MODE

Signal	Connected To	Direction	Description
tx_enable	**DATA[0]**	IN	Active high transmit enable.
tx_data	**DATA[1]**	IN	Tx differential data on DP/DM when tx_enable is high.
tx_se0	**DATA[2]**	IN	Tx SE0 on DP/DM when tx_enable is high.
interrupt	**DATA[3]**	OUT	Asserted when any unmasked interrupt occurs. Active high.
rx_dp	**DATA[4]**	OUT	Single-ended receive data on DP.
rx_dm	**DATA[5]**	OUT	Single-ended receive data on DM.
rx_rcv	**DATA[6]**	OUT	Differential receive data from DP and DM.
Reserved	**DATA[7]**	OUT	Driven low.

6.7 Carkit Mode

The USB83340 includes Carkit Mode to support a USB UART and USB Audio Mode.

By entering Carkit Mode, the USB83340 current drain is minimized. The internal PLL is disabled and the 60 MHz ULPI **CLKOUT** will be stopped to conserve power by default. The Link may configure the 60 MHz clock to continue by setting the *ClockSuspendM* bit of the Interface Control register before entering Carkit Mode. If set, the 60 MHz clock will continue during the Carkit Mode of operation.

In Carkit Mode, interrupts are possible if they have been enabled in the Carkit Interrupt Enable register. The state of each interrupt source is sampled prior to the assertion of **DIR** and this is compared against the asynchronous level from interrupt source. In Carkit Mode, the Linestate signals are not available per the ULPI specification.

The ULPI interface is redefined to the following when Carkit Mode is entered.

TABLE 6-10: PIN DEFINITIONS IN CARKIT MODE

Signal	Connected To	Direction	Description
txd	**DATA[0]**	IN	UART TXD signal that is routed to the **DM** pin if the *TxdEn* is set in the Carkit Control register.
rxd	**DATA[1]**	OUT	UART RXD signal that is routed to the **DP** pin if the *RxdEn* bit is set in the Carkit Control register.
Reserved	**DATA[2]**	OUT	Driven low (*CarkitDataMC = 0, default)*
		IN	Tri-state *(CarkitDataMC = 1)*
int	**DATA[3]**	OUT	Asserted when any unmasked interrupt occurs. Active high.
Reserved	**DATA[4:7]**	OUT	Driven low.

Exiting Carkit Mode is the same as exiting Low Power Mode as described in Section 6.5.2. The Link must assert **STP** to signal the PHY to exit serial mode. When the PHY can accept a command, **DIR** is de-asserted and the PHY will wait until the Link de-asserts **STP** to resume synchronous ULPI operation. The **RESETB** pin can also be pulsed low to reset the USB83340 and return it to Synchronous Mode.

6.7.1 ENTERING USB UART MODE

The USB83340 can be placed into UART Mode by first setting the *TxdEn* and *RxdEn* bits in the Carkit Control register. Then the Link can set the *CarkitMode* bit in the Interface Control register. The *TxdEn* and *RxdEn* bits must be written before the *CarkitMode* bit.

TABLE 6-11: ULPI REGISTER PROGRAMMING EXAMPLE TO ENTER UART MODE

R/W	Address (HEX)	Value (HEX)	Description	Result
W	04	49	Configure Non-Driving mode Select FS transmit edge rates	*OpMode*=01 *XcvrSelect*=01
W	39	00	Set regulator to 3.3 V	*UART RegOutput*=00
W	19	0C	Enable UART connections	*RxdEn*=1 *TxdEn*=1
W	07	04	Enable Carkit Mode	*CarkitMode*=1

After the *CarkitMode* bit is set, the ULPI interface will become redefined as described in Table 6-10, and the USB83340 will transmit data through the **DATA[0]** to **DM** of the USB connector and receive data on **DP** and pass the information to the Link on **DATA[1]**.

When entering UART Mode, the regulator output will automatically switch to the value configured by the *UART RegOutput bits in the* USB IO & Power Management register and the R_{CD} pull-up resistors will be applied internally to **DP** and **DM**. This will hold the UART in its default operating state.

While in UART Mode, the transmit edge rates can be set to either the full-speed USB or low-speed USB edge rates by using the *XcvrSelect[1:0]* bits in the Function Control register.

6.7.2 USB AUDIO MODE

When the USB83340 is powered in Synchronous Mode, the Audio switches can be enabled by asserting the *SpkLeftEn*, or *SpkRightEn* bits in the Carkit Control register. After the register write is complete, the USB83340 will immediately enable or disable the audio switch. Then the Link can set the *CarkitMode* bit in the Interface Control register. The *SpkLeftEn*, or *SpkRightEn* bits must be written before the *CarkitMode* bit.

TABLE 6-12: ULPI REGISTER PROGRAMMING EXAMPLE TO ENTER AUDIO MODE

R/W	Address (HEX)	Value (HEX)	Description	Result
W	04	48	Configure Non-Driving mode	*OpMode*=01
W	19	30	Enable Audio connections	*SpkrRightEn*=1, *SpkrLeftEn*=1
W	07	04	Enable Carkit Mode	*CarkitMode*=1

After the *CarkitMode* bit is set, the ULPI interface will become redefined as described in Table 6-10.

6.8 R_{ID} Converter Operation

The R_{ID} converter is designed to read the value of the ID resistance to ground and report back its value through the ULPI interface.

When a resistor to ground is applied to the **ID** pin the state of the IdGnd comparator will change from a 1 to a 0 as described in Section 5.6.1. If the USB83340 is in ULPI mode, an RX CMD will be generated with bit 6 low. If the USB83340 is in Low Power Mode (or one of the other non-ULPI modes), the DATA[3] interrupt signal will go high.

After the USB83340 has detected the change of state on the **ID** pin, the R_{ID} converter can be used to determine the value of ID resistance. To start an ID resistance measurement, the *RidConversionStart* bit is set in the Vendor R_{ID} Conversion register.

The Link can use one of two methods to determine when the R_{ID} conversion is complete. One method is polling the *RidConversionStart* bit as described in Section 7.1.3.4. The preferred method is to set the *RidIntEn* bit in the Vendor R_{ID} Conversion register. When *RidIntEn* is set, an RX CMD will be generated after the R_{ID} conversion is complete. As described in Table 6-3, the *alt_int* bit of the RX CMD will be set.

After the R_{ID} conversion is complete, the Link can read *RidValue* from the Vendor R_{ID} Conversion register.

6.8.1 HEADSET AUDIO MODE

This mode is designed to allow a user to view the status of several signals while using an analog audio headset with a USB connector. This mode is provided as an alternate mode to the CarKit Mode defined in Section 6.7. In the CarKit Mode the Link is unable to view the source of the interrupt on ID. For the Link to view the interrupt on ID the PHY must be returned to Synchronous Mode so the interrupt can be read. This will force the audio switches to be deactivated during the PHY start-up which may glitch the audio signals. In addition the Link can not change the resistance on the ID pin without starting up the PHY to access the ULPI registers.

The Headset Audio Mode is entered by writing to the Headset Audio Mode register, and allows the Link access to the state of the **VBUS** and **ID** pins during audio without having to break the audio connection. The Headset Audio Mode also allows for the Link to change the resistance on the **ID** pin to change the audio device attached from mono to stereo.

TABLE 6-13: PIN DEFINITIONS IN HEADSET AUDIO MODE

Signal	Connected To	Direction	Description
SessVld	**DATA[0]**	OUT	Output of SessVld comparator
VbusVld	**DATA[1]**	OUT	Output of VbusVld comparator (interrupt must be enabled)
IdGndDrv	**DATA[2]**	IN	Drives **ID** pin to ground when asserted. 0b: Not connected 1b: Connects **ID** to ground.
	DATA[3]	OUT	Driven low
IdGround	**DATA[4]**	OUT	Asserted when the **ID** pin is grounded. 0b: **ID** pin is grounded. 1b: **ID** pin is floating.
IdFloat	**DATA[5]**	OUT	Asserted when the **ID** pin is floating. *IdPullup* or *Id_pullup330* must be enabled. *IdFloatRise* and *IdFloatFall* must be enabled.
IdPullup330	**DATA[6]**	IN	When enabled a 330 kΩ pull-up is applied to the **ID** pin. This bit will also change the trip point of the IdGnd comparator to the value shown in Table 4-5. 0b: Disables the pull-up resistor 1b: Enables the pull-up resistor
IdPullup	**DATA[7]**	IN	Connects the 100 kΩ pull-up resistor from the **ID** pin to **VDD33** 0b: Disables the pull-up resistor 1b: Enables the pull-up resistor

Exiting Headset Audio Mode is the same as exiting Low Power Mode as described in Section 6.5.2. The **RESETB** pin can also be pulsed low to reset the USB83340 and return to Synchronous Mode.

7.0 ULPI REGISTER MAP

7.1 ULPI Register Array

The USB83340 PHY implements all of the ULPI registers detailed in the ULPI revision 1.1 specification. The complete USB83340 ULPI register set is shown in Table 7-1. All registers are 8 bits. This table also includes the default state of each register upon POR or de-assertion of **RESETB**, as described in Section 5.5.2. The RESET bit in the Function Control register does not reset the bits of the ULPI register array. The Link should not read or write to any registers not listed in this table.

The USB83340 supports extended register access. The immediate register set (00-3Fh) can be accessed through either an immediate address or an extended register address.

TABLE 7-1: ULPI REGISTER MAP

Register Name	Default State	Address (6 Bit)			
		READ	WRITE	SET	CLEAR
Vendor ID Low	24h	00h	-	-	-
Vendor ID High	04h	01h	-	-	-
Product ID Low	09h	02h	-	-	-
Product ID High	00h	03h	-	-	-
Function Control	41h	04-06h	04h	05h	06h
Interface Control	00h	07-09h	07h	08h	09h
OTG Control	06h	0A-0Ch	0Ah	0Bh	0Ch
USB Interrupt Enable Rising	1Fh	0D-0Fh	0Dh	0Eh	0Fh
USB Interrupt Enable Falling	1Fh	10-12h	10h	11h	12h
USB Interrupt Status (Note 1)	00h	13h	-	-	-
USB Interrupt Latch	00h	14h	-	-	-
Debug	00h	15h	-	-	-
Scratch Register	00h	16-18h	16h	17h	18h
Carkit Control	00h	19-1Bh	19h	1Ah	1Bh
Reserved	00h	1Ch			
Carkit Interrupt Enable	00h	1D-1Fh	1Dh	1Eh	1Fh
Carkit Interrupt Status	00h	20h	-	-	-
Carkit Interrupt Latch	00h	21h	-	-	-
Reserved	00h	22-30h			
HS Compensation and LPM Register	00h	31h	31h	-	-
USB-IF Charger Detection	00h	32h	32h	-	-
Headset Audio Mode	00	33	33	-	-
Reserved	00h	34-35h			
Vendor R_{ID} Conversion	00h	36-38h	36h	37h	38h
USB IO & Power Management	04h	39-3Bh	39h	3Ah	3Bh
Reserved	00h	3C-3Fh			

Note 1: Dynamically updates to reflect current status of interrupt sources.

7.1.1 ULPI REGISTER SET

The following registers are used for the ULPI interface.

7.1.1.1 Vendor ID Low

Address = 00h (read only)

Field Name	Bit	Access	Default	Description
Vendor ID Low	7:0	rd	24h	Microchip Vendor ID

7.1.1.2 Vendor ID High

Address = 01h (read only)

Field Name	Bit	Access	Default	Description
Vendor ID High	7:0	rd	04h	Microchip Vendor ID

7.1.1.3 Product ID Low

Address = 02h (read only)

Field Name	Bit	Access	Default	Description
Product ID Low	7:0	rd	09h	Microchip Product ID

7.1.1.4 Product ID High

Address = 03h (read only)

Field Name	Bit	Access	Default	Description
Product ID High	7:0	rd	00h	Microchip Product ID

7.1.1.5 Function Control

Address = 04-06h (read), 04h (write), 05h (set), 06h (clear)

Field Name	Bit	Access	Default	Description
XcvrSelect[1:0]	1:0	rd/w/s/c	01b	Selects the required transceiver speed. 00b: Enables HS transceiver 01b: Enables FS transceiver 10b: Enables LS transceiver 11b: Enables FS transceiver for LS packets (FS preamble automatically prepended)
TermSelect	2	rd/w/s/c	0b	Controls the DP and DM termination depending on *XcvrSelect*, *OpMode*, *DpPulldown*, and *DmPulldown*. The DP and DM termination is detailed in Table 5-1.
OpMode	4:3	rd/w/s/c	00b	Selects the required bit encoding style during transmit. 00b: Normal operation 01b: Non-Driving 10b: Disable bit-stuff and NRZI encoding 11b: Reserved
Reset	5	rd/w/s/c	0b	Active high transceiver reset. This reset does not reset the ULPI interface or register set. Automatically clears after reset is complete.
SuspendM	6	rd/w/s/c	1b	Active low PHY suspend. When cleared the PHY will enter Low Power Mode as detailed in Section 6.5. Automatically set when exiting Low Power Mode.
LPM Enable	7	rd/w/s/c	0b	When enabled the PLL start-up time is shortened to allow fast start-up for LPM. The reduced PLL start-up time is achieved by bypassing the VCO process compensation which was done on initial start-up.

7.1.1.6 Interface Control

Address = 07-09h (read), 07h (write), 08h (set), 09h (clear)

Field Name	Bit	Access	Default	Description
6-pin FsLsSerialMode	0	rd/w/s/c	0b	When asserted the ULPI interface is redefined to the 6-pin Serial Mode. The PHY will automatically clear this bit when exiting serial mode.
3-pin FsLsSerialMode	1	rd/w/s/c	0b	When asserted the ULPI interface is redefined to the 3-pin Serial Mode. The PHY will automatically clear this bit when exiting serial mode.
CarkitMode	2	rd/w/s/c	0b	When asserted the ULPI interface is redefined to the Carkit interface. The PHY will automatically clear this bit when exiting Carkit Mode.
ClockSuspendM	3	rd/w/s/c	0b	Enables Link to turn on 60 MHz CLKOUT in Serial Mode or Carkit Mode. 0b: Disable clock in Serial or Carkit Mode. 1b: Enable clock in Serial or Carkit Mode.
AutoResume	4	rd/w/s/c	0b	Only applicable in host mode. Enables the PHY to automatically transmit resume signaling. This function is detailed in Section 6.4.1.4.
IndicatorComplement	5	rd/w/s/c	0b	Inverts the EXTVBUS signal. This function is detailed in Section 5.6.2. **Note:** The EXTVBUS signal is always high on the USB83340.
IndicatorPassThru	6	rd/w/s/c	0b	Disables AND'ing the internal VBUS comparator with the EXTVBUS signal when asserted. This function is detailed in Section 5.6.2. **Note:** The EXTVBUS signal is always high on the USB83340.
InterfaceProtectDisable	7	rd/w/s/c	0b	Used to disable the integrated **STP** pull-up resistor used for interface protection. This function is detailed in Section 6.5.4.

7.1.1.7 OTG Control

Address = 0A-0Ch (read), 0Ah (write), 0Bh (set), 0Ch (clear)

Field Name	Bit	Access	Default	Description
IdPullup	0	rd/w/s/c	0b	Connects a 100 kΩ pull-up resistor from the **ID** pin to **VDD33** 0b: Disables the pull-up resistor 1b: Enables the pull-up resistor
DpPulldown	1	rd/w/s/c	1b	Enables the 15 kΩ pull-down resistor on **DP**. 0b: Pull-down resistor not connected 1b: Pull-down resistor connected
DmPulldown	2	rd/w/s/c	1b	Enables the 15 kΩ pull-down resistor on **DM**. 0b: Pull-down resistor not connected 1b: Pull-down resistor connected
DischrgVbus	3	rd/w/s/c	0b	This bit is only used during SRP. Connects a resistor from VBUS to ground to discharge **VBUS**. 0b: Disconnects resistor from **VBUS** to ground 1b: Connects resistor from **VBUS** to ground
ChrgVbus	4	rd/w/s/c	0b	This bit is only used during SRP. Connects a resistor from **VBUS** to **VDD33** to charge **VBUS** above the SessValid threshold. 0b: Disconnects resistor from **VBUS** to **VDD33** 1b: Connects resistor from **VBUS** to **VDD33**
DrvVbus	5	rd/w/s/c	0b	Enables external 5 V supply to drive 5 V on VBUS. This signal is or'ed with *DrvVbusExternal*. 0b: Do not drive Vbus, **CPEN** driven low. 1b: Drive Vbus, **CPEN** driven high.
DrvVbusExternal	6	rd/w/s/c	0b	Enables external 5 V supply to drive 5 V on VBUS. This signal is or'ed with *DrvVbus*. 0b: Do not drive Vbus, **CPEN** driven low. 1b: Drive Vbus, **CPEN** driven high..
UseExternalVbus Indicator	7	rd/w/s/c	0b	Tells the PHY to use an external VBUS over-current or voltage indicator. This function is detailed in Section 5.6.2. 0b: Use the internal VbusValid comparator 1b: Use the EXTVBUS input as for VbusValid signal. **Note:** The EXTVBUS signal is always high on the USB83340.

7.1.1.8 USB Interrupt Enable Rising

Address = 0D-0Fh (read), 0Dh (write), 0Eh (set), 0Fh (clear)

Field Name	Bit	Access	Default	Description
HostDisconnect Rise	0	rd/w/s/c	1b	Generate an interrupt event notification when HostDisconnect changes from low to high. Applicable only in host mode.
VbusValid Rise	1	rd/w/s/c	1b	Generate an interrupt event notification when VbusValid changes from low to high.
SessValid Rise	2	rd/w/s/c	1b	Generate an interrupt event notification when SessValid changes from low to high.
SessEnd Rise	3	rd/w/s/c	1b	Generate an interrupt event notification when SessEnd changes from low to high.
IdGnd Rise	4	rd/w/s/c	1b	Generate an interrupt event notification when IdGnd changes from low to high.
Reserved	7:5	rd	0h	Read only, 0.

7.1.1.9 USB Interrupt Enable Falling

Address = 10-12h (read), 10h (write), 11h (set), 12h (clear)

Field Name	Bit	Access	Default	Description
HostDisconnect Fall	0	rd/w/s/c	1b	Generate an interrupt event notification when HostDisconnect changes from high to low. Applicable only in host mode.
VbusValid Fall	1	rd/w/s/c	1b	Generate an interrupt event notification when VbusValid changes from high to low.
SessValid Fall	2	rd/w/s/c	1b	Generate an interrupt event notification when SessValid changes from high to low.
SessEnd Fall	3	rd/w/s/c	1b	Generate an interrupt event notification when SessEnd changes from high to low.
IdGnd Fall	4	rd/w/s/c	1b	Generate an interrupt event notification when IdGnd changes from high to low.
Reserved	7:5	rd	0h	Read only, 0.

7.1.1.10 USB Interrupt Status

Address = 13h (read only)

This register dynamically updates to reflect current status of interrupt sources.

Field Name	Bit	Access	Default	Description
HostDisconnect	0	rd (read only)	0b	Current value of the UTMI+ HS HostDisconnect output. Applicable only in host mode.
VbusValid	1		0b	Current value of the UTMI+ VbusValid output. If *VbusValid Rise* and *VbusValid Fall* are set this register will read 0.
SessValid	2		0b	Current value of the UTMI+ SessValid output. This register will always read the current status of the Session Valid comparator regardless of the *SessValid Rise* and *SessValid Fall* settings.
SessEnd	3		0b	Current value of the UTMI+ SessEnd output. If *SessEnd Rise* and *SessEnd Fall* are set this register will read 0.
IdGnd	4		0b	Current value of the UTMI+ IdGnd output.
Reserved	7:5		0h	Read only, 0.

2: The default value is only valid after POR. When the register is read it will match the current status of the comparators at the moment the register is read.

7.1.1.11 USB Interrupt Latch

Address = 14h (read only with auto clear)

Field Name	Bit	Access	Default	Description
HostDisconnect Latch	0	rd (Note 3)	0b	Set to 1b by the PHY when an unmasked event occurs on HostDisconnect. Cleared when this register is read. Applicable only in host mode.
VbusValid Latch	1		0b	Set to 1b by the PHY when an unmasked event occurs on VbusValid. Cleared when this register is read.
SessValid Latch	2		0b	Set to 1b by the PHY when an unmasked event occurs on SessValid. Cleared when this register is read.
SessEnd Latch	3		0b	Set to 1b by the PHY when an unmasked event occurs on SessEnd. Cleared when this register is read.
IdGnd Latch	4		0b	Set to 1b by the PHY when an unmasked event occurs on IdGnd. Cleared when this register is read.
Reserved	7:5	rd	0h	Read only, 0.

3: rd: Read only with auto clear.

7.1.1.12 Debug

Address = 15h (read only)

Field Name	Bit	Access	Default	Description
Linestate[1:0]	1:0	rd	00b	Contains the current value of Linestate[1:0].
Reserved	7:2	rd	000000b	Read only, 0.

7.1.1.13 Scratch Register

Address = 16-18h (read), 16h (write), 17h (set), 18h (clear)

Field Name	Bit	Access	Default	Description
Scratch	7:0	rd/w/s/c	00h	Empty register byte for testing purposes. Software can read, write, set, and clear this register and the PHY functionality will not be affected.

7.1.2 CARKIT CONTROL REGISTERS

The following registers are used to set-up and enable the USB UART and USB Audio functions.

7.1.2.1 Carkit Control

Address = 19-1Bh (read), 19h (write), 1Ah (set), 1Bh (clear)

This register is used to program the USB83340 into and out of the Carkit Mode. When entering the UART Mode the Link must first set the desired *TxdEn* and the *RxdEn* bits and then transition to Carkit Mode by setting the *CarkitMode* bit in the Interface Control register. When *RxdEn* is not set then the **DATA[1]** pin is held to a logic high.

Field Name	Bit	Access	Default	Description
CarkitPwr	0	rd	0b	Read only, 0.
IdGndDrv	1	rd/w/s/c	0b	Drives **ID** pin to ground
TxdEn	2	rd/w/s/c	0b	Connects UART TXD (**DATA[0]**) to **DM**
RxdEn	3	rd/w/s/c	0b	Connects UART RXD (**DATA[1]**) to **DP**
SpkLeftEn	4	rd/w/s/c	0b	Connects **DM** pin to **SPK_L** pin
SpkRightEn	5	rd/w/s/c	0b	Connects **DP** pin to **SPK_R** pin. See Note 4 below.
MicEn	6	rd/w/s/c	0b	Connects **DP** pin to **SPK_R** pin. See Note 4 below.
CarkitDataMC	7	rd/w/s/c	0b	When set the UPLI DATA[2] pin is changed from a driven 0 to tri-state, when Carkit Mode is entered.

4: If *SpkRightEn* or *MicEn* are asserted the **DP** pin will be connected to **SPK_R**. To disconnect the **DP** pin from the **SPK_R** pin both *SpkrRightEn* and *MicEn* must be set to de-asserted.

If using USB UART Mode, the UART data will appear at the **SPK_L** and **SPK_R** pins if the corresponding *SpkLeftEn*, *SpkRightEn*, or *MicEn* switches are enabled.

If using USB Audio the *TxdEn* and *RxdEn* bits should not be set when the *SpkLeftEn*, *SpkRightEn*, or *MicEn* switches are enabled. The USB single-ended receivers described in Section 5.2.1 are disabled when either *SpkLeftEn*, *SpkRightEn*, or *MicEn* are set.

7.1.2.2 Carkit Interrupt Enable

Address = 1D-1Fh (read), 1Dh (write), 1Eh (set), 1Fh (clear)

Field Name	Bit	Access	Default	Description
IdFloatRise	0	rd/w/s/c	0b	When enabled an interrupt will be generated on the alt_int of the RX CMD byte when the **ID** pin transitions from non-floating to floating. The *IdPullup* bit in the OTG Control register should be set.
IdFloatFall	1	rd/w/s/c	0b	When enabled an interrupt will be generated on the alt_int of the RX CMD byte when the **ID** pin transitions from floating to non-floating. The *IdPullup* bit in the OTG Control register should be set.
VdatDetIntEn	2	rd/w/s/c	0b	When enabled an interrupt will be generated on the alt_int of the RX CMD byte when the V_{DAT_DET} comparator changes state.
CarDpRise	3	rd	0b	Not implemented. Reads as 0b.
CarDpFall	4	rd	0b	Not implemented. Reads as 0b.
RidIntEn	5	rd/w/s/c	0b	When enabled an interrupt will be generated on the alt_int of the RX CMD byte when *RidConversionDone* bit is asserted. **Note:** This register bit is OR'ed with the *RidIntEn* bit of the Vendor R_{ID} Conversion register.
Reserved	6	rd/w/s/c	0b	Read only, 0.
Reserved	7	rd	0b	Read only, 0.

7.1.2.3 Carkit Interrupt Status

Address = 20h (read only)

Field Name	Bit	Access	Default	Description
IdFloat	0	rd	0b	Asserted when the **ID** pin is floating. *IdPullup* must be enabled.
VdatDet	1	rd	0b	V_{DAT_DET} comparator output 0b: No voltage is detected on **DP**. 1b: Voltage detected on **DP**, *IdatSinkEn* must be set to 1. **Note:** *VdatDet* can also be read from the USB-IF Charger Detection.
CarDp	2	rd	0b	Not implemented. Reads as 0b.
RidValue	5:3	rd	000b	Conversion value of R_{ID} resistor 000: 0 Ω 001: 75 Ω 010: 102 kΩ 011: 200 kΩ 100: 440 kΩ 101: ID floating 111: Error **Note:** *RidValue* can also be read from the Vendor R_{ID} Conversion register.
RidConversionDone	6	rd	0b	Automatically asserted by the USB83340 when the R_{ID} conversion is finished. The conversion will take 282 µs. This bit will auto clear when the *RidValue* is read from the Vendor R_{ID} Conversion register. Reading the *RidValue* from the Carkit Interrupt Status register will not clear either *RidConversionDone* status bit. **Note:** *RidConversionDone* can also be read from the Vendor R_{ID} Conversion register.
Reserved	7	rd	0b	Read only, 0.

7.1.2.4 Carkit Interrupt Latch

Address = 21h (read only with auto-clear)

Field Name	Bit	Access	Default	Description
IdFloat Latch	0	rd (Note 5)	0b	Asserted if the state of the **ID** pin changes from non-floating to floating while the *IdFloatRise* bit is enabled or if the state of the **ID** pin changes from floating to non-floating while the *IdFloatFall* bit is enabled.
VdatDet Latch	1	rd	0b	If *VdatDetIntEn* is set and the *VdatDet* bit changes state, this bit will be asserted.
CarDp Latch	2	rd	0b	Not implemented. Reads as 0b.
RidConversionLatch	3	rd (Note 5)	0b	If *RidIntEn* is set and the state of the *RidConversion-Done* bit changes from a 0 to 1 this bit will be asserted.
Reserved	7:4	rd	0000b	Read only, 0.

5: rd: Read only with auto clear

7.1.3 VENDOR REGISTER ACCESS

The vendor specific registers include the range from 30h to 3Fh. These can be accessed by the ULPI immediate register read / write.

7.1.3.1 HS Compensation and LPM Register

Address = 31h (read / write)

The USB83340 is designed to meet the USB specifications and requirements when the DP and DM signals are properly designed on the PCB. The DP and DM trace impedance should be 45 Ω single-ended and 90 Ω differential. In cases where the DP and DM traces are not able to meet these requirements the HS Compensation register can be used to compensate for the losses in signal amplitude.

Field Name	Bit	Access	Default	Description
VariSense	1:0	rd/w	00b	Used to lower the threshold of the squelch detector. 00: 100% (default) 01: 83% 10: 66.7% 11: 50%
Reserved	2	rd	0b	Read only, 0.
Reserved	3	rd	0b	Read only, 0.
PHYBoost	6:4	rd/w	000b	Used to change the output voltage of the high-speed transmitter 000: Nominal 001: +3.7% 010: +7.4% 011: +11.0% 100: +14.7% 101: +18.3% 110: +22.0% 111: +25.7%
Reserved	7	rd	0b	Read only, 0.

7.1.3.2 USB-IF Charger Detection

Address = 32h (read / write)

Field Name	Bit	Access	Default	Description
VDatSrcEn	0	rd/w	0	V_{DAT_SRC} voltage enable 0b: Disabled 1b: Enabled
IDatSinkEn	1	rd/w	0	I_{DAT_SINK} current sink and V_{DAT_DET} comparator enable 0b: Disabled, V_{DAT_DET} = 0. 1b: Enabled
ContactDetectEn	2	rd/w	0	I_{DP_SRC} enable 0b: Disabled 1b: Enabled
HostChrgEn	3	rd/w	0	Enable Charging Host Port Mode. 0b: Portable device 1b: Charging Host Port. When the charging host port bit is set the connections of V_{DAT_SRC}, I_{DAT_SINK}, I_{DP_SRC}, and V_{DAT_DET} are reversed between **DP** and **DM**.
VdatDet	4	rd	0	V_{DAT_DET} comparator output. *IdatSinkEn* must be set to 1 to enable the comparator. 0b: No voltage is detected on **DP** or *Linestate[1:0]* is not equal to 00b. 1b: Voltage detected on **DP**, and *Linestate[1:0]* = 00b. **Note:** *VdatDet* can also be read from the Carkit Interrupt Status register.
Reserved	5-7	rd		Read only, 0.

Note: The charger detection should be turned off before beginning USB operation. USB-IF Charger Detection bits 2:0 should be set to 000b.

7.1.3.3 Headset Audio Mode

Address = 33h (read / write)

Field Name	Bit	Access	Default	Description
HeadsetAudioEn	3:0	rd/w	0000b	When this field is set to a value of '1010', the Headset Audio Mode is enabled as described in Section 6.8.1.
Reserved	7:4	rd	0h	Read only, 0.

7.1.3.4 Vendor R_{ID} Conversion

Address = 36-38h (read), 36h (write), 37h (set), 38h (clear)

Field Name	Bit	Access	Default	Description
RidValue	2:0	rd/w	000b	Conversion value of R_{ID} resistor 000: 0 Ω 001: 75 Ω 010: 100 kΩ 011: 200 kΩ 100: 440 kΩ 101: ID floating 111: Error **Note:** *RidValue* can also be read from the Carkit Interrupt Status register.
RidConversionDone	3	rd (Note 6)	0b	Automatically asserted by the USB83340 when the R_{ID} conversion is finished. The conversion will take 282 µs. This bit will auto clear when the *RidValue* is read from the R_{ID} Conversion register. Reading the *RidValue* from the Carkit Interrupt Status register will not clear either *RidConversionDone* status bit. **Note:** *RidConversionDone* can also be read from the Carkit Interrupt Status register.
RidConversionStart	4	rd/w/s/c	0b	When this bit is asserted either through a register write or set, the R_{ID} converter will read the value of the ID resistor. When the conversion is complete this bit will auto clear.
Reserved	5	rd/w/s/c	0b	This bit must remain at 0.
RidIntEn	6	rd/w/s/c	0b	When enabled an interrupt will be generated on the alt_int of the RX CMD byte when *RidConversionDone* bit is asserted. **Note:** This register bit is OR'ed with the *RidIntEn* bit of the Carkit Interrupt Status register.
Reserved	7	rd	0b	Read only, 0.

6: rd: Read only with auto clear.

7.1.3.5 USB IO & Power Management

Address = 39-3Bh (read), 39h (write), 3Ah (set), 3Bh (clear)

Field Name	Bit	Access	Default	Description
Reserved	0	rd/w/s/c	0b	Read only, 0.
SwapDP/DM	1	rd/w/s/c	0b	When asserted, the **DP** and **DM** pins of the USB PHY are swapped. This bit can be used to prevent crossing the DP/DM traces on the board. In UART Mode, it swaps the routing to the **DP** and **DM** pins. In USB Audio Mode, it does not affect the **SPK_L** and **SPK_R** pins.
UART RegOutput	3:2	rd/w/s/c	01b	Controls the output voltage of the **VBAT** to **VDD33** regulator in UART Mode. When the PHY is switched from USB Mode to UART Mode regulator output will automatically change to the value specified in this register when *TxdEn* is asserted. 00: 3.3 V 01: 3.0 V (default) 10: 2.75 V 11: 2.5 V **Note:** When in USB Audio Mode the regulator will remain at 3.3 V. When using this register it is recommended that the Link exit UART Mode by using the **RESETB** pin.
ChargerPullupEnDP	4	rd/w/s/c	0b	Enables the R_{CD} pull-up resistor on the **DP** pin. (The pull-up is automatically enabled in UART Mode)
ChargerPullupEnDM	5	rd/w/s/c	0b	Enables the R_{CD} pull-up resistor on the **DM** pin. (The pull-up is automatically enabled in UART Mode)
USB RegOutput	7:6	rd/w/s/c	00b	Controls the output voltage of the **VBAT** to **VDD33** regulator in USB Mode. When the PHY is in Synchronous Mode, Serial Mode, or Low Power Mode, the regulator output will be the value specified in this register. 00: 3.3 V (default) 01: 3.0 V 10: 2.75 V 11: 2.5 V For USB compliance this register must be set to the default value.

8.0 APPLICATION NOTES

8.1 Application Diagram

The USB83340 requires few external components as shown in the application diagrams. The USB 2.0 specification restricts the voltage at the VBUS pin to a maximum value of 5.25 V. In some applications, the voltage will exceed this limit, so the USB83340 provides an integrated over-voltage protection circuit. The over-voltage protection circuit works with an external resistor (R_{VBUS}) to lower the voltage at the **VBUS** pin.

TABLE 8-1: COMPONENT VALUES IN APPLICATION DIAGRAMS

Reference Designator	Value	Description	Notes
C_{OUT}	See Table 4-7	Bypass capacitor to ground (< 1 Ω ESR) for regulator stability.	Place as close as possible to the PHY.
C_{VBUS}	See Table 8-2	Capacitor to ground required by the USB specification. Microchip recommends < 1 Ω ESR.	Place near the USB connector.
C_{BYP}	System dependent	Bypass capacitor to ground. Typical values used are 0.1 or 0.01 µF.	Place as close as possible to the PHY.
C_{DC_LOAD}	System dependent	The USB connector housing may be AC-coupled to the device ground.	Industry convention is to ground only the host side of the cable shield.
R_{VBUS}	1 kΩ or 20 kΩ	Series resistor to work with internal over-voltage protection.	See Section 5.6.2.6 for information regarding power dissipation.
R_{BIAS}	8.06 kΩ (±1%)	Series resistor to establish reference voltage.	See Section 5.3 for information regarding power dissipation.

TABLE 8-2: CAPACITANCE VALUES AT VBUS OF USB CONNECTOR

MODE	MIN VALUE	MAX VALUE
Host	120 µF	
Device	1 µF	10 µF
OTG	1 µF	6.5 µF

FIGURE 8-1: USB83340 APPLICATION DIAGRAM (DEVICE, ULPI OUTPUT CLOCK MODE, 24 MHz)

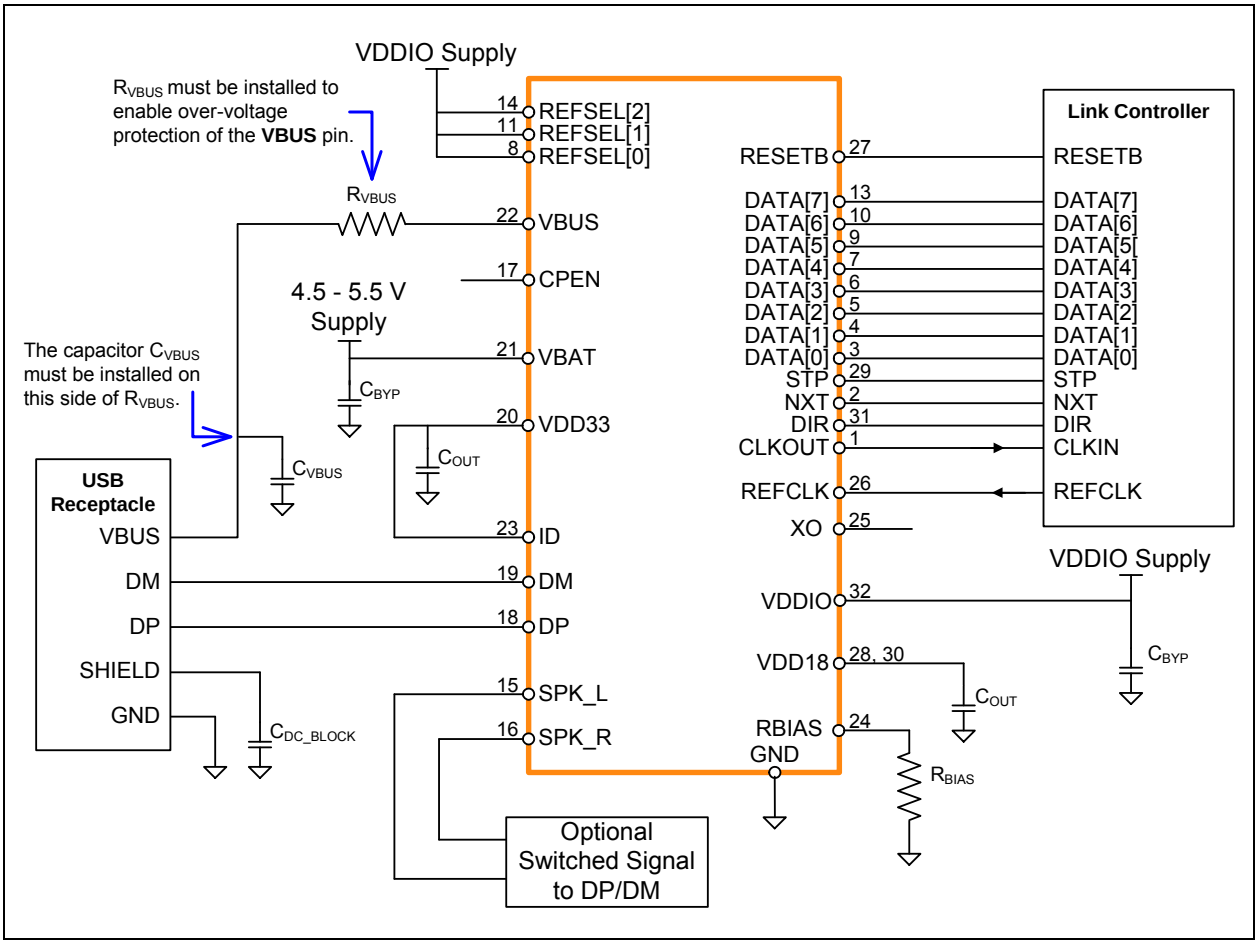


FIGURE 8-2: USB83340 APPLICATION DIAGRAM (DEVICE, ULPI INPUT CLOCK MODE, 60 MHz)

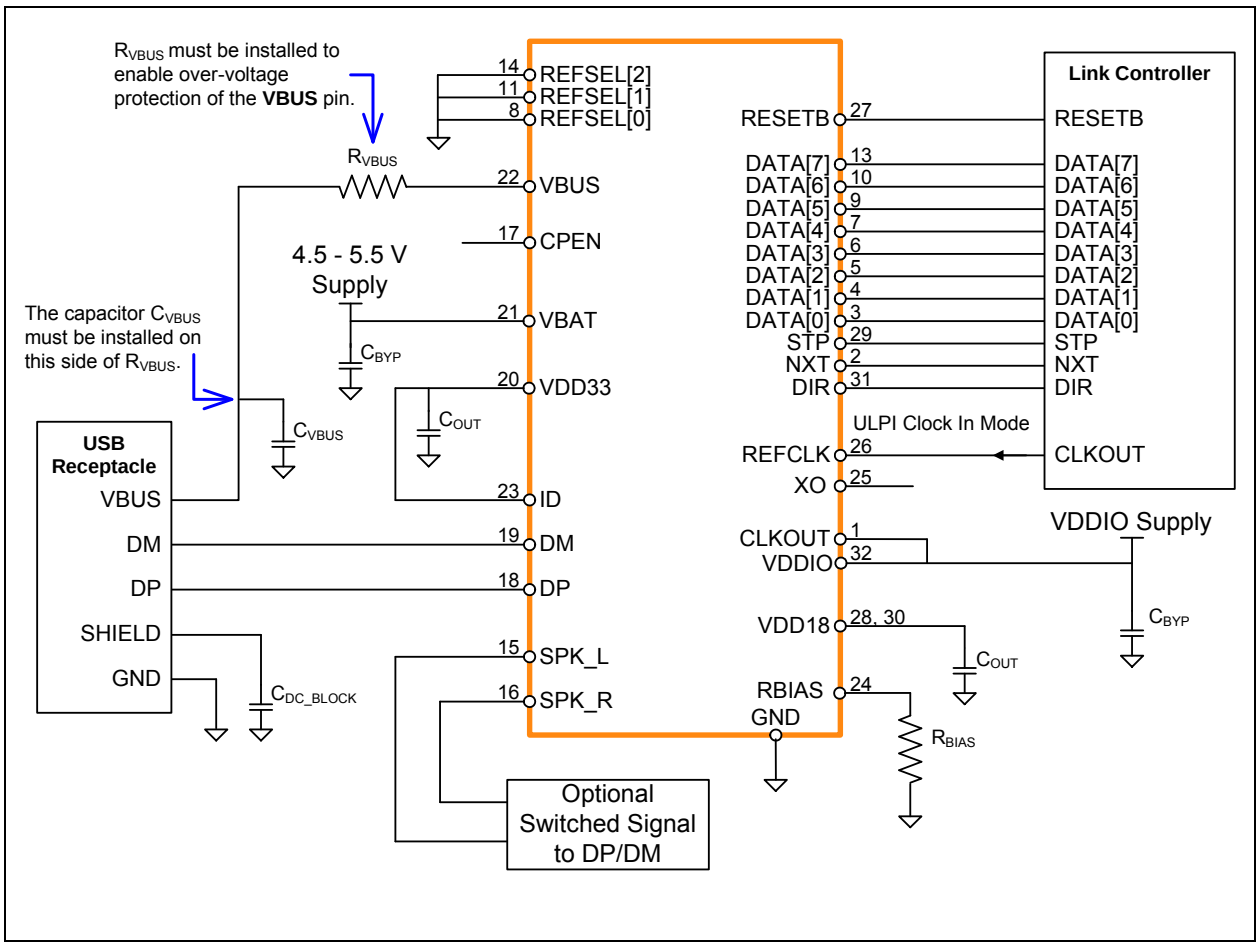
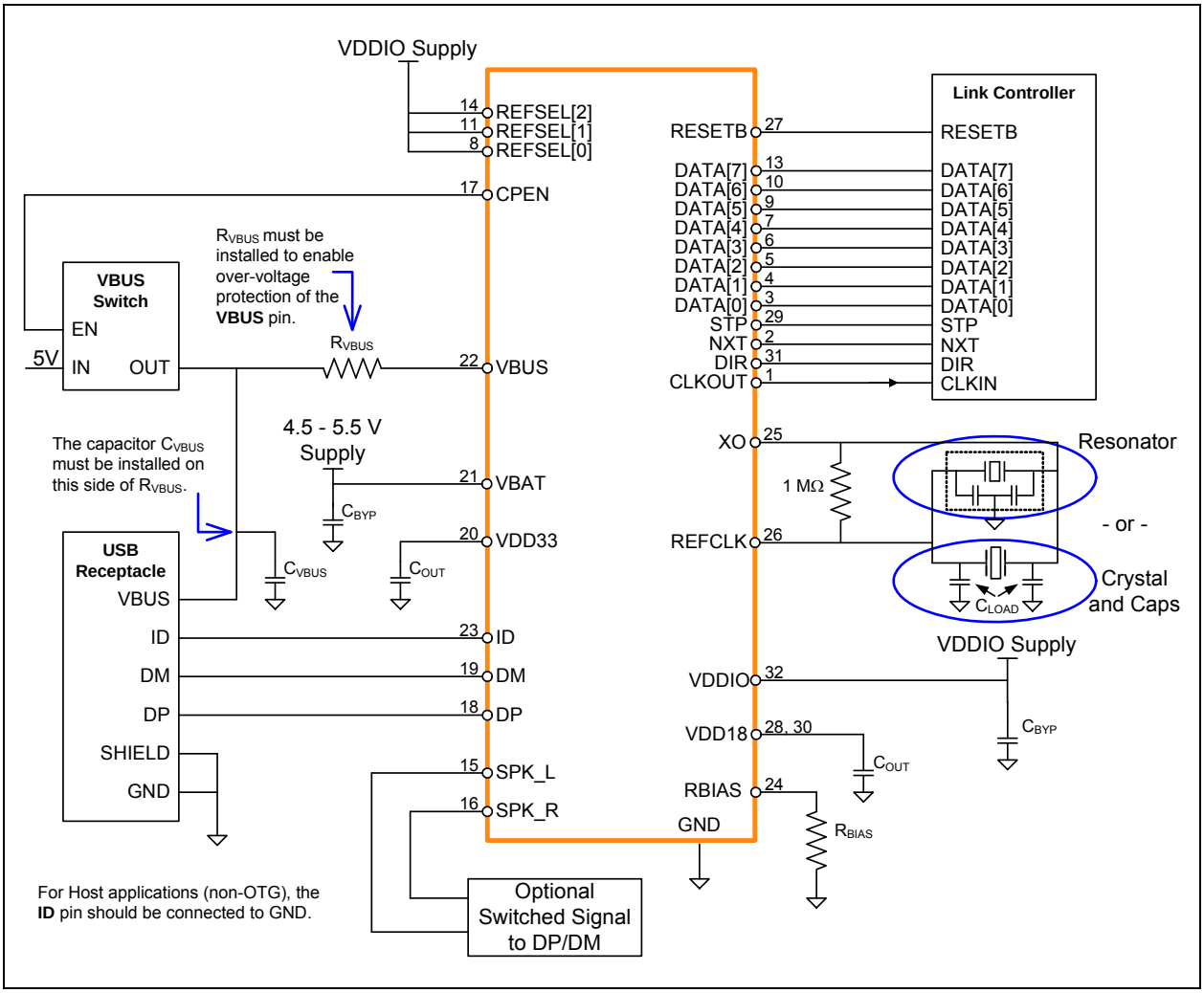


FIGURE 8-3: USB83340 APPLICATION DIAGRAM (HOST OR OTG, ULPI OUTPUT CLOCK MODE, 24 MHz)



8.2 USB Charger Detection

The USB83340 provides the hardware described in the USB Battery Charging Specification. Microchip provides an Application Note which describes how to use the USB83340 in a battery charging application.

8.3 Reference Designs

Microchip has generated reference designs for connecting the USB83340 to SoCs with a ULPI port. Please contact the Microchip sales office for more details.

8.4 ESD Performance

The USB83340 is protected from ESD strikes. By eliminating the requirement for external ESD protection devices, board space is conserved, and the board manufacturer is enabled to reduce cost. The advanced ESD structures integrated into the USB83340 protect the device whether or not it is powered up.

8.4.1 AIR DISCHARGE

To perform this test, a charged electrode is moved close to the system being tested until a spark is generated. This test is difficult to reproduce because the discharge is influenced by such factors as humidity, the speed of approach of the electrode, and construction of the test equipment.

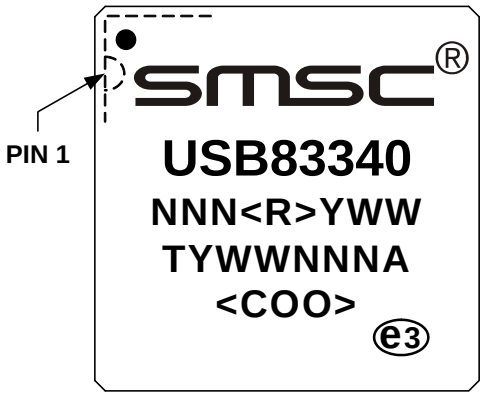
8.4.2 CONTACT DISCHARGE

The uncharged electrode first contacts the USB connector to prepare this test, and then the probe tip is energized. This yields more repeatable results, and is the preferred test method. The independent test laboratories contracted by Microchip provide test results for both types of discharge methods.

9.0 PACKAGE INFORMATION

9.1 Package Marking Information

32-QFN (5x5 mm)



Legend:	USB83340	Product
	NNN<R>YWW	Internal Code + Prod Rev + Date Code
	TYWWNNNA	Trace Code
	<COO>	Country of Origin
	e3	Pb free Symbol

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

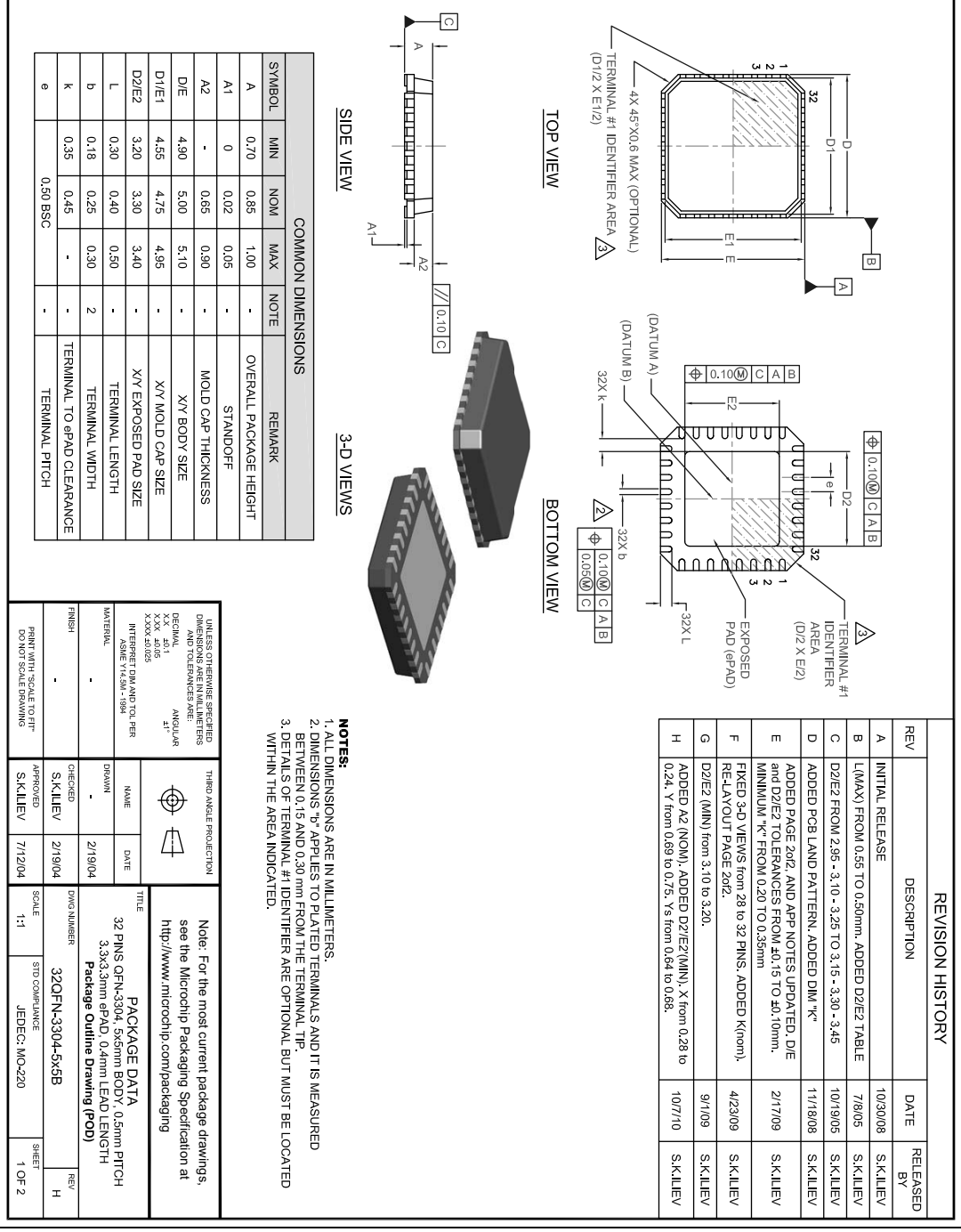
* Standard device marking consists of Microchip part number, year code, week code and traceability code. For device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

9.2 Package Drawings

Note: For the most current package drawings, see the Microchip Packaging Specification at: http://www.microchip.com/packaging.

The USB83340 is offered in a compact 32-pin QFN package.

FIGURE 9-1: 32-PIN QFN PACKAGE



REVISION HISTORY

REV	DESCRIPTION	DATE	RELEASED BY
A	INITIAL RELEASE	10/30/08	S.K.ILIEV
B	L(MAX) FROM 0.55 TO 0.50mm. ADDED D2/E2 TABLE	7/6/05	S.K.ILIEV
C	D2/E2 FROM 2.95 - 3.10 - 3.25 TO 3.15 - 3.30 - 3.45	10/19/05	S.K.ILIEV
D	ADDED PCB LAND PATTERN. ADDED DIM "K"	11/18/08	S.K.ILIEV
E	ADDED PAGE 2of2 AND APP NOTES UPDATED. D/E and D2/E2 TOLERANCES FROM ±0.15 TO ±0.10mm. MINIMUM "K" FROM 0.20 TO 0.35mm	2/17/09	S.K.ILIEV
F	FIXED 3-D VIEWS from 28 to 32 PINS. ADDED K(nom). RE-LAYOUT PAGE 2of2.	4/23/09	S.K.ILIEV
G	D2/E2 (MIN) from 3.10 to 3.20.	9/1/09	S.K.ILIEV
H	ADDED A2 (NOM). ADDED D2'/E2'(MIN). X from 0.28 to 0.24. Y from 0.69 to 0.75. Ys from 0.64 to 0.68.	10/7/10	S.K.ILIEV

COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.70	0.85	1.00	-	OVERALL PACKAGE HEIGHT
A1	0	0.02	0.05	-	STANDOFF
A2	-	0.65	0.90	-	MOLD CAP THICKNESS
D/E	4.90	5.00	5.10	-	X/Y BODY SIZE
D1/E1	4.55	4.75	4.95	-	X/Y MOLD CAP SIZE
D2/E2	3.20	3.30	3.40	-	X/Y EXPOSED PAD SIZE
L	0.30	0.40	0.50	-	TERMINAL LENGTH
b	0.18	0.25	0.30	2	TERMINAL WIDTH
k	0.35	0.45	-	-	TERMINAL TO ePAD CLEARANCE
e	0.50 BSC			-	TERMINAL PITCH

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS AND TOLERANCES ARE:
DECIMAL X.X ±0.1, X.XX ±0.05, X.XXX ±0.025
ANGULAR ±1°
INTERPRET DIM AND TOL PER ASME Y14.5M - 1994
MATERIAL: -
FINISH: -
PRINT WITH "SCALE TO FIT" DO NOT SCALE DRAWING

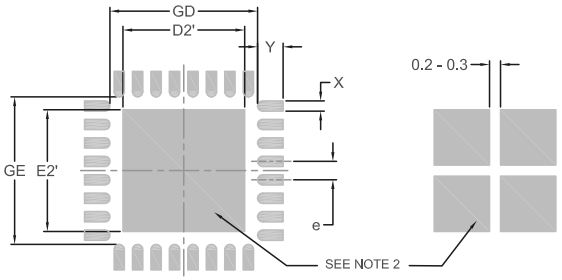
THIRD ANGLE PROJECTION

	NAME	DATE
DRAWN	-	2/19/04
CHECKED	S.K.ILIEV	2/19/04
APPROVED	S.K.ILIEV	7/12/04

Note: For the most current package drawings, see the Microchip Packaging Specification at http://www.microchip.com/packaging

TITLE: PACKAGE DATA
32 PINS QFN-3304 , 5x5mm BODY, 0.5mm PITCH
3.3x3.3mm ePAD, 0.4mm LEAD LENGTH
Package Outline Drawing (POD)

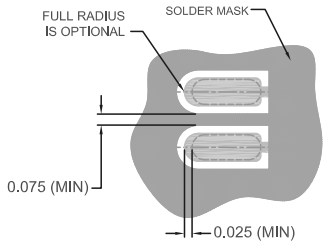
DWG NUMBER: 32QFN-3304-5x5B
REV: H
SCALE: 1:1
STD COMPLIANCE: JEDEC: MO-220
SHEET: 1 OF 2



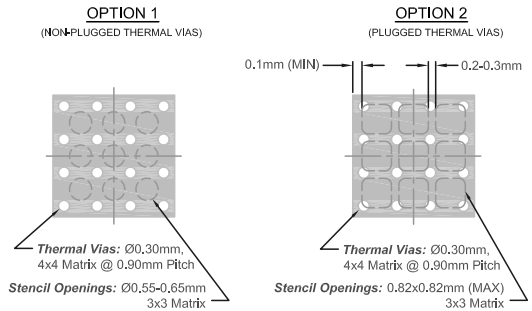
LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	4.00	-	4.10
D2'/E2'	3.10	-	3.30
X	-	0.24	0.28
Y	-	0.69	0.75
e		0.50	

NOTES:
1. THE USER MAY MODIFY THE PCB LAND PATTERN DESIGN AND DIMENSIONS BASED ON THEIR EXPERIENCE AND/OR PROCESS CAPABILITY
2. EXPOSED SOLDERABLE COPPER AREA OF THE CENTER PAD CAN BE EITHER SOLID OR SEGMENTED
3. MAXIMUM THERMAL AND ELECTRICAL PACKAGE PERFORMANCE IS ACHIEVED WHEN AN ARRAY OF SOLID VIAS IS INCORPORATED IN THE CENTER LAND PATTERN

PCB LAND PATTERN

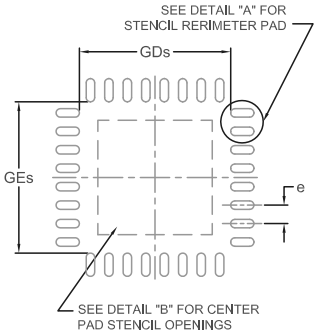


DETAIL "A" - STENCIL OPENING for PERIMETER LANDS



DETAIL "B"

THERMAL VIAS and STENCIL OPENING - CENTER PAD



STENCIL DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GDs/GEs	4.05	-	-
Xs	-	0.23	0.25
Ys	-	0.62	0.68
e		0.50	

STENCIL

SMT APPLICATION NOTES

1. THE USER MAY MODIFY THE PCB LAND PATTERN DIMENSIONS BASED ON THEIR EXPERIENCE AND/OR PROCESS CAPABILITY.
2. THE LAND PATTERN CORRESPONDING TO THE PACKAGE EXPOSED PAD (IN THE CENTER) CAN BE LARGER, AND WITH DIFFERENT SHAPE THAN THE EXPOSED PAD ON THE PACKAGE. HOWEVER, THE SOLDERABLE AREA, AS DEFINED BY THE SOLDER MASK (SMD), OR NON-SOLDER MASK DEFINED (NSMD), SHOULD BE AS SHOWN FOR THE BEST THERMAL & ELECTRICAL PERFORMANCE.
3. MAXIMUM THERMAL AND ELECTRICAL PERFORMANCE IS ACHIEVED WHEN AN ARRAY OF SOLID VIAS IS INCORPORATED IN THE CENTER LAND PATTERN (See Options 1 & 2).
4. THE VIAS SHOULD BE AT 0.8 to 1.2MM PITCH WITH 0.30 TO 0.40MM DIAMETER, AND 1 OZ COPPER VIA BARREL PLATING.
5. NON SOLDER MASK DEFINED (NSMD) PAD DESIGN IS RECOMMENDED FOR PERIMETER LANDS.
6. A LASER-CUT STAINLESS STEEL STENCIL IS RECOMMENDED WITH ELECTRO POLISHED TRAPEZOIDAL WALLS. THE RECOMMENDED STENCIL THICKNESS IS 0.125 mm FOR PITCHES 0.4 and 0.5 mm.
7. RECOMMENDED STENCIL AREA & ASPECT RATIOS ARE 0.66 & 1.5 (MIN) RESPECTIVELY.
8. RECOMMENDED STENCIL APERTURES ARE AS SHOWN.
9. IT IS RECOMMENDED TO USE "NO-CLEAN", TYPE 3 SOLDER PASTE.
10. THE REFLOW PROFILE DEPENDS ON THE EXACT SOLDER PASTE USED AND THE GIVEN BOARD DETAILS, SUCH AS GEOMETRY, COMPONENTS ETC.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS AND TOLERANCES ARE: DECIMAL X.X ±0.1, X.XX ±0.05, X.XXX ±0.025 ANGULAR ±1° INTERPRET DIM AND TOL PER ASME Y14.5M - 1994	THIRD ANGLE PROJECTION		Note: For the most current package drawings, see the Microchip Packaging Specification at http://www.microchip.com/packaging
	NAME	DATE	TITLE: PACKAGE DATA 32 PINS QFN-3304, 5x5mm BODY, 0.5mm PITCH, 3.3x3.3mm EXPOSED PAD, 0.4mm LEAD LENGTH **Application Notes**
MATERIAL: -	DRAWN: -	2/17/09	
FINISH: -	CHECKED: -	2/17/09	DWG NUMBER: 32QFN-3304-5x5B; REV: H
PRINT WITH "SCALE TO FIT" DO NOT SCALE DRAWING	APPROVED: S.K.ILIEV	2/17/09	SCALE: 1:1; STD COMPLIANCE: JEDEC: MO-220; SHEET: 2 OF 2

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE 9-1: CUSTOMER REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS60001311B	Section 2.0, "USB83340 Pin Locations and Definitions," on page 6	Pin 30 function changed from VDD18 to NC (No Connect).
	Section 9.0, "Package Information," on page 85	Package information adapted.
	Product Identification System	Adopted according to new system.
DS60001311A	All	Version migrated to Microchip template. Microchip DS number inserted. Revision A replaces the previous SMSC version 1.3. Trademark and last page according to Microchip guidelines.
	Cover Sheet	'AEC-Q100 compliance remark' replaces 'TrueAuto remark'. USB-IF Battery Charging 1.1 Specification -> USB-IF Battery Charging 1.2 Specification
	Section 4.9, "USB Charger Detection Characteristics," on page 14	USB-IF Battery Charging 1.1 Specification -> USB-IF Battery Charging 1.2 Specification
	Section 5.9, "USB Audio Support," on page 37	USB-IF Battery Charging 1.1 Specification -> USB-IF Battery Charging 1.2 Specification
	Section 7.1.3.1, "HS Compensation and LPM Register," on page 76	Field name: *VariSense:* 01: 83%I -> 01: 83%
	Section Appendix B:, "Acronyms," on page 91	Section 1.1 moved to Section Appendix B:, "Acronyms"
	Section Appendix C:, "References," on page 92	Web sites added.
Rev. 1.3 (07-31-13)	All	• Order numbers adapted • Lead-free information removed • Microchip logo and legend added.
	Table 4-7, "Regulator Output Voltages and Capacitor Requirement," on page 15	• Line "Regulator Bypass Capacitor C_{OUT33}": Max value changed from TBD to 10 µF. • Line "Regulator Bypass Capacitor C_{OUT18}": Max value changed from TBD to 10 µF.
	Table 4-8, "USB83340 Quartz Crystal Specifications," on page 16	• Line added for Crystal load capacitance.

TABLE 9-1: CUSTOMER REVISION HISTORY (CONTINUED)

Revision Level & Date	Section/Figure/Entry	Correction
Rev 1.3 (07-25-12)	Table 4.10, “Regulator Output Voltages and Capacitor Requirement,” on page 15	Table 4-7: Added min and max value for: • VDD33 5.5>VBAT>4.5 V • VDD18 3.6>VBAT>2.25 V
Rev 1.2 (10-26-11)	Section 2.1.2, "Pin Definitions"	Pin 1: CLKOUT tied to VDDIO.
		Pin 12: Added: Leave pin floating..
Rev 1.2 (10-26-11) cont.	Section 2.1.2, "Pin Definitions"	Pin 28: “Only one bypass capacitor is needed between both VDD18 pins.” replaced by “Pin 28 and Pin 30 must be tied together. Only one bypass capacitor is required between Pin 28 and Pin 30.”
		Pin 30: “Only one bypass capacitor is needed between both VDD18 pins.” replaced by “Pin 28 and Pin 30 must be tied together. Only one bypass capacitor is required between Pin 28 and Pin 30.”
		Pin 32: Removed: “This voltage sets the value of V_{OH} for the ULPI interface.”
	Section 5.4.1	Second paragraph: “If a connection to VDD18 is detected, ...” replaced by “If a connection to VDDIO is detected, ...”
	Section 5.4.1.1	Second sentence: “and the CLKOUT pin is tied high to VDD33.” replaced by “and the CLKOUT pin is tied high to VDDIO.” Figure 5-2: 2VDD33” replaced by “VDD18/VDDIO”.
	Section 5.4.2	Second sentence: “The REFCLK pin is designed to be driven with a square wave from 0 V to V_{DD18},...” replaced by “The **REFCLK** pin is designed to be driven with a square wave from 0 V to V_{DDIO},”
	Section 8.1	Figure 8-2: “VDD33 Supply” replaced by “VDDIO Supply”
Rev 1.2 (04-07-11)	Section 2.1.2, "Pin Definitions"	CLKOUT tied to VDD33
	Section 3.1, "Absolute Maximum Ratings"	Table 3-1: Description of note adapted.

TABLE 9-1: CUSTOMER REVISION HISTORY (CONTINUED)

Revision Level & Date	Section/Figure/Entry	Correction
Rev 1.2 (04-07-11) cont.	Chapter 4.0	Removed specification for USB Audio Mode (Table 4-1), T_{PREP_LPM} (Table 4-2), Input Rise Time and Input Fall Time (Table 4-4). Table 4-1: Characterization data corrected/added for: Synchronous Mode Current (Default configuration = FS configuration) • Synchronous Mode Current (HS USB operation) • Synchronous Mode Current (FS/LS USB operation) • Low Power Mode, $I_{VBAT(SUSPEND)}$, $I_{VIO(SUSPEND)}$, conditions added • RESET Mode Table 4-2: Characterization data corrected/added for: • CLKOUT Duty Cycle • REFCLK Duty Cycle Table 4-3: Characterization data corrected/added for: • Output Delay (control out, 8-bit data out) • Hold Time (STP, data in) Table 4-4: Characterization data corrected/added for: • Low-Level Input Voltage • High-Level Input Voltage • High-Level Output Voltage • Output Rise Time • Output Fall Time • STP Pull-up Resistance • DATA[7:0] Pull-down Resistance Table 4-5: Characterization data corrected/added for: • ID Ground Trip Point
Revision 1.1 (02-12-10)	Section 4.11, "Piezoelectric Resonator for Internal Oscillator"	New section added.
Revision 1.0 (02-02-10)	Initial document release	

APPENDIX B: ACRONYMS

The following is a list of the general terms used throughout this document:

TABLE 9-3: ACRONYMS

Acronym	Description
ASIC	Application-Specific Integrated Circuit
ECN	Engineering Chance Notice
EOP	End-of-Packet
ESD	Electro Static Discharge
ESR	Equivalent Series Resistance
FS	Full-Speed
HS	High-Speed
LPM	Link Power Management
LS	Low-Speed
NOPID	No Packet Identifier
NRZI	Non Return to Zero Invert
OTG	On-the-Go
OVP	Over-Voltage Protection
PCB	Printed Circuit Board
PHY	Physical Layer
PID	Packet Identifier
PLL	Phase-Locked Loop
POR	Power On Reset
SDR	Single Data Rate
SE0	Single-Ended Zero
SE1	Single-Ended One
SE RX	Single-Ended Receivers
SOF	Start of Frame
SRP	Session Request Protocol
ULPI	UTMI+ Low Pin Interface
UTMI	USB 2.0 Transceiver Macrocell Interface
UTMI+	UTMI extension supporting On-The-Go
VCO	Voltage Controlled Oscillator

APPENDIX C: REFERENCES

[1] Universal Serial Bus Specification, Version 2.0, April 27, 2000 (12/7/2000 and 5/28/2002 Errata)
http://www.usb.org

[2] UTMI+ Low Pin Interface (ULPI) Specification, Revision 1.1
http://www.ulpi.org/

[3] On-The-Go Supplement to the USB2.0 Specification, Revision 1.3
http://www.usb.org

[4] On-The-Go Supplement to the USB2.0 Specification, Revision 2.0
http://www.usb.org

[5] USB Battery Charging Specification, Revision 1.2
http://www.usb.org

THE MICROCHIP WEB SITE

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- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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- Technical Support

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Technical support is available through the web site at: http://microchip.com/support

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X]	X	[X](1)	-	X	- (2)	Vxx
Device	Temperature Range	Package	Tape and Reel Option		Pattern		Designator

Device:	USB83340	
Temperature Range:	A	= -40°C to +105°C
Package:	M	= QFN (32-pin)
Tape and Reel Option:	Blank R	= Standard packaging (tray) = Tape and Reel(1)
Pattern	B	= Product Version
Designator	Vxx	= Automotive Designator

Examples:

a) USB83340AMR-B-V02
-40°C to + 105°C,
QFN (32-pin),
Tape & Reel,
B,
V02

b) USB83340AM-B-V02
-40°C to + 105°C,
QFN (32-pin),
Tray,
B,
V02

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Note 2: "-" is optional. Check with your Microchip Sales Office for exact ordering part number.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

ISBN: 978-1-5224-1107-9

QUALITY MANAGEMENT SYSTEM
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Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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