Description

These devices are designed to limit overvoltages on the telephone line. Overvoltages are normally caused by a.c. power system or lightning flash disturbances which are induced or conducted on to the telephone line. A single device provides 2-point protection and is typically used for the protection of 2-wire telecommunication equipment (e.g. between the Ring and Tip wires for telephones and modems). Combinations of devices can be used for multi-point protection (e.g. 3-point protection between Ring, Tip and Ground).

The protector consists of a symmetrical voltage-triggered bidirectional thyristor. Overvoltages are initially clipped by breakdown clamping until the voltage rises to the breakover level, which causes the device to crowbar into a low-voltage on state. This low-voltage on state causes the current resulting from the overvoltage to be safely diverted through the device. The high crowbar holding current helps prevent d.c. latchup as the diverted current subsides.

The TISP4xxxL3 range consists of fifteen voltage variants to meet various maximum system voltage levels (58 V to 320 V). They are guaranteed to voltage limit and withstand the listed international lightning surges in both polarities. These protection devices are in an SMAJ (JEDEC DO-214AC with J-bend leads) plastic package. These devices are supplied in embossed tape reel carrier pack. For alternative voltage and holding current values, consult the factory. For higher rated impulse currents, the 50 A 10/1000 TISP4xxxM3AJ series in SMA and the 100 A 10/1000 TISP4xxxH3BJ series in SMB are available.

Absolute Maximum Ratings, T_A = 25 °C (Unless Otherwise Noted)

Rating		Symbol	Value	Unit
Repetitive peak off-state voltage, (see Note 1)	'4070	V_{DRM}	± 58	V
	'4080		± 65	
	'4090		± 70	
	'4125		± 100	
	'4145		± 120	
	'4165		± 135	
	'4180		± 145	
	'4220		± 160	
	'4240		± 180	
	'4260		± 200	
	'4290		± 230	
	'4320		± 240	
	'4350		± 275	
	'4360		± 290	
	'4395		± 320	
Non-repetitive peak on-state pulse current (see Notes 2, 3 and 4)		I_{TSP}		A
2/10 µs (GR-1089-CORE, 2/10 µs voltage wave shape)			125	
8/20 µs (IEC 61000-4-5,combination wave generator, 1.2/50 voltage, 8/20 current)			100	
10/160 µs (FCC Part 68, 10/160 µs voltage wave shape)			65	
5/310 µs (ITU-T K.20/21/45, K.44 10/700 µs voltage wave shape)			50	
5/310 µs (FTZ R12, 10/700 µs voltage wave shape)			50	
10/560 µs (FCC Part 68, 10/560 µs voltage wave shape)			40	
10/1000 µs (GR-1089-CORE, 10/1000 µs voltage wave shape)			30	
Non-repetitive peak on-state current (see Notes 2, 3 and 4)		I_{TSM}		A
20 ms (50 Hz) full sine wave			18	
1 s (50 Hz) full sine wave			7	
1000 s 50 Hz/60 Hz a.c.			1.6	
Junction temperature		T_J	-40 to +150	°C
Storage temperature range		T_{stg}	-65 to +150	°C

NOTES: 1. For voltage values at lower temperatures, derate at 0.13 %/°C.
2. Initially, the TISP4xxxL3 must be in thermal equilibrium with T_J = 25 °C
3. The surge may be repeated after the TISP4xxxL3 returns to its initial conditions.
4. EIA/JESD51-2 environment and EIA/JESD51-3 PCB with standard footprint dimensions connected with 5 A rated printed wiring track widths. Derate current values at -0.61 %/°C for ambient temperatures above 25 °C.

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Recommended Operating Conditions

Component		Min	Typ	Max	Unit
R_S	series resistor for FCC Part 68, 10/560 type A surge survival	12			Ω
	series resistor for FCC Part 68, 9/720 type B surge survival	0			Ω
	series resistor for GR-1089-CORE first-level and second-level surge survival	23			Ω
	series resistor for K.20, K.21 and K.45 1.5 kV, 10/700 surge survival	0			Ω
	series resistor for K.20, K.21 and K.45 coordination with a 400 V primary protector	7			Ω

Electrical Characteristics, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
I_{DRM}	Repetitive peak off-state current	$V_D = V_{DRM}$	T_A = 25 °C			±5	μA
			T_A = 85 °C			±10	
$V_{(BO)}$	Breakover voltage	dv/dt = ±250 V/ms, R_{SOURCE} = 300 Ω	'4070			±70	V
			'4080			±80	
			'4090			±90	
			'4125			±125	
			'4145			±145	
			'4165			±165	
			'4180			±180	
			'4220			±220	
			'4240			±240	
			'4260			±260	
			'4290			±290	
			'4320			±320	
			'4350			±350	
			'4360			±360	
			'4395			±395	
$I_{(BO)}$	Breakover current	dv/dt = ±250 V/ms, R_{SOURCE} = 300 Ω				±0.8	A
I_H	Holding current	I_T = ±5 A, di/dt = +/-30 mA/ms		±0.15		±0.60	A
dv/dt	Critical rate of rise of off-state voltage	Linear voltage ramp, Maximum ramp value < 0.85V_{DRM}		±5			kV/μs
I_D	Off-state current	'4070, V_D = ±52 V '4080, V_D = ±59 V '4090, V_D = ±63 V '4125, V_D = ±90 V '4145, V_D = ±108 V '4165, V_D = ±122 V '4180, V_D = ±131 V '4220, V_D = ±144 V '4240, V_D = ±162 V '4260, V_D = ±180 V '4290, V_D = ±207 V '4320, V_D = ±216 V '4350, V_D = ±248 V '4360, V_D = ±261 V '4395, V_D = ±288 V				±2	μA
I_D	Off-state current	V_D = ±50 V				±10	μA

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Electrical Characteristics, T_A = 25 °C (Unless Otherwise Noted) (Continued)

Parameter		Test Conditions		Min	Typ	Max	Unit
C_{off}	Off-state capacitance	f = 1 MHz, V_d = 1 V rms, V_D = ±1V	4070 thru ‘4090		53	64	pF
			‘4125 thru ‘4220		40	48	
			‘4240 thru ‘4395		33	40	
		f = 1 MHz, V_d = 1 V rms, V_D = ±50 V	‘4070 thru ‘4090		25	30	
			‘4125 thru ‘4220		18	22	
			‘4240 thru ‘4395		14	17	

Thermal Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
$R_{\theta JA}$	Junction to free air thermal resistance	EIA/JESD51-3 PCB, $I_T = I_{TSM(1000)}$, T_A = 25 °C, (see Note 75)			115	°C/W
		265 mm x 210 mm populated line card, 4-layer PCB, $I_T = I_{TSM(1000)}$, T_A = 25 °C		52		

NOTE 5: EIA/JESD51-2 environment and PCB has standard footprint dimensions connected with 5 A rated printed wiring track widths.

Parameter Measurement Information

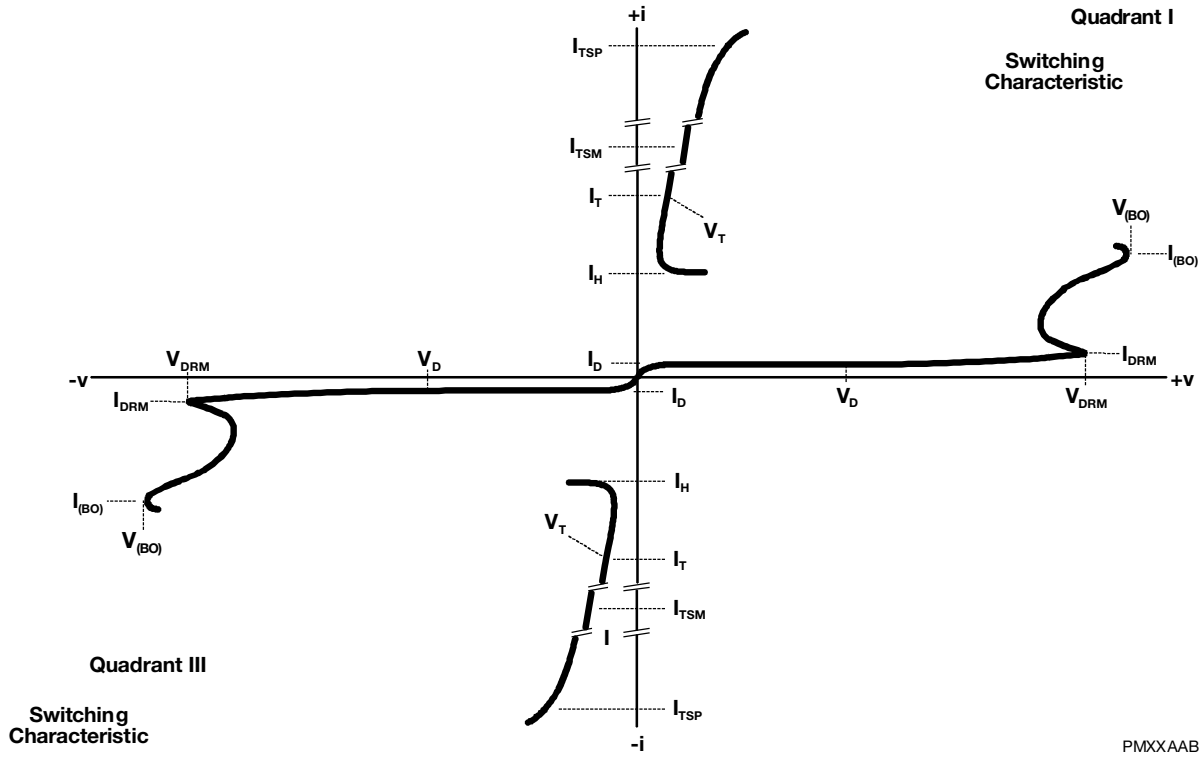

Figure 1. Voltage-Current Characteristic for T and R Terminals
All Measurements are Referenced to the R Terminal

Typical Characteristics

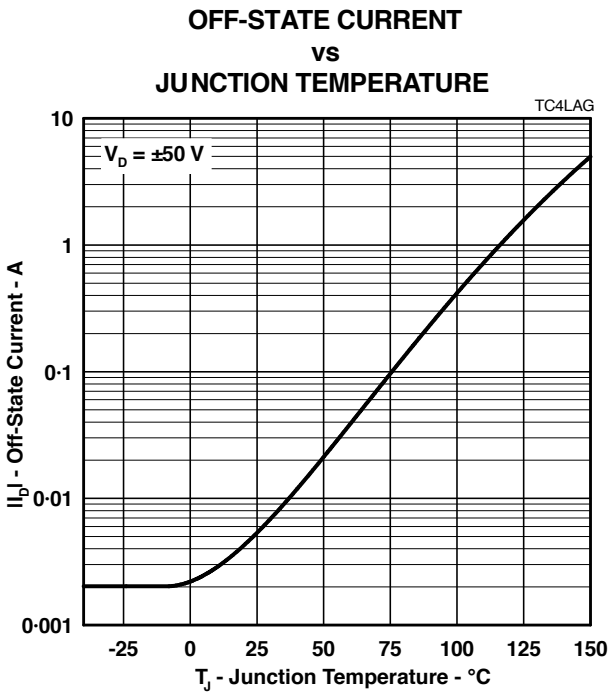

Figure 2.

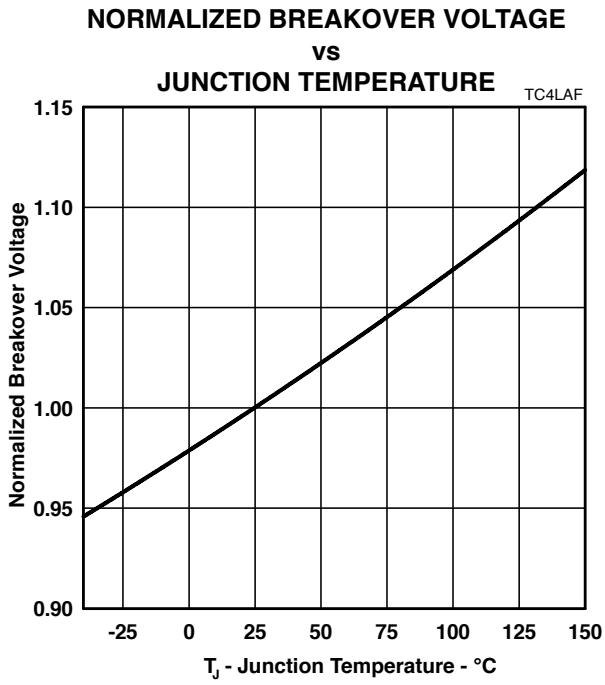

Figure 3.

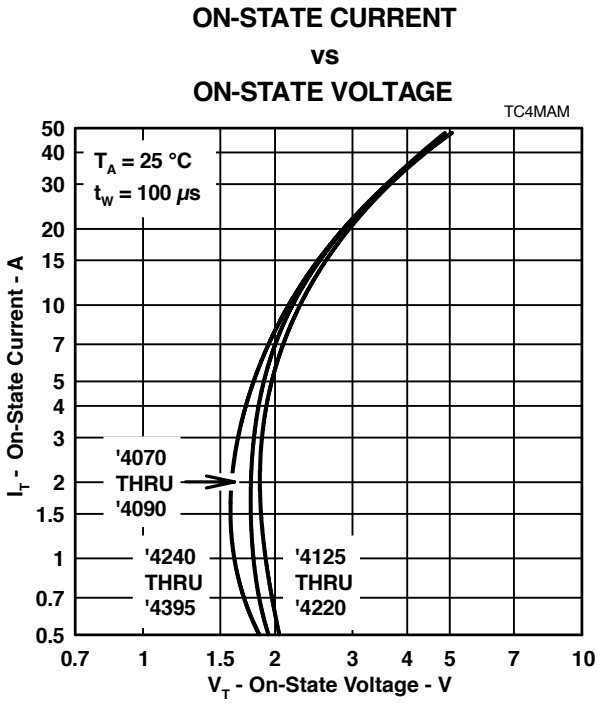

Figure 4.

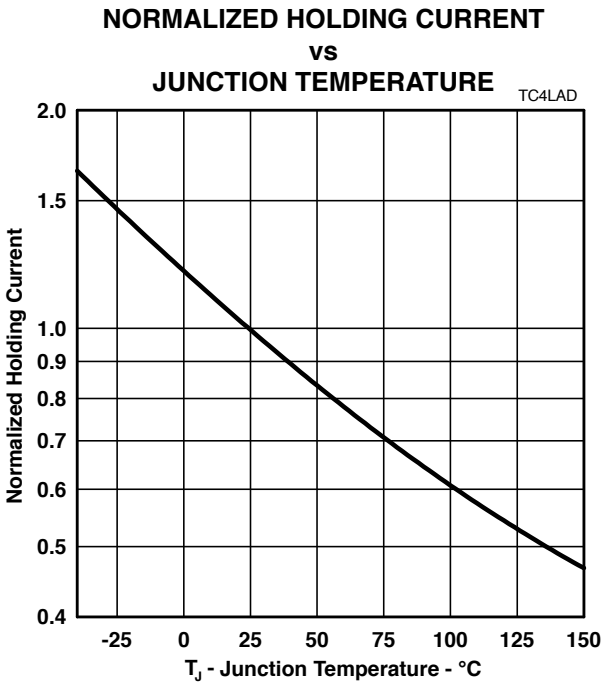

Figure 5.

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Typical Characteristics

NORMALIZED CAPACITANCE vs OFF-STATE VOLTAGE

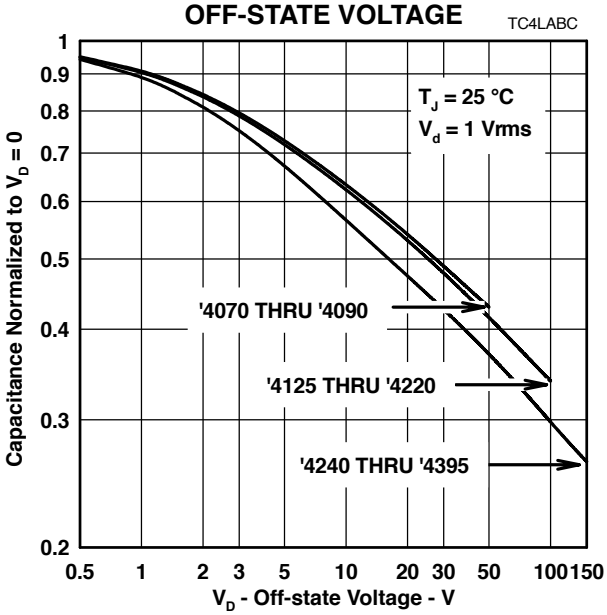

Figure 6.

DIFFERENTIAL OFF-STATE CAPACITANCE vs RATED REPETITIVE PEAK OFF-STATE VOLTAGE

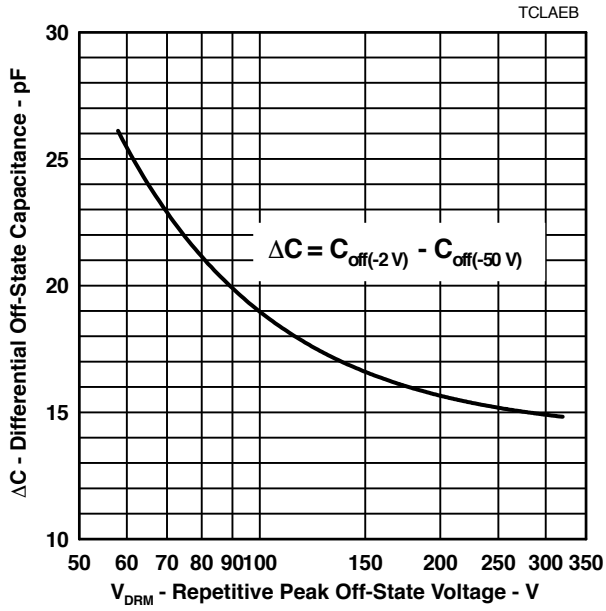

Figure 7.

TYPICAL CAPACITANCE ASYMMETRY vs OFF-STATE VOLTAGE

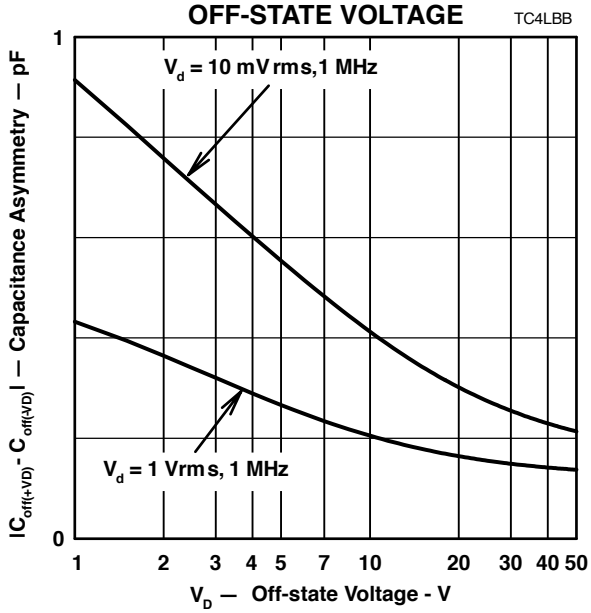

Figure 6.

Rating and Thermal Information

NON-REPETITIVE PEAK ON-STATE CURRENT vs CURRENT DURATION

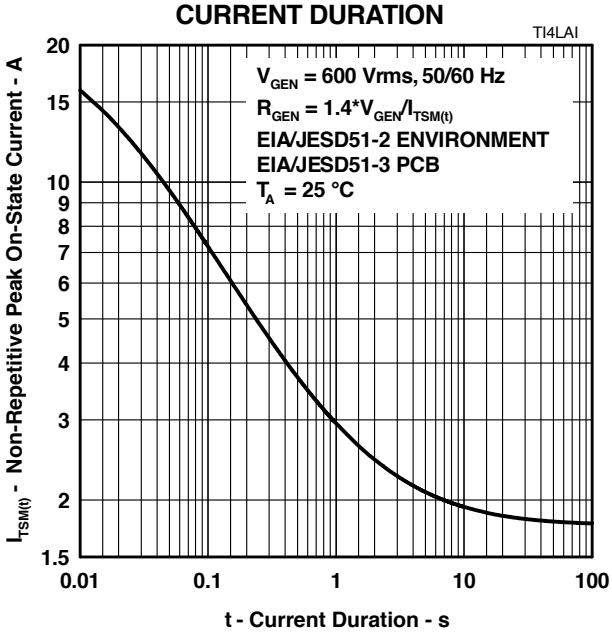

Figure 9.

V_{DRM} DERATING FACTOR vs MINIMUM AMBIENT TEMPERATURE

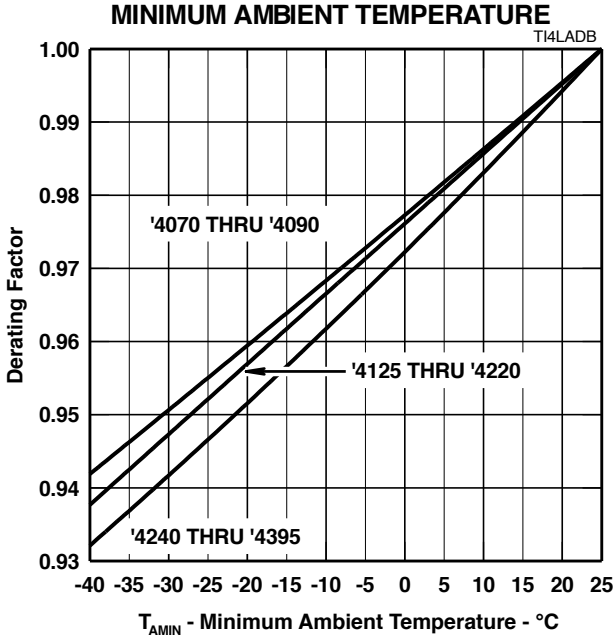

Figure 10.

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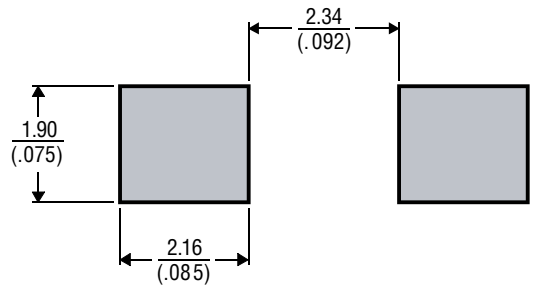
MECHANICAL DATA

Recommended Printed Wiring Land Pattern Dimensions

SMA Land Pattern



DIMENSIONS ARE: MILLIMETERS / (INCHES)

MDXXBIC

Device Symbolization Code

Devices will be coded as below. As the device parameters are symmetrical, terminal 1 is not identified.

Device	Symbolization Code
TISP4070L3	4070L
TISP4080L3	4080L
TISP4090L3	4090L
TISP4125L3	4125L
TISP4145L3	4145L
TISP4165L3	4165L
TISP4180L3	4180L
TISP4220L3	4220L
TISP4240L3	4240L
TISP4260L3	4260L
TISP4290L3	4290L
TISP4320L3	4320L
TISP4350L3	4350L
TISP4360L3	4360L
TISP4395L3	4395L

Carrier Information

For production quantities, the carrier will be embossed tape reel pack. Evaluation quantities may be shipped in bulk pack or embossed tape.

Carrier	Standard Quantity
Embossed Tape Reel Pack	5,000

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