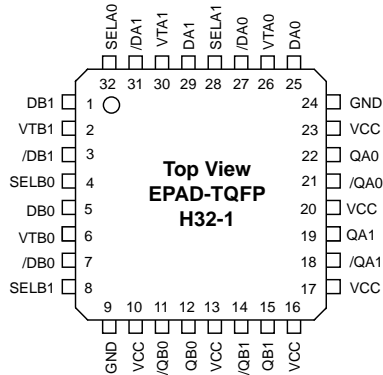


**PACKAGE/ORDERING INFORMATION****32-Pin EPAD-TQFP (H321)****Ordering Information<sup>(1)</sup>**

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY55858UHI	H32-1	Industrial	SY55858UHI	Sn-Pb
SY55858UHITR <sup>(2)</sup>	H32-1	Industrial	SY55858UHI	Sn-Pb
SY55858UHG <sup>(3)</sup>	H32-1	Industrial	SY55858UHG with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY55858UHGTR <sup>(2, 3)</sup>	H32-1	Industrial	SY55858UHG with Pb-Free bar-line indicator	Pb-Free NiPdAu

**Notes:**

1. Contact factory for die availability. Dice are guaranteed at  $T_A = 25^\circ\text{C}$ , DC Electricals only.
2. Tape and Reel.
3. Pb-Free package recommended for new designs.

**TRUTH TABLES**

SELA0	SELA1	QA0	QA1	Function
0	0	DA0	DA0	Fanout Buffer or Redundant Distribution
0	1	DA0	DA1	Dual Buffer or Crosspoint
1	0	DA1	DA0	Dual Buffer or Crosspoint
1	1	DA1	DA1	Fanout Buffer or Redundant Distribution

**Table 1. Input to Output Connectivity Crosspoint A**

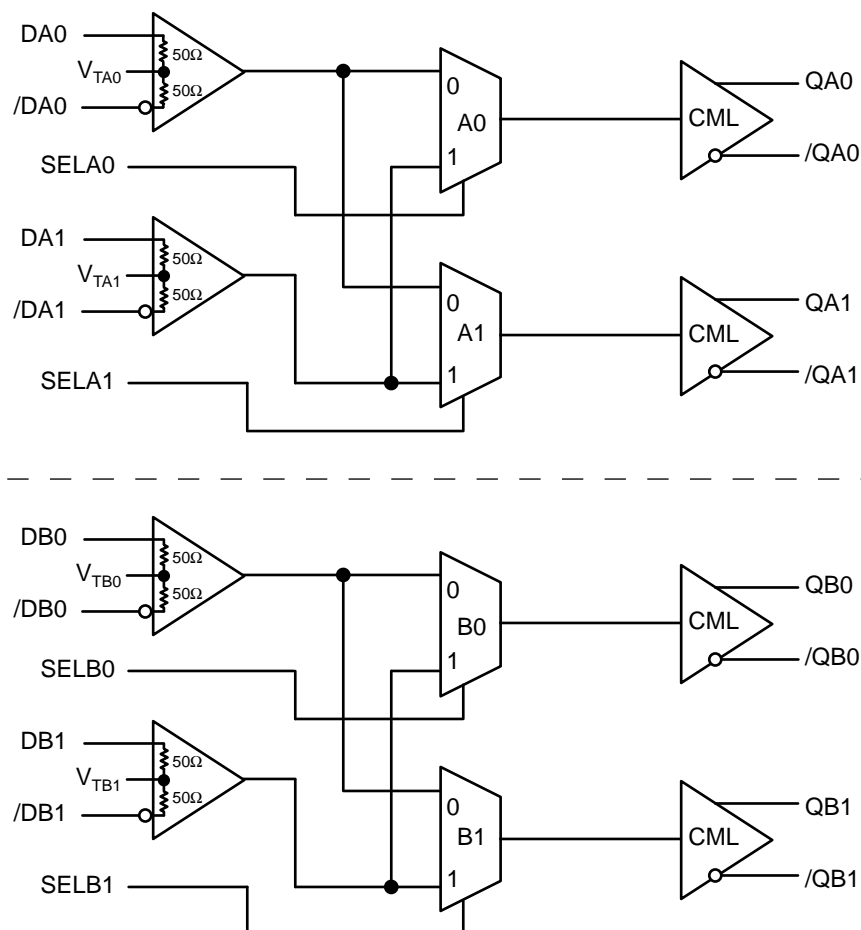
SELB0	SELB1	QB0	QB1	Function
0	0	DB0	DB0	Fanout Buffer or Redundant Distribution
0	1	DB0	DB1	Dual Buffer or Crosspoint
1	0	DB1	DB0	Dual Buffer or Crosspoint
1	1	DB1	DB1	Fanout Buffer or Redundant Distribution

**Table 2. Input to Output Connectivity Crosspoint B**

**PIN DESCRIPTION**

Pin Number	Pin Name	Pin Function
1	DB1	Channel B1 positive signal input.
2	VTB1	Channel B1 termination center-tap. For CML inputs, leave this pin floating. Otherwise, see Figures 5a–5d in “Input Interface Application” section.
3	/DB1	Channel B1 negative signal input.
4	SELB0	Channel B0 output select. TTL/CMOS input.
5	DB0	Channel B0 positive signal input.
6	VTB0	Channel B0 termination center-tap. For CML inputs, leave this pin floating. Otherwise, see Figures 5a–5d in “Input Interface Application” section.
7	/DB0	Channel B0 negative signal input.
8	SELB1	Channel B1 output select. TTL/CMOS input.
9, 24	GND	Supply Ground.
10, 13, 16, 17, 20, 23	VCC	Positive supply normally connect to 2.5V, 3.3V, or 5V nominal supply, and bypass each pin with 0.1μF//0.01μF low ESR capacitors.
11	/QB0	Channel B0 negative signal output. 50Ω CML.
12	QB0	Channel B0 positive signal output. 50Ω CML.
14	/QB1	Channel B1 negative signal output. 50Ω CML.
15	QB1	Channel B1 positive signal output. 50Ω CML.
18	/QA1	Channel A1 negative signal output. 50Ω CML.
19	QA1	Channel A1 positive signal output. 50Ω CML.
21	/QA0	Channel A0 negative signal output. 50Ω CML.
22	QA0	Channel A0 positive signal output. 50Ω CML.
25	DA0	Channel A0 positive signal input.
26	VT A0	Channel A0 termination center-tap. For CML inputs, leave this pin floating. Otherwise, see Figures 5a–5d in “Input Interface Application” section.
27	/DA0	Channel A0 negative signal input.
28	SELA1	Channel A1 output select. TTL/CMOS input.
29	DA1	Channel A1 positive signal input.
30	VT A1	Channel A1 termination center-tap. For CML inputs, leave this pin floating. Otherwise, see Figures 5a–5d in “Input Interface Application” section.
31	/DA1	Channel A1 negative signal input.
32	SELA0	Channel A1 output select. TTL/CMOS input.

## FUNCTIONAL BLOCK DIAGRAM



## INPUT AND OUTPUT STAGE

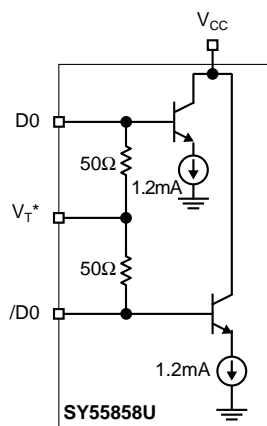


Figure 1. Input Stage

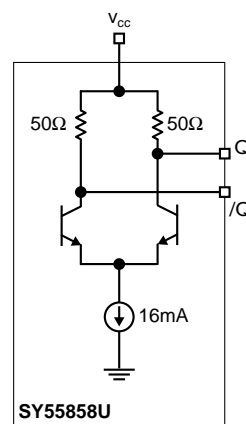


Figure 2. Output Stage

**Note 1.** See "Input Interface Applications" section for proper input connection.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Value	Unit
$V_{CC}$	Power Supply Voltage	-0.5 to +6.0	V
$V_{IN}$	Input Voltage	-0.5 to $V_{CC} + 0.5$	V
$V_{OUT}$	CML Output Voltage	$V_{CC} - 1.0$ to $V_{CC} + 0.5$	V
$T_A$	Operating Temperature Range	-40 to +85	°C
$T_{LEAD}$	Lead Temperature (soldering, 20sec.)	260	°C
$T_{store}$	Storage Temperature Range	-65 to +150	°C
$\theta_{JA}$	Package Thermal Resistance (Junction-to-Ambient)	-Still-Air (multi-layer PCB) -500lfpm (multi-layer PCB)	28 20 °C/W °C/W
$\theta_{JC}$	Package Thermal Resistance (Junction-to-Case)	4	°C/W

**Note 1.** Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**DC ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
$V_{CC}$	Power Supply Voltage	2.3	—	3.6	V	
$I_{CC}$	Power Supply Current	—	150	190	mA	No load, over temp.

**TTL CONTROL ELECTRICAL CHARACTERISTICS**

$V_{CC} = 2.3V$  to  $3.6V$ ;  $GND = 0V$ ;  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ <sup>(2)</sup>

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
$V_{IH}$	Input HIGH Voltage	2.0	—	—	V	
$V_{IL}$	Input LOW Voltage	—	—	0.8	V	
$I_{IH}$	Input HIGH Current	—	—	+20 +100	$\mu A$ $\mu A$	$V_{IN} = 2.7V$ , $V_{CC} = \text{Max.}$ $V_{IN} = V_{CC}$ , $V_{CC} = \text{Max.}$
$I_{IL}$	Input LOW Current	-300	—	—	$\mu A$	$V_{IN} = 0.5V$ , $V_{CC} = \text{Max.}$

**Note 2.** Specifications are guaranteed after thermal equilibrium has been established.

**CML DC ELECTRICAL CHARACTERISTICS**
 $V_{CC} = 2.3V$  to  $3.6V$ ;  $GND = 0V$ ;  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ <sup>(3)</sup>

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
$V_{ID}$	Differential Input Voltage	100	—	—	mV	
$R_{IN}$	Differential Input Resistance D-to-/D	90	100	110	$\Omega$	
$V_{IH}$	Input HIGH Voltage	1.6	—	$V_{CC}$	V	
$V_{IL}$	Input LOW Voltage	1.5	—	$V_{CC} - 0.1$	V	
$V_{OH}$	Output HIGH Voltage	$V_{CC} - 0.040$	$V_{CC} - 0.010$	$V_{CC}$	V	No Load
$V_{OL}$	Output LOW Voltage	$V_{CC} - 1.00$	$V_{CC} - 0.800$	$V_{CC} - 0.650$	V	No Load
$V_{OUT(SWING)}$	Output Voltage Swing <sup>(4)</sup>	0.650 —	0.800 0.400	1.00 —	V	No Load 50 $\Omega$ Environment
$R_{OUT}$	Output Source Impedance	40	50	60	$\Omega$	

**Note 3.** Device is guaranteed to meet the DC specifications, shown in the table above, after thermal equilibrium has been established. The device is tested in a socket such that traverse airflow  $\geq 500$ lfpm is maintained.

**Note 4.**  $V_{OUT(SWING)}$  is defined as the swing on one output of a differential pair, that is  $|V_{OH} - V_{OL}|$  on one pin. The swing for common mode immunity purposes is  $2 \times V_{OUT(SWING)}$ . Actual voltage levels and differential swing will depend on customer termination scheme. Typically, a 400mV swing is available in the 50 $\Omega$  environment. Refer to the "CML Output Termination Application" section, Figures 3 and 4, for more details.

**AC ELECTRICAL CHARACTERISTICS**
 $V_{CC} = 2.3V$  to  $3.6V$ ;  $GND = 0V$ ;  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ <sup>(5)</sup>

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
$f_{MAX}$	Maximum Frequency NRZ Data Rate	3.0	—	—	Gbps	
	Clock Frequency <sup>(6)</sup>	3.0	—	—	GHz	
$t_{PLH}$ $t_{PHL}$	Differential Propagation Delay D-to-Q	220	350	450	ps	
$t_{SWITCH}$	Select-to-Valid Output <sup>(7)</sup>	—	0.50	1.0	ns	
$t_{SKEW}$	Within-Device Skew <sup>(8)</sup>	—	12	25	ps	
	Within-Device Skew <sup>(9)</sup>	—	25	50	ps	
	Part-to-Part Skew (Diff.)	—	100	—		
$R_J$	Random Jitter	—	2	5	ps <sub>RMS</sub>	
$D_J$	Deterministic Jitter	—	5	20	ps <sub>PP</sub>	
$t_r, t_f$	CML Output Rise/Fall Times (20% to 80%)	—	80	120	ps	

**Note 5.** Tested using environment of Figure 3, 50 $\Omega$  equivalent load. AC parameters are guaranteed by design and characterization.

**Note 6.**  $f_{MAX}$  clock is defined as the maximum toggle rate the device can operate while still achieving a 250mV minimum CML output swing, 50 $\Omega$  equivalent load.

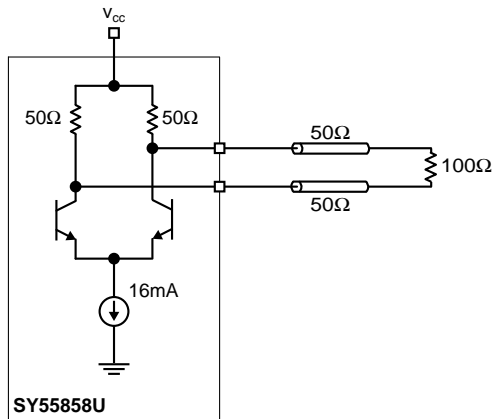
**Note 7.** Input TTL/CMOS edge rate of  $<1.5$ ns.

**Note 8.** Worst-case difference between QA0 and QA1 from either DA0 or DA1 (or between QB0 and QB1 from either DB0 or DB1 respectively), when both outputs come from the same input.

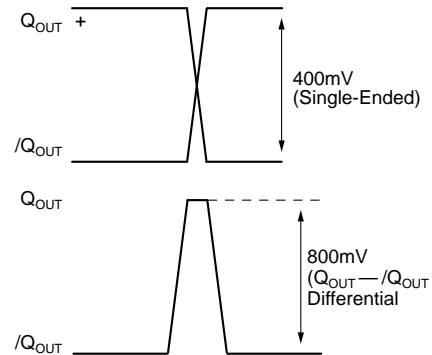
**Note 9.** Worst-case difference between QA and QB outputs, when DA or DB inputs are shorted.

## CML OUTPUT TERMINATION APPLICATION

All CML inputs accept a CML output from any other member of this family. All CML outputs are source terminated 50Ω differential drivers as shown in **Figure 3**.

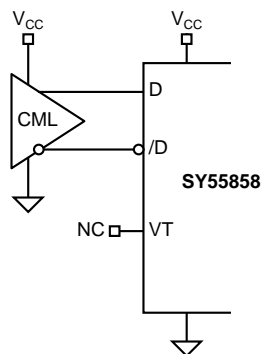


**Figure 3. 50Ω Output Termination**

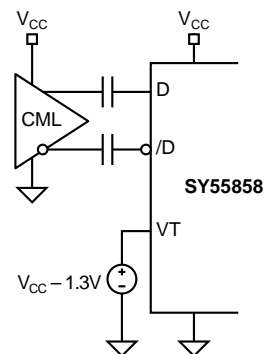


**Figure 4. Output Levels**

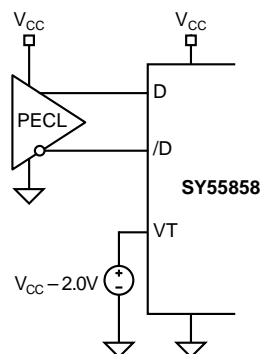
## INPUT INTERFACE APPLICATIONS



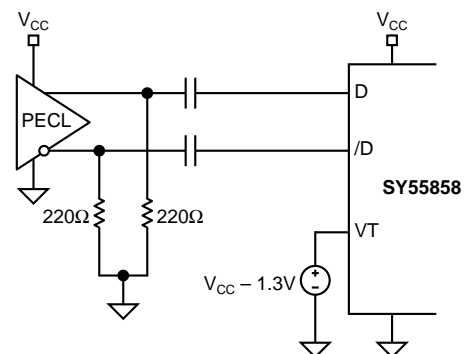
**Figure 5a. CML-to-CML  
(DC-Coupled) Input Interface**



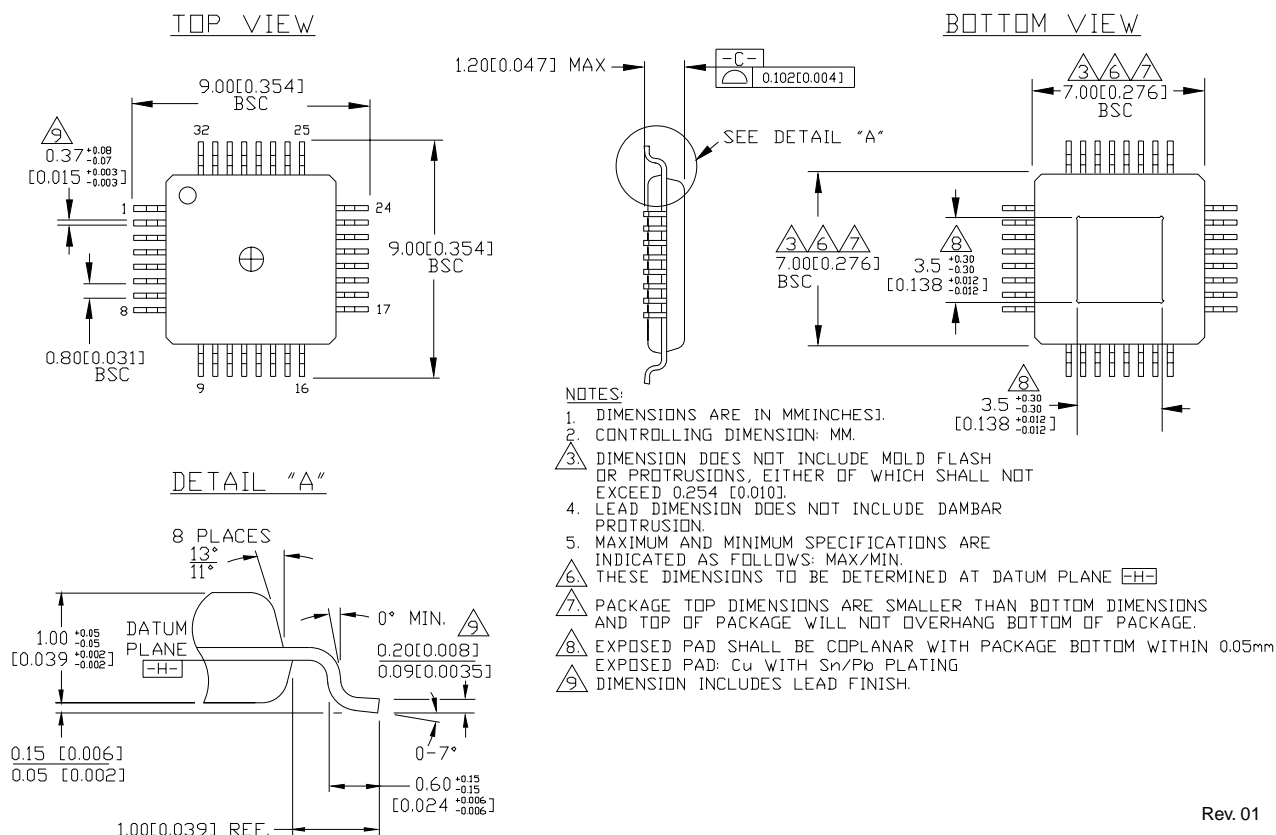
**Figure 5b. CML-to-CML  
(AC-Coupled) Input Interface**



**Figure 5c. PECL-to-CML  
(DC-Coupled) Input Interface**



**Figure 5d. PECL-to-CML  
(AC-Coupled) Input Interface**

**32 -PIN EPAD-TQFP (DIE UP) (H32-1)**

Rev. 01

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