

# 1 Electrical characteristics

**Table 1. Absolute maximum ratings (limiting values)**

Symbol	Parameter	Rating	Unit
$P_{IN}$	Input peak power $RF_{IN}$ (CW mode)/all RF ports	+40	dBm
$V_{ESD(HBM)}$	Human body model, JESD22-A114-B, all I/O	Class 1B <sup>(1)</sup>	V
$V_{ESD(MM)}$	Machine model, JESD22-A115-A, all I/O	100	V
$T_{device}$	Device temperature	+125	°C
$T_{stg}$	Storage temperature	-55 to +150	
$V_x$	Bias voltage	25	V

1. Class 1B defined as passing 500 V, but fails after exposure to 1000V ESD pulse.

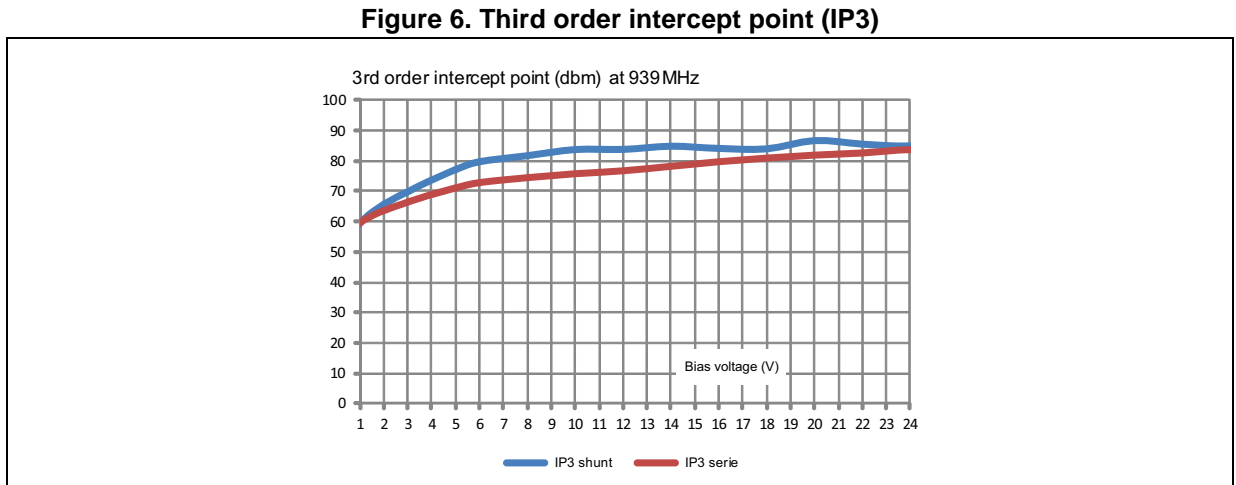
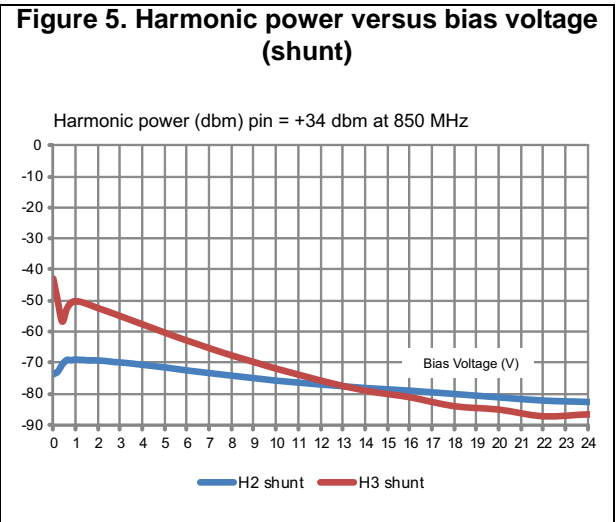
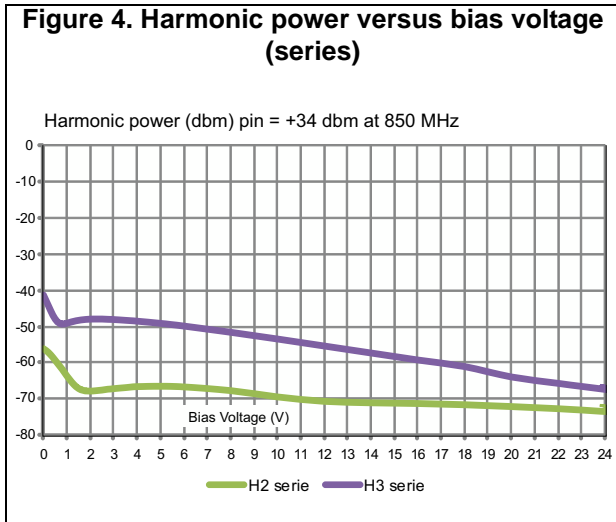
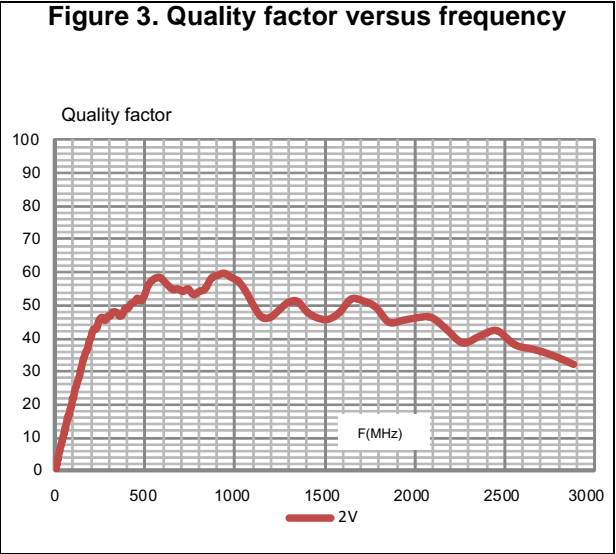
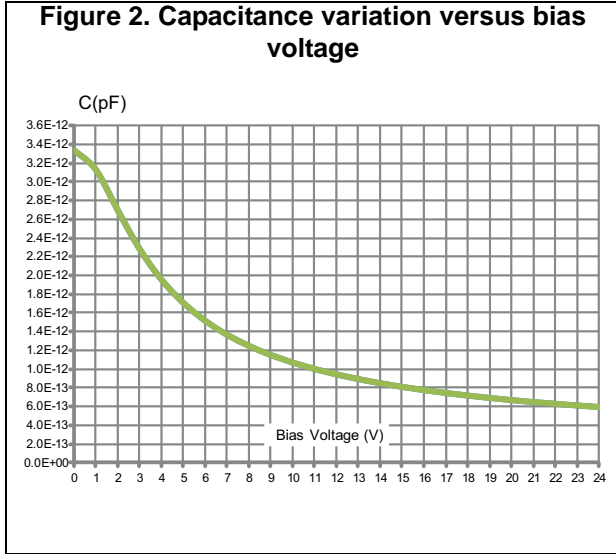
**Table 2. Recommended operating conditions**

Symbol	Parameter	Rating			Unit
		Min.	Typ.	Max.	
$P_{IN}$	RF input power		+33	+39	dBm
$F_{OP}$	Operating frequency	700		2700	MHz
$T_{device}$	Device temperature			+100	°C
$T_{OP}$	Operating temperature	-30		+85	
$V_{BIAS}$	Bias voltage	1		24	V

Table 3. Representative performance ( $T_{amb} = 25\text{ }^{\circ}\text{C}$  otherwise specified)

Symbol	Parameter	Conditions	Value			Unit
			Min.	Typ.	Max.	
$C_{1V}$	capacitance at 1 V bias	STPTIC-27L2	2.8	3.2	3.58	pF
$C_{2V}$	capacitance at 2 V bias	STPTIC-27L2	2.43	2.7	2.97	pF
$C_{20V}$	capacitance at 20V bias	STPTIC-27L2	0.63	0.69	0.75	pF
$C_{24V}$	capacitance at 24 V bias	STPTIC-27L2	0.56	0.61	0.66	pF
$\Delta C$	Tuning range	Ratio between $C_{1V}/C_{24V}$ <sup>(1)</sup>	5/1			
$I_L$	Leakage current	Measured with $V_{bias} = 24\text{ V}$			100	nA
$Q_{LB}$	Quality factor	Measured at 700 MHz at 2 V	50	55		
$Q_{HB}$	Quality factor	Measured at 2700 MHz at 2 V	35	40		
IP3	Third order intercept point	$V_{bias} = 1\text{ V}^{(2)(4)}$	60			dBm
		$V_{bias} = 24\text{ V}^{(2)(4)}$	80			
		$V_{bias} = 20\text{ V}^{(2)(4)}$	80			
H2	Second harmonic	$V_{bias} = 1\text{ V}^{(3)(4)}$		-70	-65	dBm
		$V_{bias} = 24\text{ V}^{(3)(4)}$		-80	-75	
		$V_{bias} = 20\text{ V}^{(3)(4)}$			-65	
H3	Third harmonic	$V_{bias} = 1\text{ V}^{(3)(4)}$		-55	-45	dBm
		$V_{bias} = 24\text{ V}^{(3)(4)}$		-85	-70	
		$V_{bias} = 20\text{ V}^{(3)(4)}$			-70	
$t_T$	Transition time	Average for any transition between $C_{min}$ to $C_{max}$ <sup>(5)</sup>		50		$\mu\text{s}$
		Average transition between $C_{max}$ to $C_{min}$ <sup>(5)</sup>		30		

1. Measured at low frequency
2.  $F_1 = 894\text{ MHz}$ ,  $F_2 = 849\text{ MHz}$ ,  $P_1 = +25\text{ dBm}$ ,  $P_2 = +25\text{ dBm}$ ,  $2f_1 - f_2 = 939\text{ MHz}$
3.  $850\text{ MHz}$ ,  $P_{in} = +34\text{ dBm}$ , CW
4. IP3 and harmonics are measured in the shunt configuration in a  $50\ \Omega$  environment
5. One or both of  $RF_{in}$  and  $RF_{out}$  must be connected to DC ground, using the HVDAC turbo mode



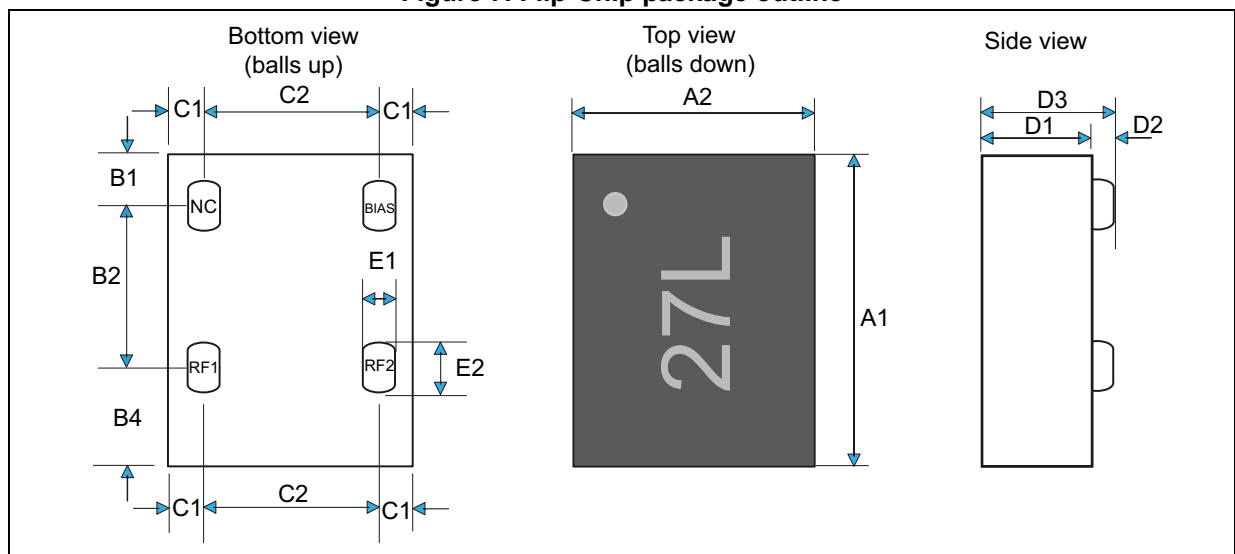
## 2 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 2.1 Flip-Chip package information

Figure 7. Flip-Chip package outline



The land pattern below is recommended for soldering the STPTIC-G2 on PCB.

NC stands for No Connect, this pad must not be connected on application board. Please leave this pad floating.

Table 4. Flip-Chip package dimensions

Dimensions (in microns)	A1	A2	B1	B2	B4	C1	C2	D1	D2	D3	E1	E2
STPTIC-27L2	1000	750	140	500	360	105	540	225	90	315	125	165
Tolerance	±30	±30	±15	±10	±15	±15	±10	±20	±20	±40	±20	±20

Figure 8. Recommended PCB land pattern for Flip-Chip package

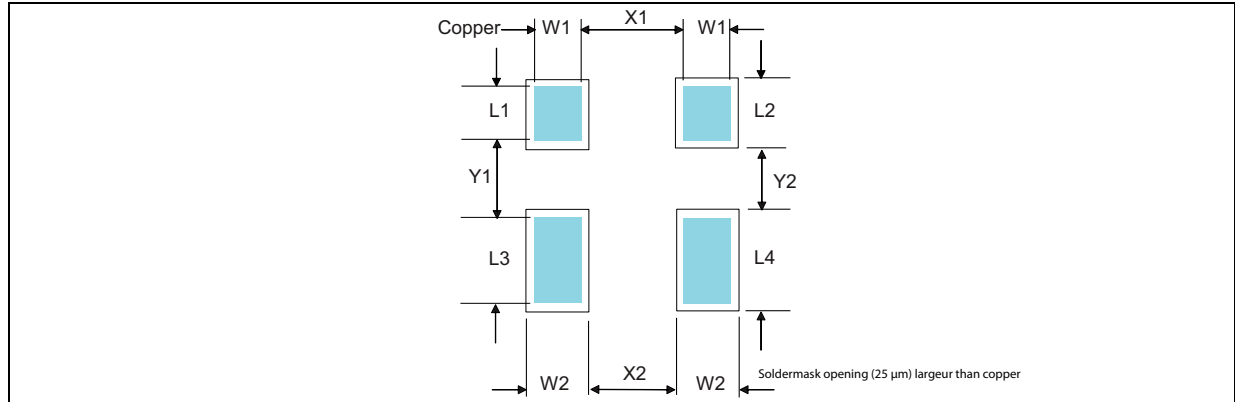


Table 5. Dimensions

Dimensions	L1	W1	L3	L2	W2	L4	X1	X2	Y1	Y2
Typical values (in microns)	160	160	260	210	210	310	320	270	240	190

## 2.2 Packing information

Figure 9. Flip-Chip tape and reel outline

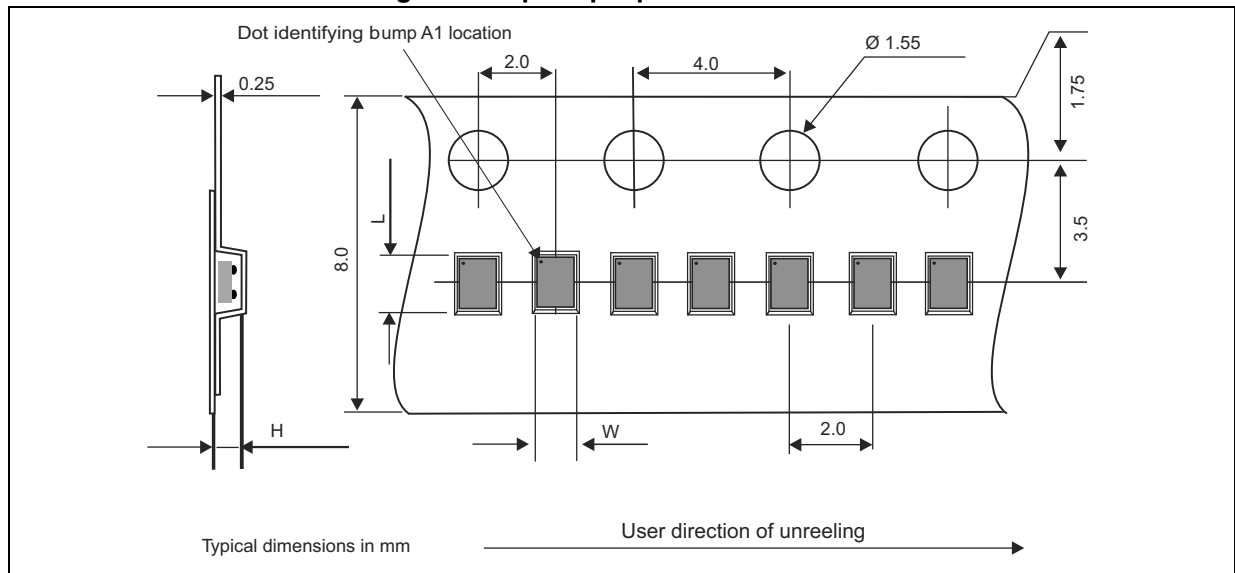


Table 6. Dimensions

Pocket dimensions	L	W	H
STPTIC-27L2	1070	820	380

Figure 10. Flip-Chip marking

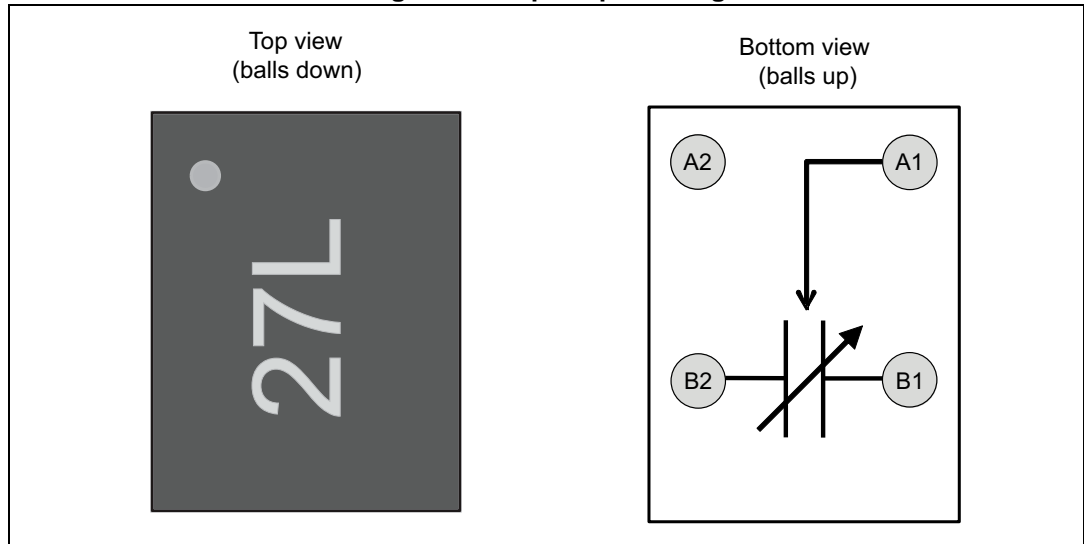


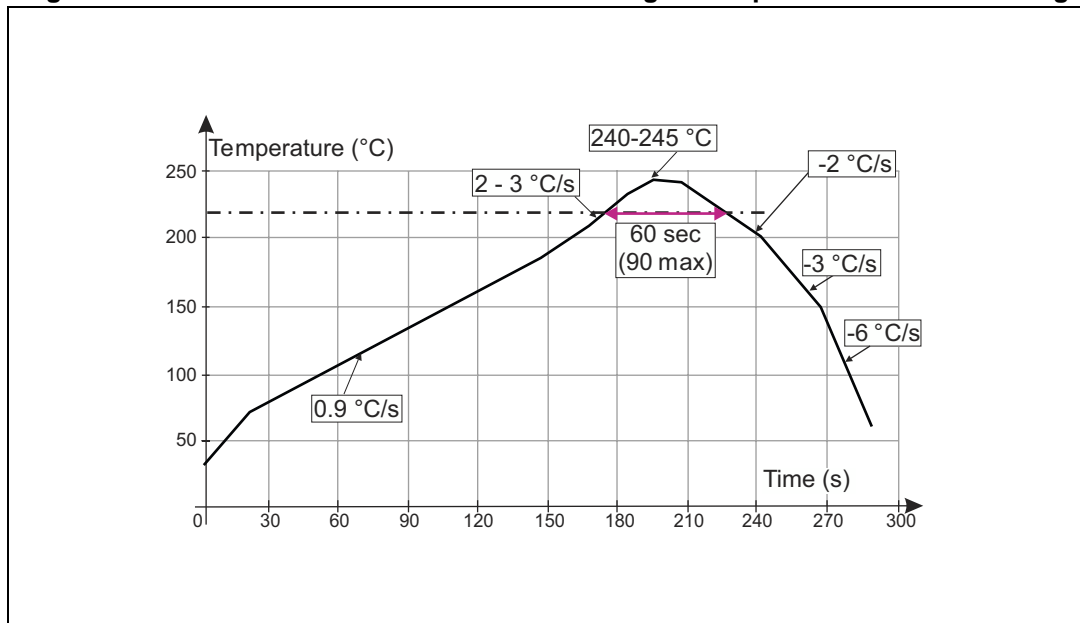
Table 7. Pinout description

Pad / ball number	Pin name	Description
A1	DC bias	DC bias voltage
B1	RF2	RF input / output <sup>(1)</sup>
A2	NC	Not connected
B2	RF1	RF input / output

1. When connected in shunt, please connect RF2 (B1 ball) to GND

### 3 Reflow profile

Figure 11. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

Table 8. Recommended values for soldering reflow

Profile	Value	
	Typical	Max.
Temperature gradient in preheat (T = 70-180 °C)	0.9 °C/s	3 °C/s
Temperature gradient (T = 200-225 °C)	2 °C/s	3 °C/s
Peak temperature in reflow	240-245 °C	260 °C
Time above 220 °C	60 s	90 s
Temperature gradient in cooling	-2 to -3 °C/s	-6 °C/s
Time from 50 to 220 °C	160 to 220 s	

## 4 Ordering information

Figure 12. Ordering information scheme

<b>ST</b>	<b>PTIC</b>	<b>-</b>	<b>27</b>	<b>L</b>	<b>2</b>	<b>C5</b>
<u>Manufacturer</u>	<u>Product family</u>	<b>-</b>	<u>Capacitor value</u>	<u>Linearity</u>	<u>Tuning</u>	<u>Package</u>
ST Microelectronics	PTIC Parascan™ tunable Integrated capacitor		15 = 1.5 pF 27 = 2.7 pF 33 = 3.3 pF 39 = 3.9 pF 47 = 4.7 pF 56 = 5.6 pF 68 = 6.8 pF 82 = 8.2 pF	F: Standard (x24) G: Standard (x24) L: High (x48)	1 = 4/1 tuning 2 = 5/1 tuning	M6 : QFN C5 : WLCSP 400 μm coating H5 : WLCSP

Table 9. Ordering information

Part number	Marking	Base qty	Package	Delivery mode
STPTIC-27L2C5	27L	15 000	Flip-Chip	Tape and reel

## 5 Revision history

Table 10. Document revision history

Date	Revision	Changes
04-Dec-2015	1	Initial release.



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