# Contents

# 1 Block diagram

**Figure 1. Block diagram (fixed version)**

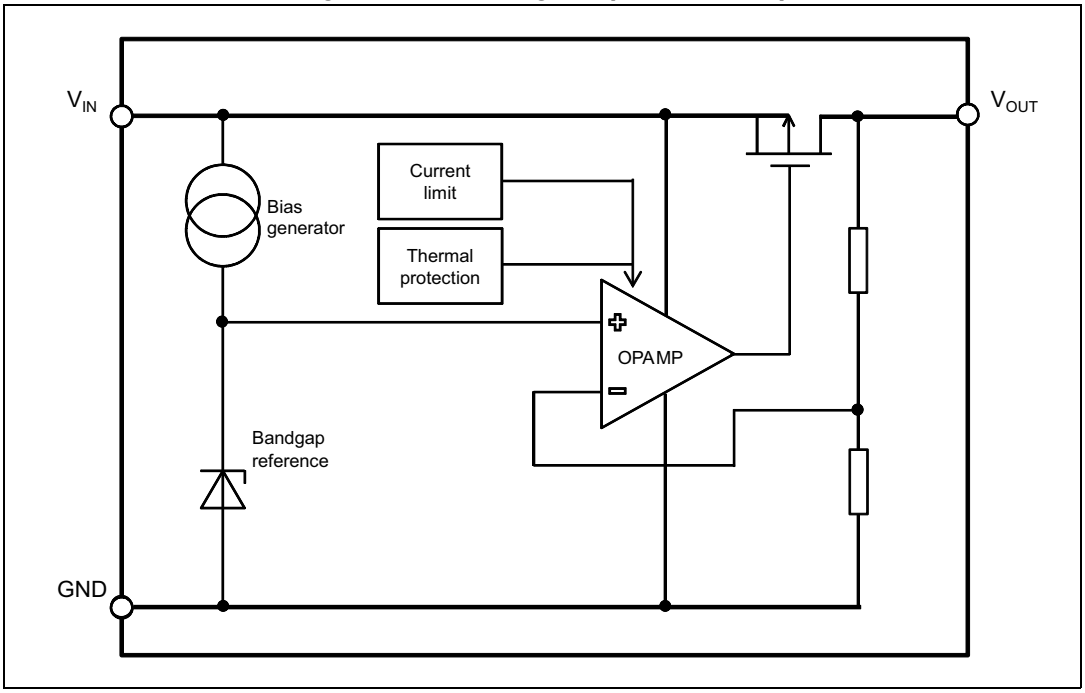
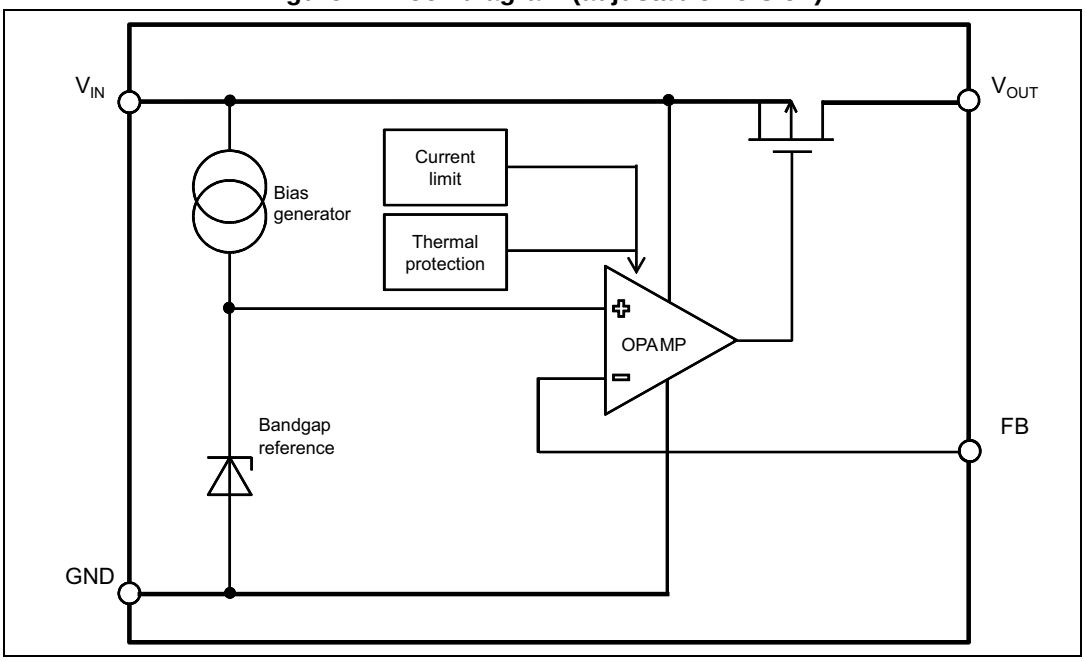



**Figure 2. Block diagram (adjustable version)**



# 2 Pin configuration

**Figure 3. Pin connections (top view)**

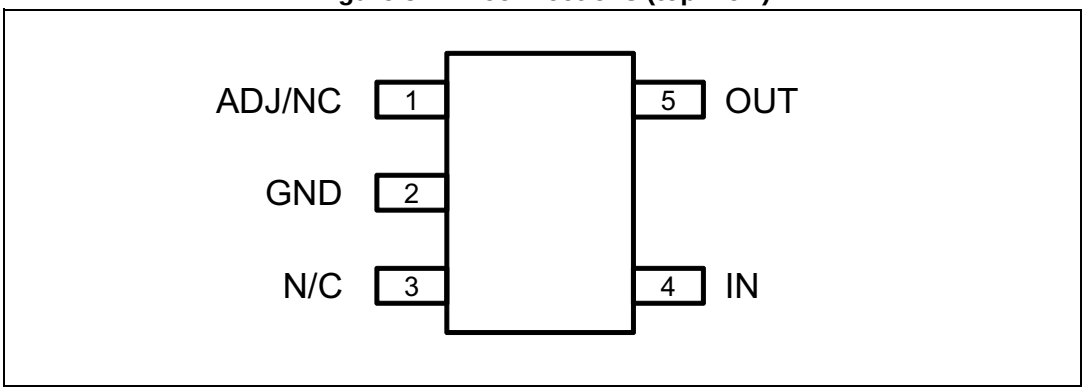



**Table 2. Pin description**

| Pin n° | Symbol | Note |
|---|---|---|
| 1 | ADJ | ADJ pin on the Adjustable version |
| | N/C | Not connected on fixed version |
| 2 | GND | Ground |
| 3 | N/C | Not connected |
| 4 | IN | Input voltage |
| 5 | OUT | Output voltage |

# 3 Maximum ratings

**Table 3. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_I$ | DC Input voltage | -0.3 to +14 | V |
| $V_{ADJ}$ | ADJ pin voltage | -0.3 to +7 | V |
| ESD | Human body model | ±2 | kV |
| $T_J$ | Junction temperature | -40 to 150 | °C |
| $T_{STG}$ | Storage temperature range | -55 to 150 | °C |

*Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.*

**Table 4. Thermal data**

| Symbol | Parameter | SOT323-5L | Unit |
|---|---|---|---|
| $R_{thJA}$ | Thermal resistance junction-ambient | 331.4 (1) | °C/W |

1. This value is referred to a 4-layer PCB, JEDEC standard test board.

# 4 Electrical characteristics

$V_I = V_{O(NOM)}$ +1 V or $V_I$ = 2.5 V if $V_O$ < 1.5 V; $T_A$= -40 °C to 125 °C; $I_O$ = 1 mA; typical values are at $T_A$ = 25 °C, $C_O$ = 1 µF unless otherwise specified.

**Table 5. Electrical characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_I$ | Input voltage range | $I_O$ = 20 mA | 2.3 | | 12 | V |
| | | $I_O$ = 50 mA | 2.5 | | 12 | |
| $I_Q$ | Quiescent current (measured on ground pin, fixed version) | $V_I$ = 5 V | | 3.5 | 5.0 | µA |
| | | $V_I$ = 12 V | | 4.1 | 6.0 | |
| $V_O$ | Output voltage range (STLQ50ADJ) | | 1.222 | | 11 | V |
| | Accuracy as percentage of nominal voltage at $T_J$ = 25 °C | | -2 | | +2 | % |
| $V_{DROP-MAX}$ | Max dropout voltage (1) | $I_O$ = 50 mA; | | 0.4 | 0.7 | V |
| $\Delta V_O$ | Load regulation | 1 mA < $I_O$ < 50 mA | | | 0.15 | %/mA |
| $\Delta V_O$ | Line regulation | $V_O$ = 1.5 V:<br>$V_O$ + 1 V < $V_I$ < 12 V;<br>$V_O$ < 1.5 V:<br>2.5 V < $V_I$ < 12 V; | | | 0.3 | %/V |
| SVR | Supply voltage rejection | $V_{RIPPLE}$ = 0.1 V,<br>$I_O$ = 20 mA, f = 120 Hz | | 30 | | dB |
| eN | Output noise voltage | $B_W$ from 200 Hz to 100 kHZ; $I_O$ = 10 mA | | 560 | | $\mu V_{RMS}$ |
| $T_h$ | Thermal protection | | | 160 | | °C |
| $I_{OMAX}$ | Maximum output current (2) | $V_O$ = 0 V | | 500 | | mA |

1. $V_I$ = 2.5 V when $V_{O(NOM)} \leq$ 2.1 V
2. The maximum power dissipation must not be exceeded, see application information for details.

# 5 Typical application

**Figure 4. Fixed versions**

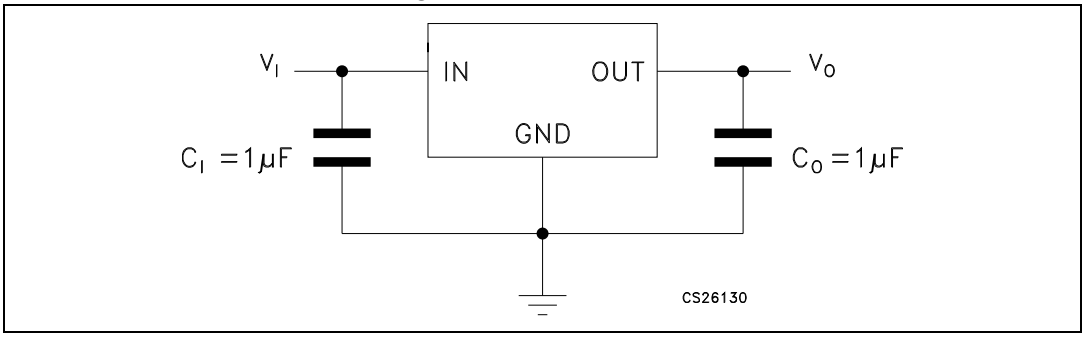
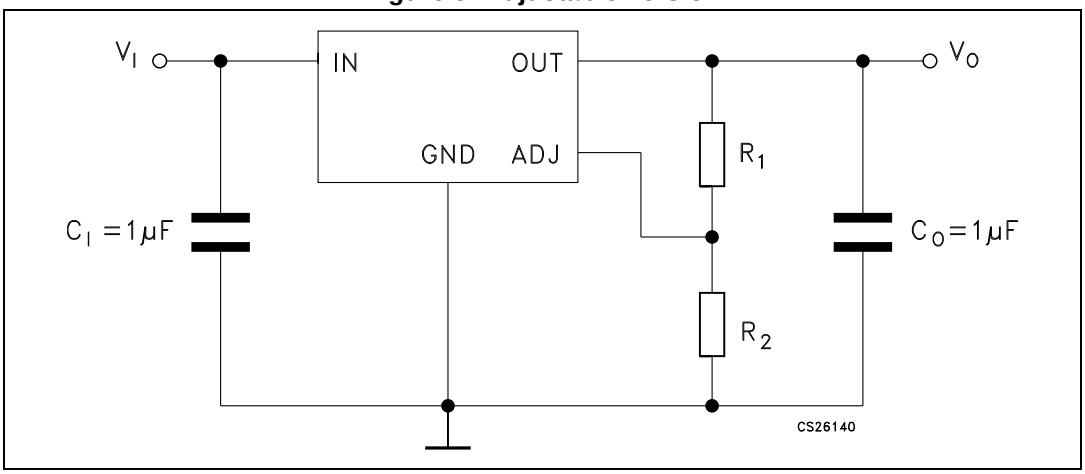



**Figure 5. Adjustable version**



# 6 Typical characteristics

Figure 6. $V_O$ vs. $T_J$

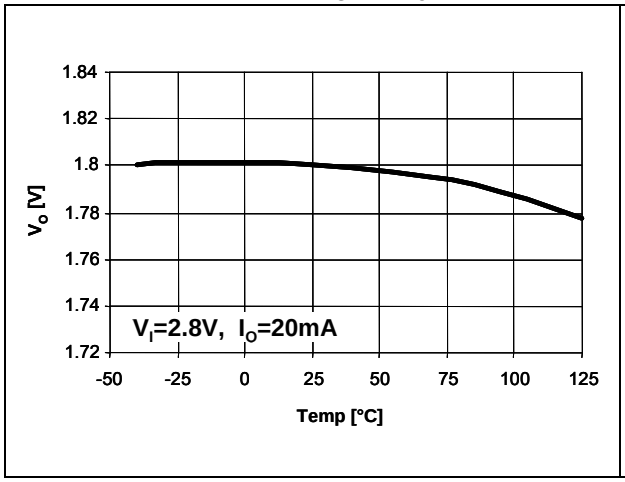



Figure 7. $V_O$ vs. $V_I$

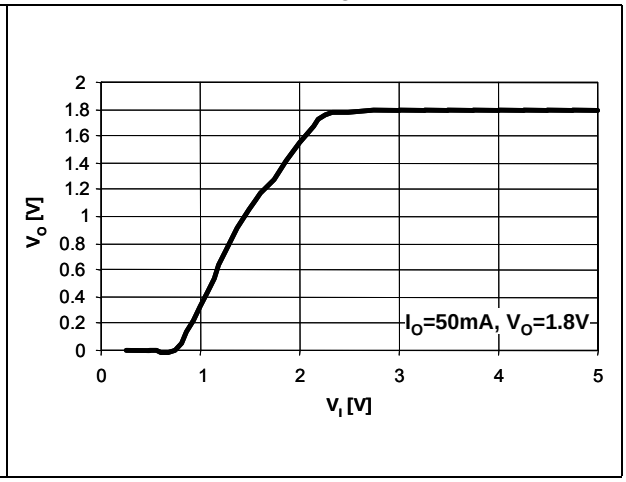



Figure 8. $I_Q$ vs. $T_J$

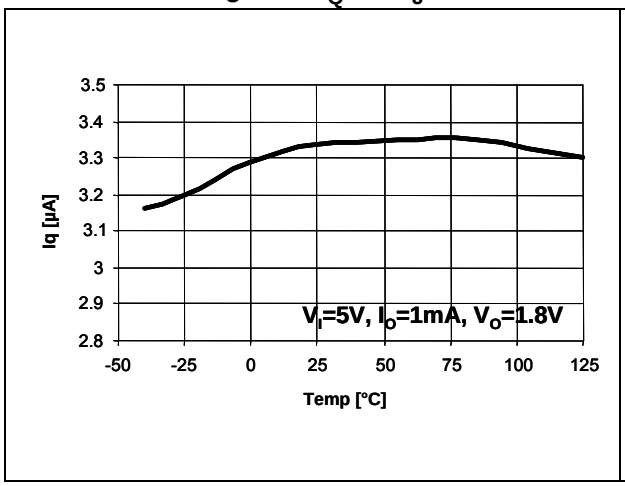



Figure 9. $V_{DROP}$ vs. $I_O$

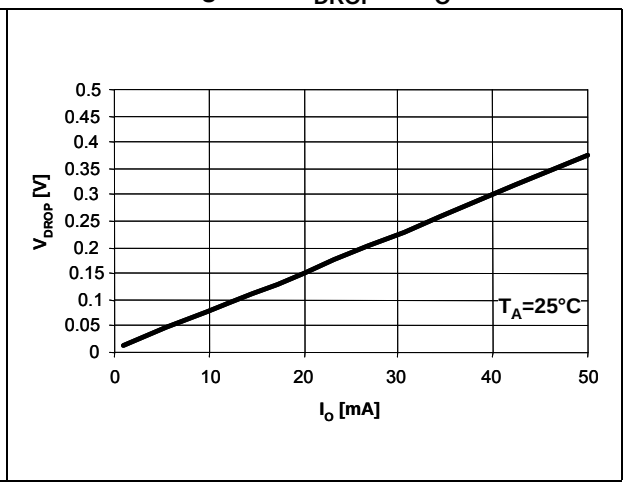



Figure 10. $V_{DROP}$ vs. $T_J$

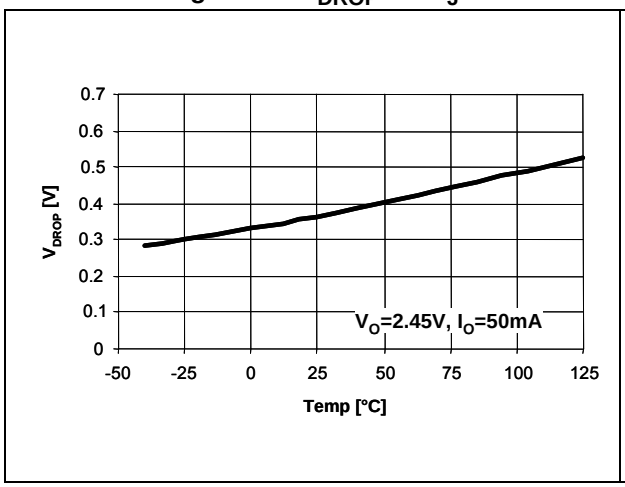



Figure 11. Stability

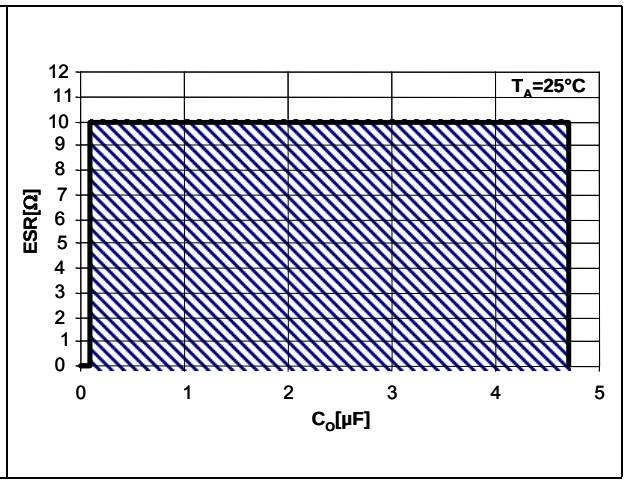


Figure 12. S.V.R. vs. Freq.

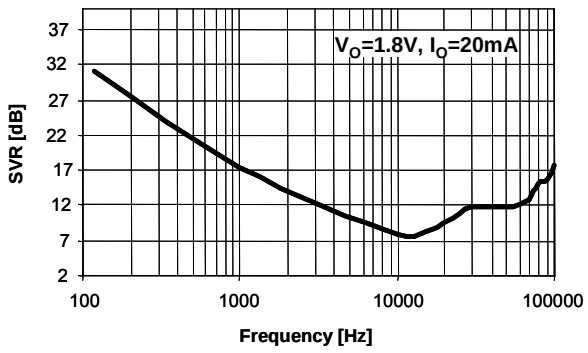



Figure 13. S.V.R. vs. $I_O$

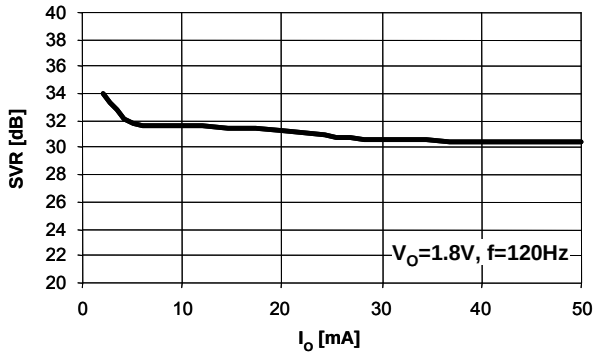
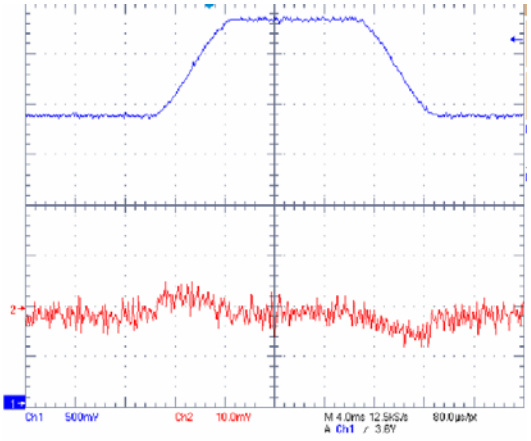
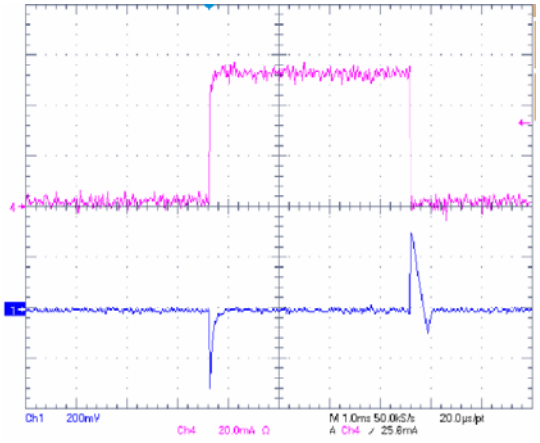



Figure 14. Line transient response



$I_O$=50mA; $C_O$=10µF; $V_I$=2.8V, $V_I$ rise/fall=5ms

Figure 15. Load transient response



$C_O$=1µF; $V_O$=1.8V; $V_I$=2.8V, Curr. rise/fall=1µs

Figure 16. Short-circuit current

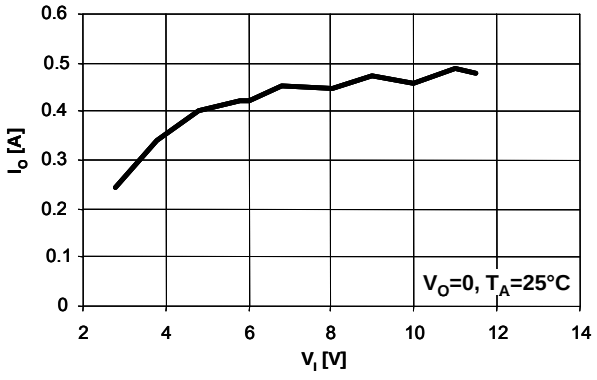
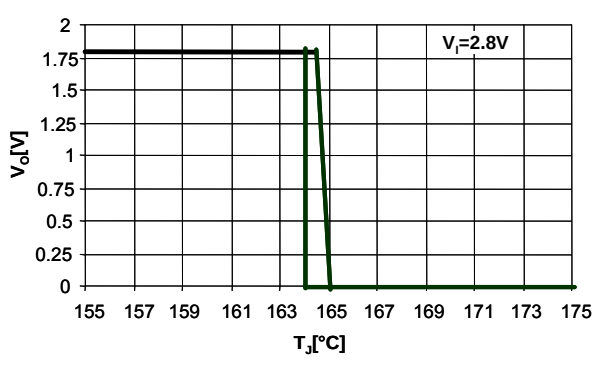



Figure 17. Thermal protection



# 7 Application information

The STLQ50 is a BiCMOS linear regulator specifically designed for operating in environments with very low power consumption requirements. The very low quiescent current of 3 µA is obtained through the use of CMOS technology which makes the device suitable for application that have long standby time. Its very low power consumption allows extended battery life and the tiny packages (SOT323-5L) satisfy the space-saving requirements of battery-powered equipment. Moreover, the STLQ50 provides wide input voltage operation from 2.5 V up to 12 V.

The PMOS pass element also permits a very good dropout values of 0.7 V at full load and at 125 °C without affecting consumption characteristics.

## 7.1 External components

The typical application schematic of the STLQ50 is shown in *Figure 4* - *Figure 5*, 1 µF input and output capacitors placed close to the device are required for proper operation. The device is stable with electrolytic and ceramic output capacitors having values higher than 1 µF (see *Figure 11* for stability details).

In the adjustable version the output voltage is programmed using an external resistor divider, as shown in *Figure 5*. The output voltage can be adjusted from 1.22 to 11 V and it can be calculated using the following equation:

**Equation 1**

$V_O = V_{FB} \times (1+R_1/R_2)$

where $V_{FB}$ = 1.222 V is the internal reference voltage.

The sum of the $R_1$ and $R_2$ resistors should be chosen in order to guarantee at least 1 µA of divider current. Lower value resistors improve the noise performance but the quiescent current will increase. Higher value resistors should be avoided because the ADJ leakage current will influence the voltage set by the resistor divider, rendering the formula above no longer valid.

The suggested design procedure is to choose $R_2$ = 1 MΩ and then calculate $R_1$ using the following equation:

**Equation 2**

$R_1 = (V_O/V_{FB}-1) \times R_2$

## 7.2 Power dissipation

In order to ensure proper operation, the STLQ50 junction temperature should never exceed 125 °C; this limits the maximum power dissipation the regulator can sustain in any application. The maximum power dissipation can be calculated as:

**Equation 3**

$P_{DMAX} = (T_{JMAX} - T_A)/R_{thJA}$

where $T_{JMAX}$ = 125 °C;

$T_A$ is the ambient temperature;

$R_{thJA}$ is the junction-to-ambient thermal resistance of the package (see *Table 4* thermal data).

The power dissipation can be calculated simply as:

**Equation 4**

$$P_D = (V_I - V_O) \times I_O$$

In every application condition, $P_D$ must be lower than $P_{DMAX}$.

## 7.3 Protection

The PMOS pass element has an internal diode with anode connected to $V_O$ and cathode to $V_I$. In case $V_O > V_I$, the current will flow from output to input without limitation. In this case, a proper limiting network is recommended.

The current limitation is automatically provided by the characteristics of the PMOS pass element (see typical characteristics), so the short-circuit current is dependent on the input voltage. When considering short-circuit current, take care in any case not to exceed the maximum sustainable power dissipation of the device.

The STLQ50 features an internal thermal protection that linearly reduces the output current when the internal temperature increases. Consequently, at a given load, the output voltage decreases also. The action of the thermal protection starts at 125 °C when the output voltage slightly decreases, while close to 163 °C the output voltage drops to 0 V. Since this is a linear control, sudden overcurrent conditions can quickly raise the chip temperature without giving time for the thermal protection to act, so it cannot be used as a limitation for the output current.

# 8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

**Figure 18. SOT323-5L drawing**

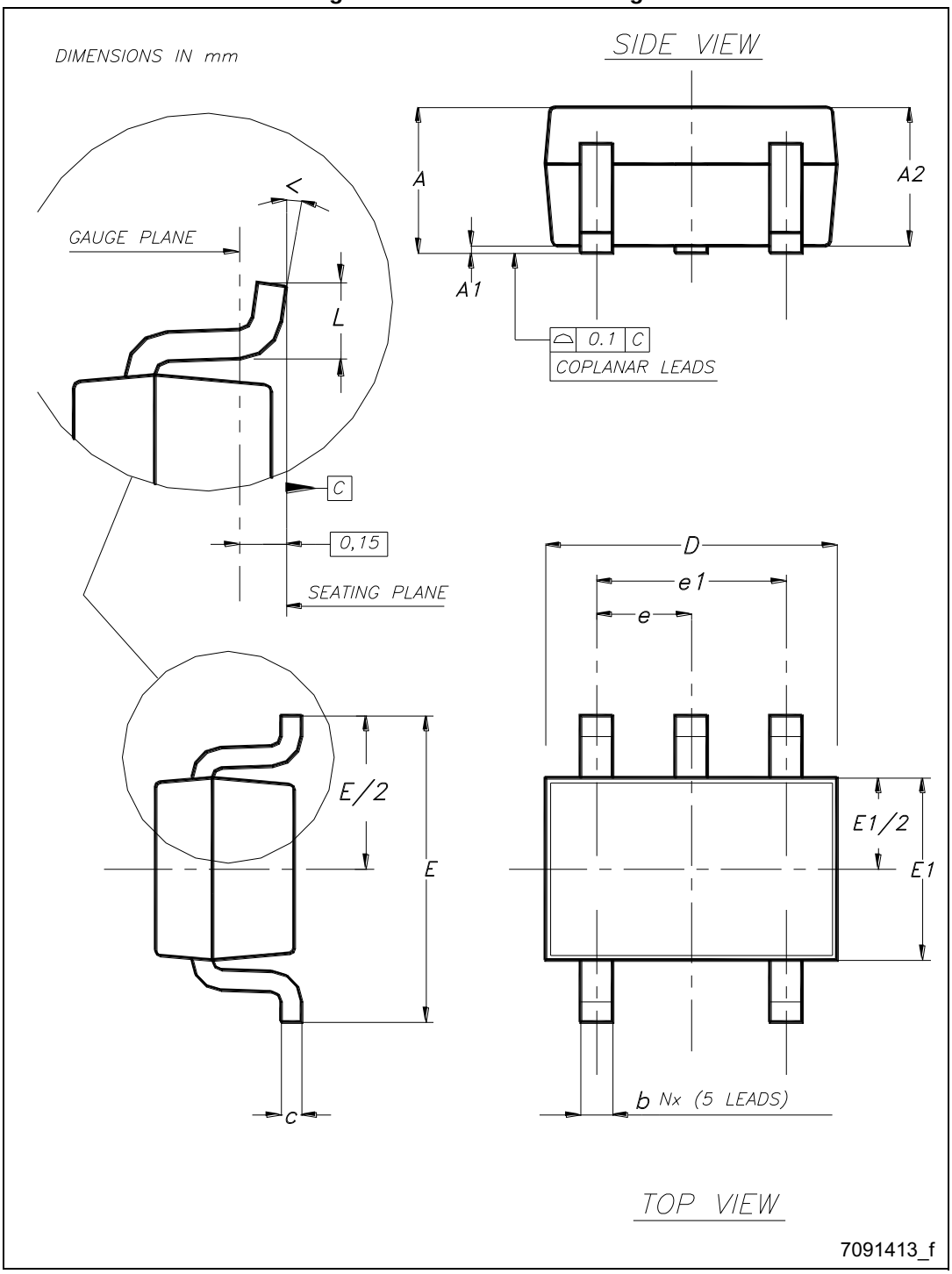


Table 6. SOT323-5L mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 0.80 | | 1.10 |
| A1 | 0 | | 0.10 |
| A2 | 0.80 | 0.90 | 1 |
| b | 0.15 | | 0.30 |
| c | 0.10 | | 0.22 |
| D | 1.80 | 2 | 2.20 |
| E | 1.80 | 2.10 | 2.40 |
| E1 | 1.15 | 1.25 | 1.35 |
| e | | 0.65 | |
| e1 | | 1.30 | |
| L | 0.26 | 0.36 | 0.46 |
| < | 0° | | 8° |

# 9 Packaging mechanical data

**Figure 19. SOT323-xL tape and reel drawing**

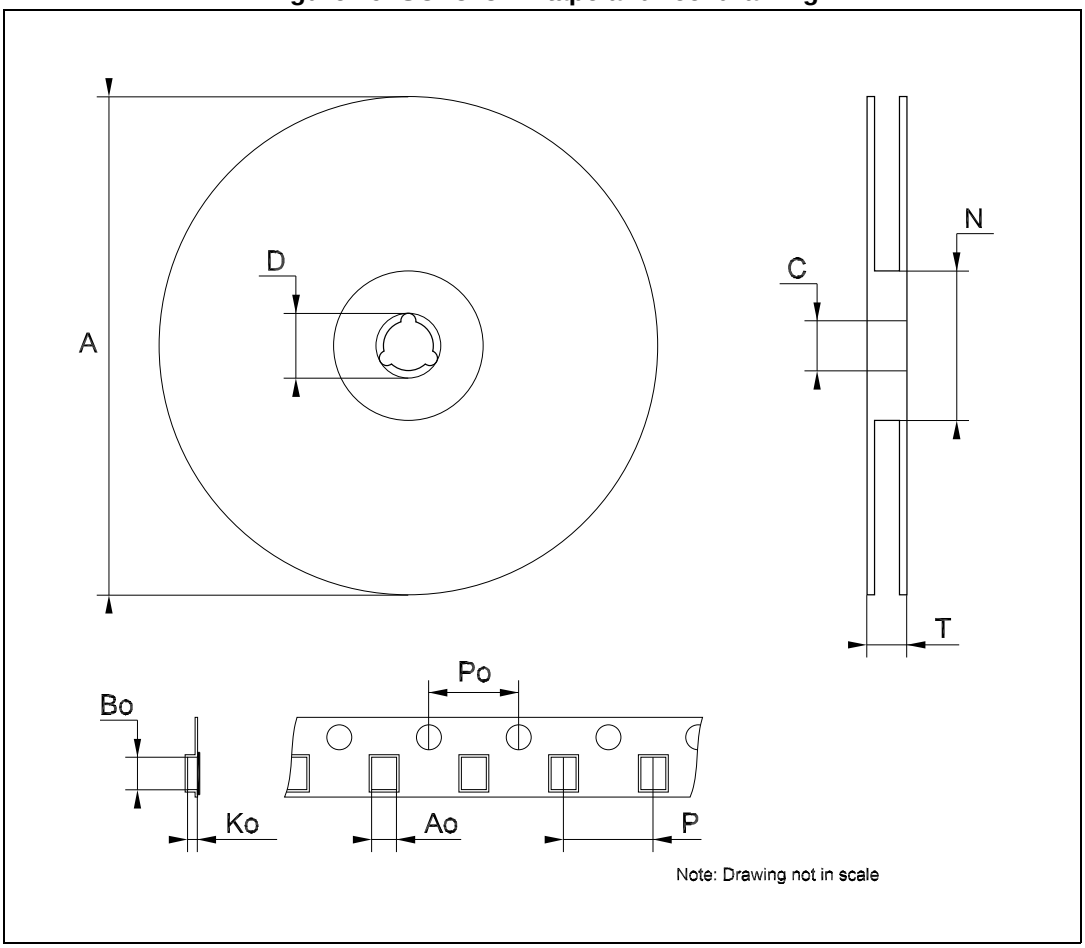


**Table 7. SOT323-xL tape and reel mechanical data**

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 175 | 180 | 185 |
| C | 12.8 | 13 | 13.2 |
| D | 20.2 | | |
| N | 59.5 | 60 | 60.5 |
| T | | | 14.4 |
| Ao | | 2.25 | |
| Bo | | 3.17 | |
| Ko | | 1.2 | |
| Po | 3.9 | 4.0 | 4.1 |
| P | 3.9 | 4.0 | 4.2 |

# 10 Revision history

**Table 8. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 07-Feb-2007 | 1 | Initial release. |
| 13-Feb-2007 | 2 | Typo in cover page 350 mA ==> 350 mV. |
| 06-Jul-2007 | 3 | Added part number. |
| 14-Nov-2007 | 4 | Added *Table 1*. |
| 31-Jan-2013 | 5 | – Modified line regulation test condition *Table 5 on page 6*.<br>– Minor text changes throughout the document. |
| 09-May-2014 | 6 | Part number STLQ50xx changed to STLQ50.<br>Removed SOT23-5L package.<br>Updated Table 1: Device summary, Section 1: Block diagram, Section 2: Pin configuration,Section 3: Maximum ratings, Section 5: Typical application, Section 7: Application information, Section 8: Package mechanical data.<br>Added Section 9: Packaging mechanical data.<br>Minor text changes. |
| 19-Jul-2019 | 7 | Added Marking in *Table 1: Device summary* on the cover page. |