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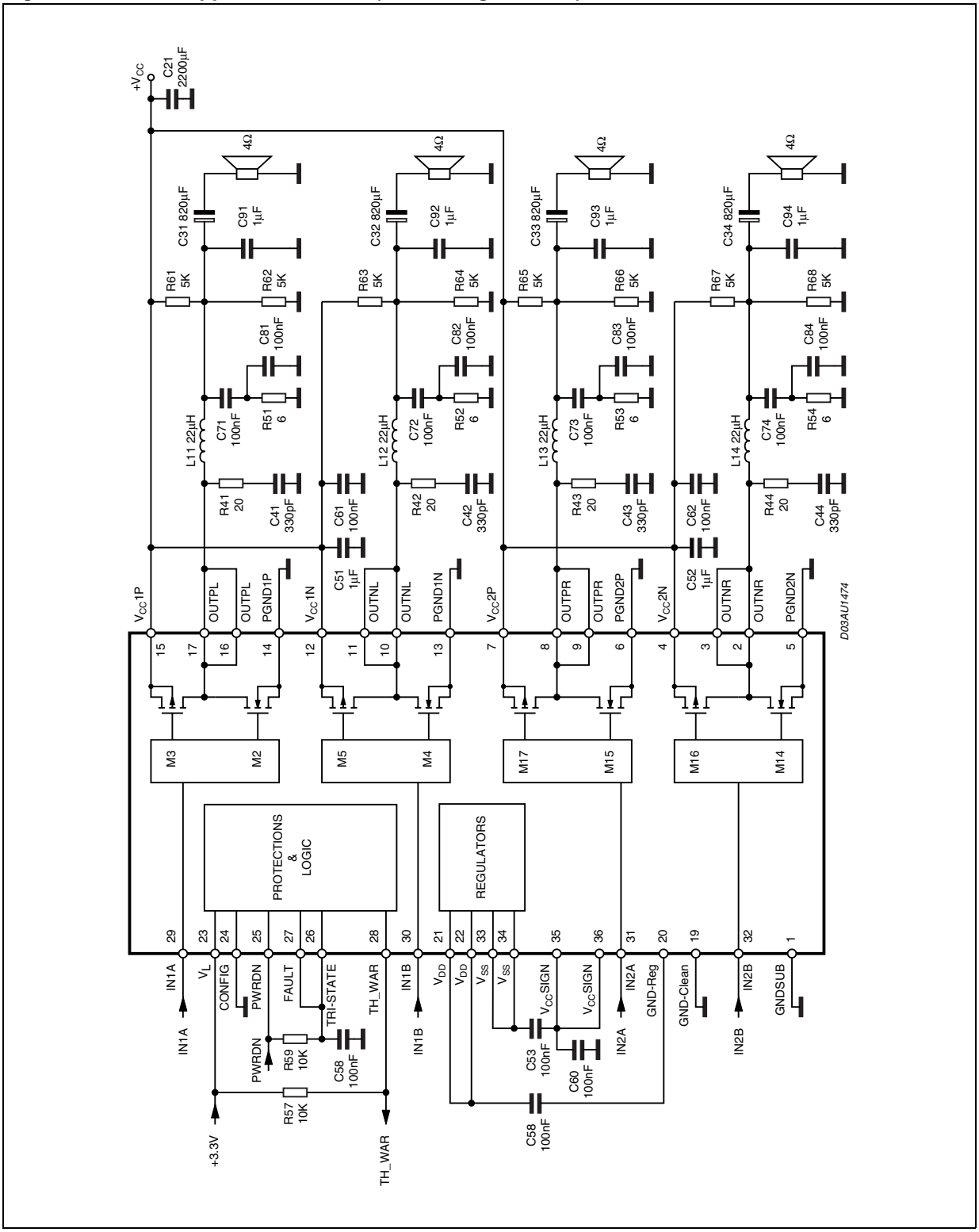
1 Audio application circuit

Figure 1. Audio application circuit (Quad single ended)



2 Pins description

Figure 2. Pin Connection (top view)

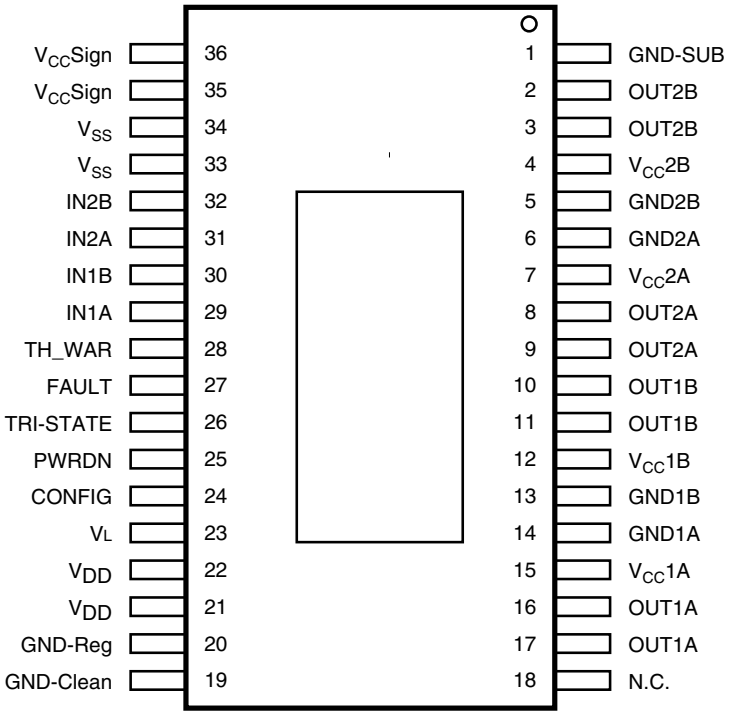


Table 1. Pin Function

N°	Pin	Description
1	GND-SUB	Substrate ground
2 ; 3	OUT2B	Output half bridge 2B
4	Vcc2B	Positive supply
5	GND2B	Negative Supply
6	GND2A	Negative Supply
7	Vcc2A	Positive supply
8 ; 9	OUT2A	Output half bridge 2A
10 ; 11	OUT1B	Output half bridge 1B
12	Vcc1B	Positive supply
13	GND1B	Negative Supply
14	GND1A	Negative Supply
15	Vcc1A	Positive supply
16 ; 17	OUT1A	Output half bridge 1A
35 ; 36	Vcc Sign	Signal Positive supply

Table 1. Pin Function (continued)

N°	Pin	Description
18	NC	Not connected
19	GND-clean	Logical ground
20	GND-Reg	Ground for regulator Vdd
21 ; 22	Vdd	5V Regulator referred to ground
23	VL	Logic Reference Voltage
24	CONFIG	Configuration pin
25	PWRDN	Stand-by pin
26	TRI-STATE	Hi-Z pin
27	FAULT	Fault pin advisor
28	TH-WAR	Thermal warning advisor
29	IN1A	Input of half bridge 1A
30	IN1B	Input of half bridge 1B
31	IN2A	Input of half bridge 2A
32	IN2B	Input of half bridge 2B
33 ; 34	Vss	5V Regulator referred to +Vcc
35 ; 36	Vcc Sign	Signal Positive supply

Table 2. Functional Pin Status

Pin Name	Pin N.	Logical value	IC - STATUS
FAULT	27	0	Fault detected (Short circuit, or Thermal.)
FAULT *	27	1	Normal Operation
TRI-STATE	26	0	All powers in Hi-Z state
TRI-STATE	26	1	Normal operation
PWRDN	25	0	Low consumption
PWRDN	25	1	Normal operation
THWAR	28	0	Temperature of the IC =130C
THWAR(1)	28	1	Normal operation
CONFIG	24	0	Normal Operation
CONFIG(2)	24	1	OUT1A=OUT1B ; OUT2A=OUT2B (IF IN1A = IN1B; IN2A = IN2B)

1. The pin is open collector. To have the high logic value, it needs to be pulled up by a resistor.
2. To put CONFIG = 1 means connect Pin 24 (CONFIG) to Pins 21, 22 (Vdd) to implemented single BTL (MONO MODE) operation for high current.

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Pin 4,7,12,15)	40	V
V_{max}	Maximum Voltage on pins 23 to 32	5.5	V
T_{op}	Operating Temperature Range	-40 to 90	°C
P_{tot}	Power Dissipation (Tcase = 70°C)	21	W
T_{stg}, T_j	Storage and Junction Temperature	-40 to 150	°C

3.2 Recommended operating conditions

Table 4. Recommended operating conditions (*)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	DC Supply Voltage	10		36.0	V
V_L	Input Logic Reference	2.7	3.3	5.0	V
T_{amb}	Ambient Temperature	0		70	°C

(*) performances not guaranteed beyond recommended operating conditions

3.3 Thermal data

Table 5. Thermal data (*)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$T_{j\text{-}case}$	Thermal Resistance Junction to Case (thermal pad)			1.5	°C/W
T_{jSD}	Thermal shut-down junction temperature		150		°C
T_{warn}	Thermal warning temperature		130		°C
t_{hSD}	Thermal shut-down hysteresis		25		°C

(*) see Thermal information

3.4 Thermal information

The power dissipated within the device depends primarly on the supply voltage, load impedance and output modulation level. The PSSO36 Package of the STA518 includes an exposed thermal slug on the top of the device to provide a direct thermal path from the IC to the heatsink. For the Quad single ended application the Dissipated Power vs Ouptut Power is shown in *Figure 10*.

Considering that for the STA518 the Thermal resistance Junction to slug is 1.5°C/W and the extimated Thermal resistance due to the grease placed between slug and heat sink is 2.3°C/W (the use of thermal pads for this package is not recommended), the suitable Heat Sink Rth to be used can be drawn from the following graph *Figure 11*, where is shown the Derating Power vs.Tambient for different heatsinkers.

3.5 Electrical characteristcs

Table 6. Electrical Characteristcs

Refer to circuit in *Figure 3* (V_L = 3.3V; V_{CC} = 30V; R_L = 8Ω; f_{sw} = 384KHz; T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_{dsON}	Power Pchannel/Nchannel MOSFET RdsON	I_d = 1A		200	270	mΩ
I_{dss}	Power Pchannel/Nchannel leakage Idss	V_{CC} = 35V			50	µA
g_N	Power Pchannel RdsON Matching	I_d = 1A	95			%
g_P	Power Nchannel RdsON Matching	I_d = 1A	95			%
Dt_s	Low current Dead Time (static)	see test circuit *Figure 3*		10	20	ns
Dt_d	High current Dead Time (dinamic)	L = 22µH; C = 470nF; R_L = 8 Ω I_d = 3A; see*Figure 5*			50	ns
$t_{d\ ON}$	Turn-on delay time	Resistive load; V_{CC} = 30V			100	ns
$t_{d\ OFF}$	Turn-off delay time	Resistive load; V_{CC} = 30V			100	ns
t_r	Rise time	Resistive load; as *Figure 3*			25	ns
t_f	Fall time				25	ns
V_{CC}	Supply voltage operating voltage		10		36	V
V_{IN-H}	High level input voltage				V_L/2 +300mV	V
V_{IN-L}	Low level input voltage		V_L/2 - 300mV			V
I_{IN-H}	Hi level Input current	Pin voltage = V_L		1		µA
I_{IN-L}	Low level input current	Pin voltage = 0.3V		1		µA
$I_{PWRDN-H}$	Hi level PWRDN pin input current	V_L = 3.3V		35		µA
V_{LOW}	Low logical state voltage VLow (pin PWRDN, TRISTATE) (1)	V_L = 3.3V	0.8			V
V_{HIGH}	High logical state voltage VHigh (pin PWRDN, TRISTATE) (1)	V_L = 3.3V			1.7	V
$I_{VCC-PWRDN}$	Supply current from Vcc in Power Down	PWRDN = 0			3	mA

Table 6. Electrical Characteristcs (continued)
Refer to circuit in *Figure 3* (V_L = 3.3V; V_{CC} = 30V; R_L = 8Ω; f_{sw} = 384KHz; T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{FAULT}	Output Current pins FAULT -TH-WARN when FAULT CONDITIONS	Vpin = 3.3V		1		mA
$I_{VCC-hiz}$	Supply current from Vcc in Tri-state	V_{CC} = 30V; Tri-state = 0		22		mA
I_{VCC}	Supply current from V_{CC} in operation (both channel switching)	V_{CC} = 30V; Input pulse width = 50% Duty; Switching Frequency = 384kHz; No LC filters;		50		mA
I_{VCC-q}	Isc (short circuit current limit) (2)	V_{CC} = 30V	3.5	6		A
V_{UV}	Undervoltage protection threshold			7		V
t_{pw_min}	Output minimum pulse width	No Load	70		150	ns

1. The *Table 7* explains the V_{LOW}, V_{HIGH} variation with Ibias.
2. See relevant Application Note AN1994

Table 7. V_{LOW}, V_{HIGH} variation with I_{bias}

V_L	$V_{Low\ min}$	$V_{High\ max}$	Unit
2.7	0.7	1.5	V
3.3	0.8	1.7	V
5	0.85	1.85	V

Table 8. Logic Truth Table (see *Figure 4*)

TRI-STATE	INxA	INxB	Q1	Q2	Q3	Q4	OUTPUT MODE
0	x	x	OFF	OFF	OFF	OFF	Hi-Z
1	0	0	OFF	OFF	ON	ON	DUMP
1	0	1	OFF	ON	ON	OFF	NEGATIVE
1	1	0	ON	OFF	OFF	ON	POSITIVE
1	1	1	ON	ON	OFF	OFF	Not used

Figure 3. Low current dead time for Single End application: test circuit.

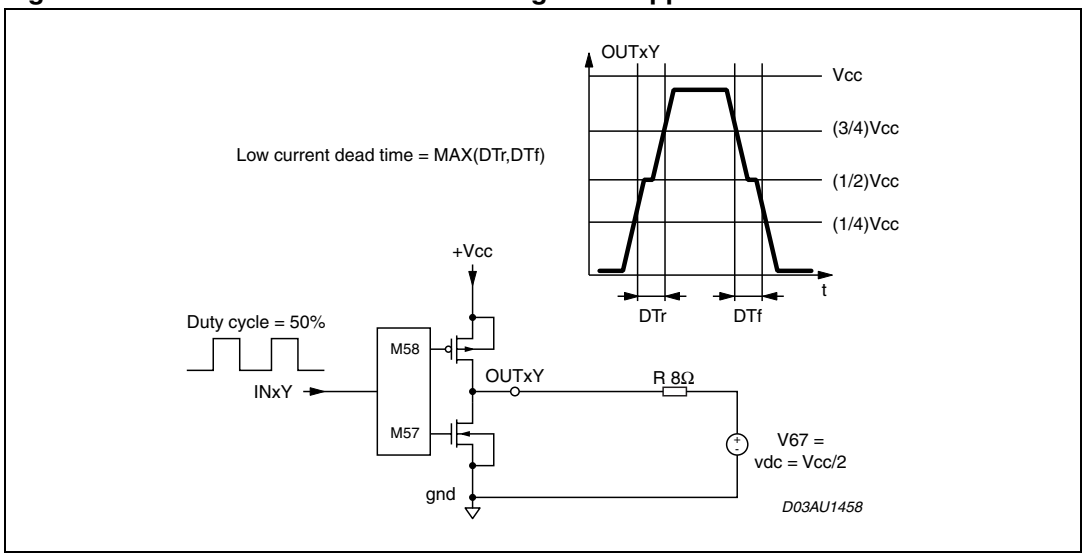


Figure 4. High current dead time for Bridge application: block diagram

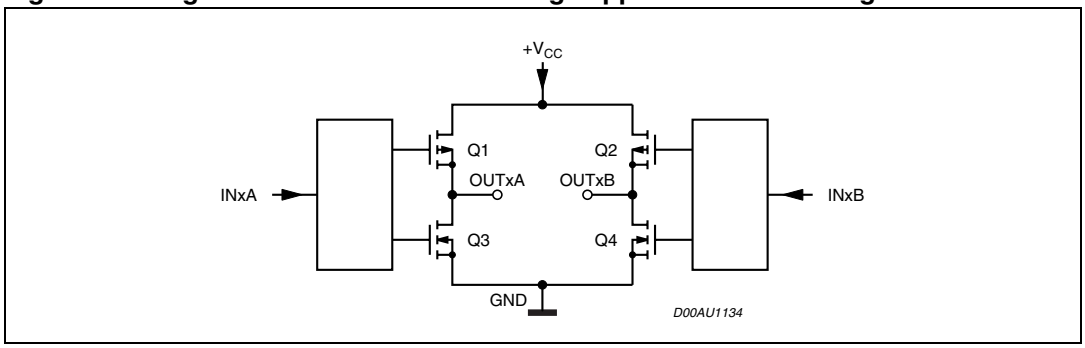
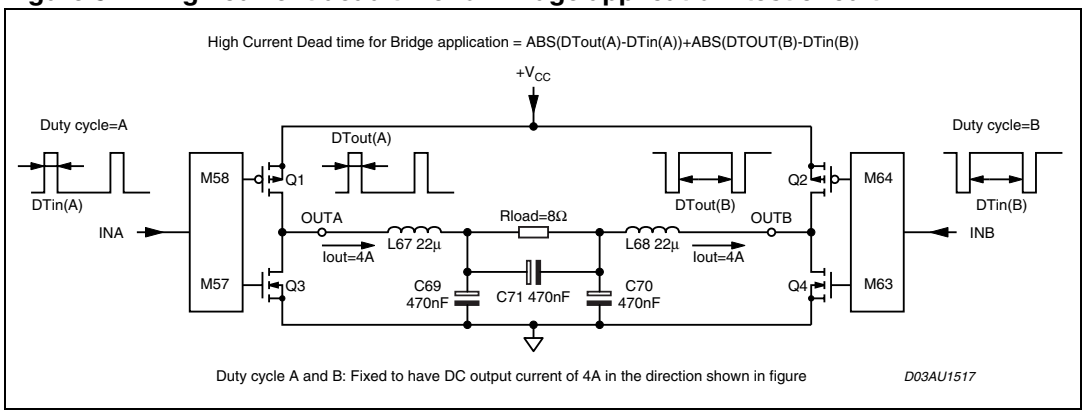


Figure 5. High current dead time for Bridge application: test circuit



4 Technical information

The STA518 is a dual channel H-Bridge that is able to deliver 50W per channel (@ THD=10% R_L = 8Ω, V_{CC} = 29V) of audio output power in high efficiency.

The STA518 converts both DDX and binary-controlled PWM signals into audio power at the load. It includes a logic interface , integrated bridge drivers, high efficiency MOSFET outputs and thermal and short circuit protection circuitry.

In DDX mode, two logic level signals per channel are used to control high-speed MOSFET switches to connect the speaker load to the input supply or to ground in a Bridge configuration, according to the damped ternary Modulation operation.

In Binary Mode operation , both Full Bridge and Half Bridge Modes are supported. The STA518 includes over-current and thermal protection as well as an under-voltage

Lockout with automatic recovery. A thermal warning status is also provided.

Figure 6. STA518 Block Diagram Full-Bridge DDX® or Binary Modes

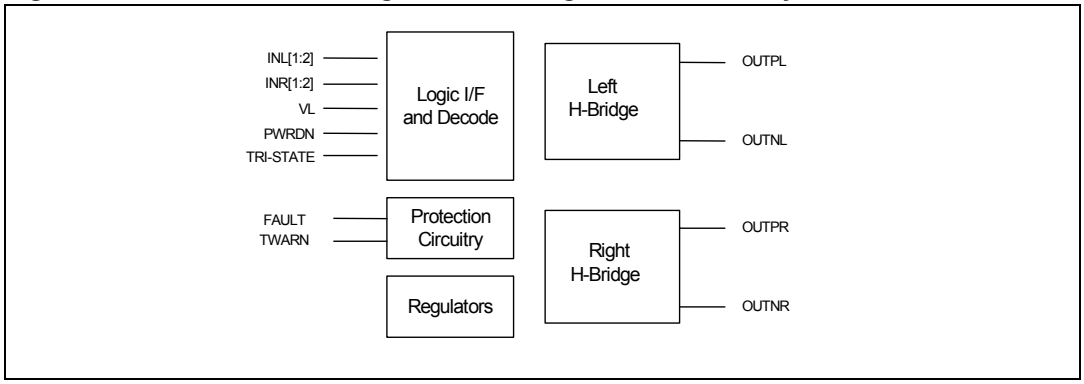
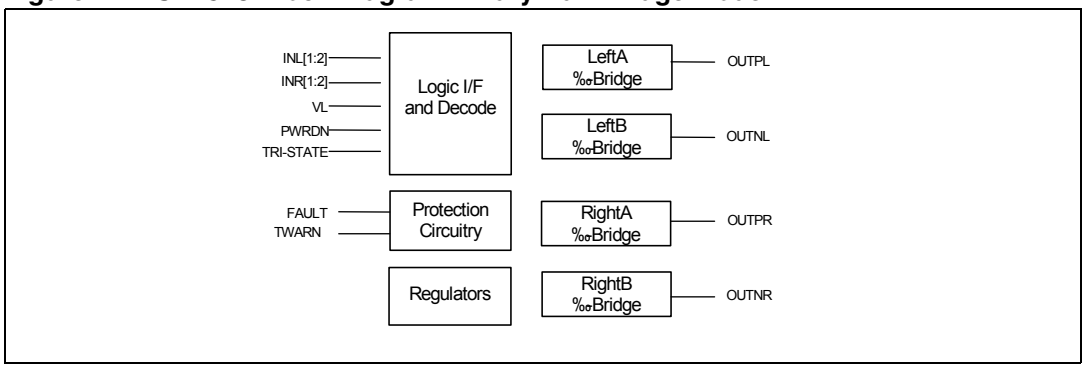


Figure 7. STA518 Block Diagram Binary Half-Bridge Mode



4.1 Logic interface and decode:

The STA518 power outputs are controlled using one or two logic level timing signals. In order to provide a proper logic interface, the Vbias input must operate at the dame voltage as the DDX control logic supply.

Protection circuitry:

The STA518 includes protection circuitry for over-current and thermal overload conditions. A thermal warning pin (pin.28) is activated low (open drain MOSFET) when the IC temperature exceeds 130°C, in advance of the thermal shutdown protection. When a fault condition is detected , an internal fault signal acts to immediately disable the output power MOSFETs, placing both H-Bridges in high impedance state. At the same time an open-drain MOSFET connected to the fault pin (pin.27) is switched on.

There are two possible modes subsequent to activating a fault:

1. **SHUTDOWN mode**: with FAULT (pull-up resistor) and TRI-STATE pins independent, an activated fault will disable the device, signaling low at the FAULT output.
   The device may subsequently be reset to normal operation by toggling the TRI-STATE pin from High to Low to High using an external logic signal.
2. **AUTOMATIC recovery mode:** This is shown in the Audio Application Circuit of Quad single Ended). The FAULT and TRI-STATE pins are shorted together and connected to a time constant circuit comprising R59 and C58.
   An activated FAULT will force a reset on the TRI-STATE pin causing normal operation to resume following a delay determined by the time constant of the circuit.
   If the fault condition is still present , the circuit operation will continue repeating until the fault condition is removed .
   An increase in the time constant of the circuit will produce a longer recovery interval. Care must be taken in the overall system design as not to exceed the protection thesholds under normal operation.

4.2 Power outputs:

The STA518 power and output pins are duplicated to provide a low impedance path for the device's bridged outputs. All duplicate power, ground and output pins must be connected for proper operation.

The PWRDN or TRI-STATE pins should be used to set all MOSFETS to the Hi-Z state during power-up until the logic power supply, V_L , is settled.

4.3 Parallel output / high current operation:

When using DDX Mode output , the STA518 outputs can be connected in parallel in order to increase the output current capability to a load. In this configuration the STA518 can provide 70W into 8 ohm.

This mode of operation is enabled with the CONFIG pin (pin.24) connected to VREG1 and the inputs combined INLA=INLB, INRA=INRB and the outputs combined OUTLA=OTLB, OUTRA=OUTRB.

4.4 Additional informations:

Output Filter: A passive 2nd-order passive filter is used on the STA518 power outputs to reconstruct an analog Audio Signal . System performance can be significantly affected by the output filter design and choice of passive components. A filter design for 6ohm/8ohm loads is shown in the Typical Application circuit of *Figure 9*.

Quad Single ended circuit (*Figure 1*) shows a filter for ½ bridge mode, 4 ohm loads.

Figure 8. Typical Stereo Full Bridge Configuration to Obtain 50+50W @ THD = 10%, R_L = 8Ω, V_{CC} =29V

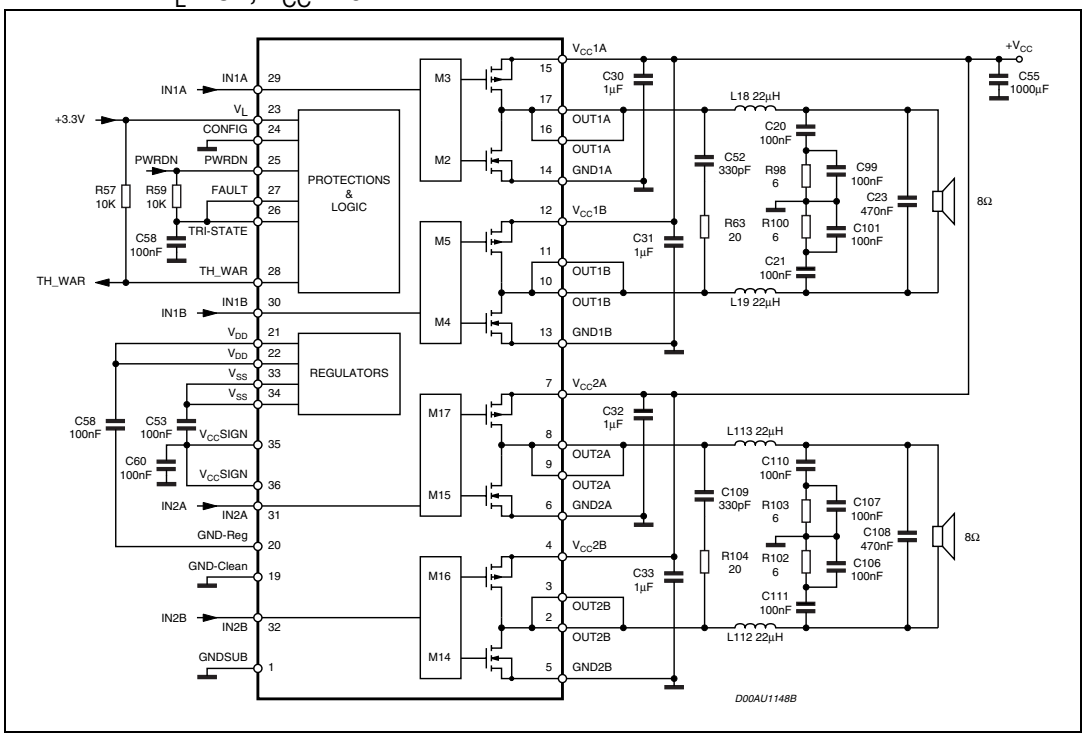
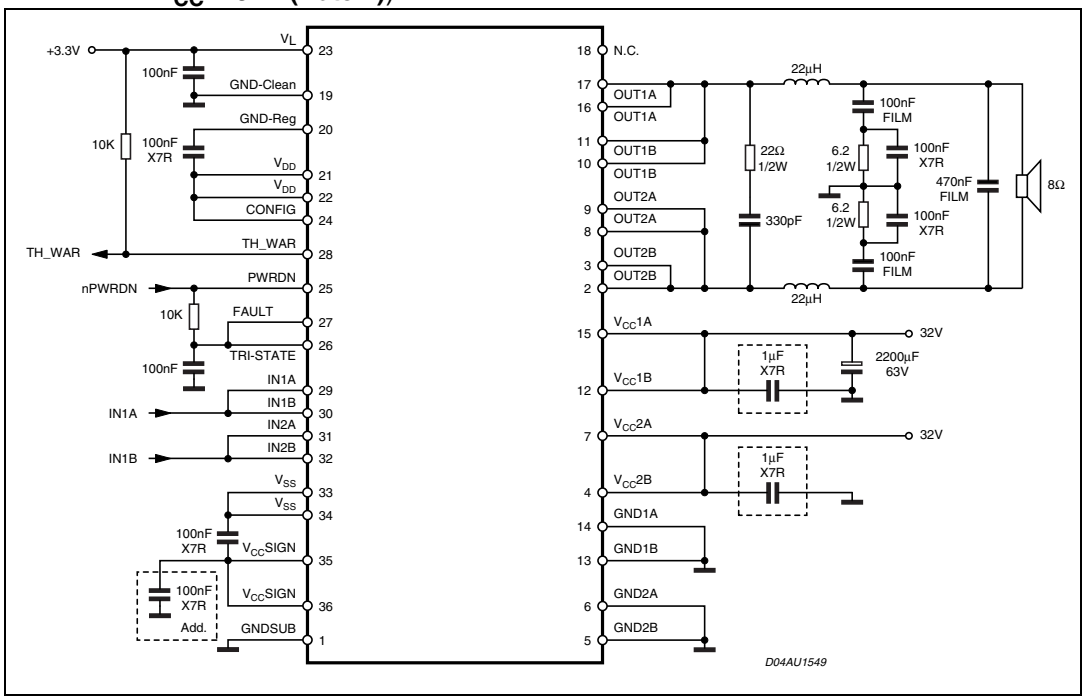


Figure 9. Typical Single BTL Configuration to Obtain 70W @ THD 10%, R_L = 8Ω, V_{CC} = 34V (note 1))



Note: 1 "A PWM modulator as driver is needed . In particular, this result is performed using the STA308+STA518+STA50X demo board". Peak Power for t ≤1sec

5 Characterization curves

The following characterization are obtained using the quad single ended configuration (*Figure 1*) with STA308A controller

Figure 10. Power Dissipation vs Output Power

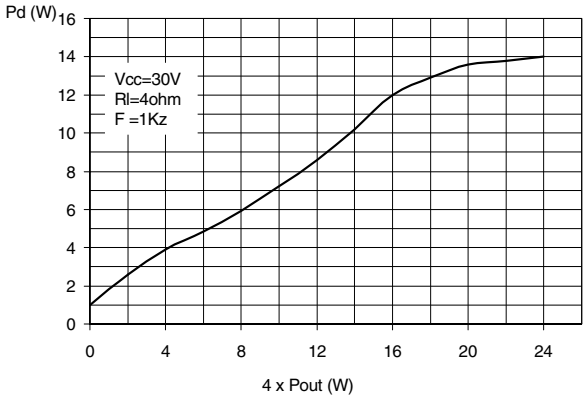


Figure 11. Power Derating Curve

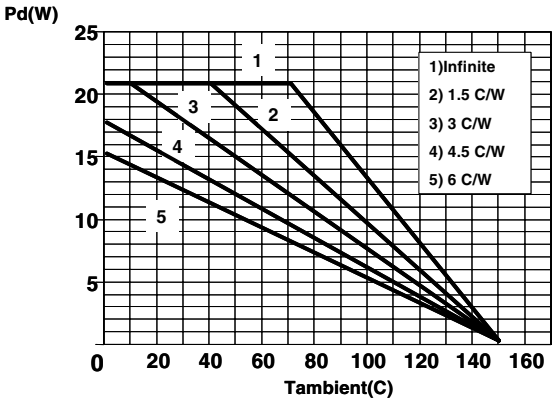


Figure 12. THD+N vs Output Power

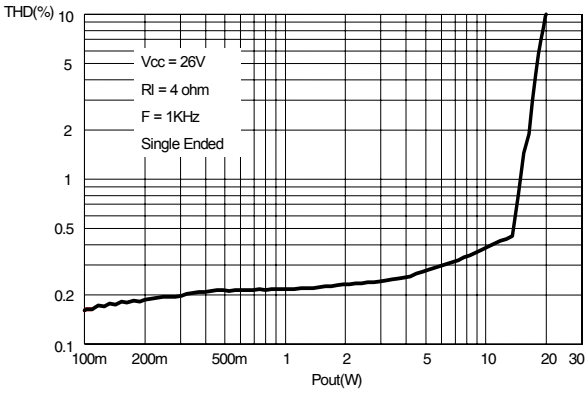


Figure 13. Output Power vs Supply Voltage

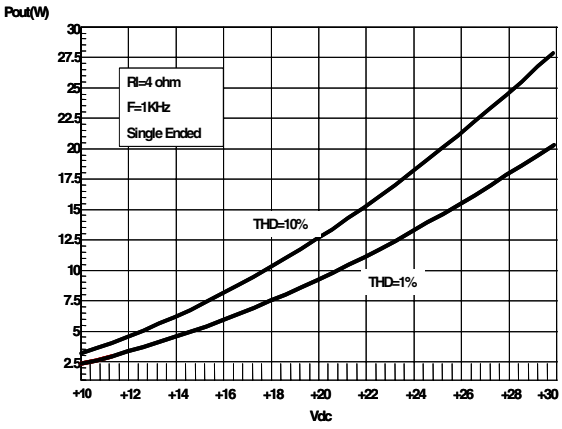
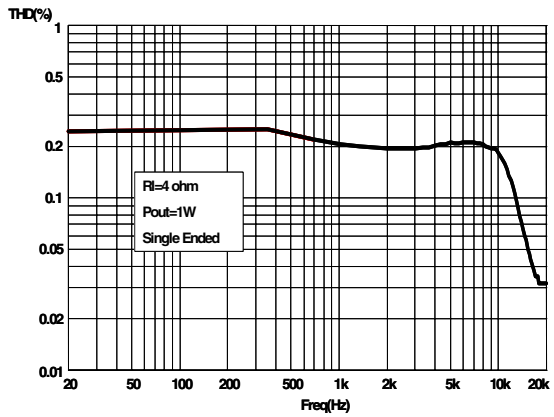


Figure 14. THD vs Frequency



The following characterizations are obtained using the stereo full bridge configuration (*Figure 8*) with STA308A controller.

Figure 15. Output Power vs Supply Voltage

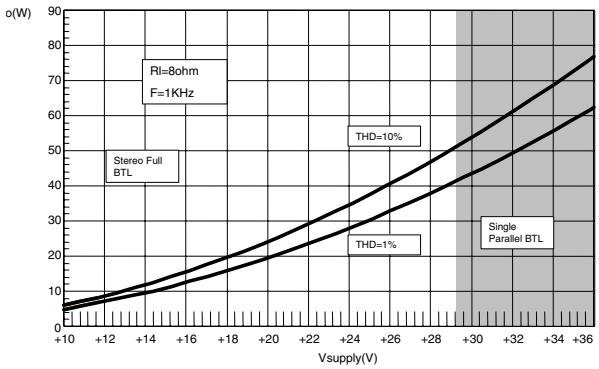


Figure 16. THD+N vs Output Power

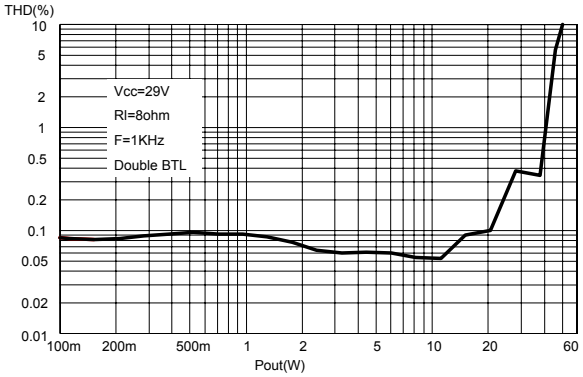
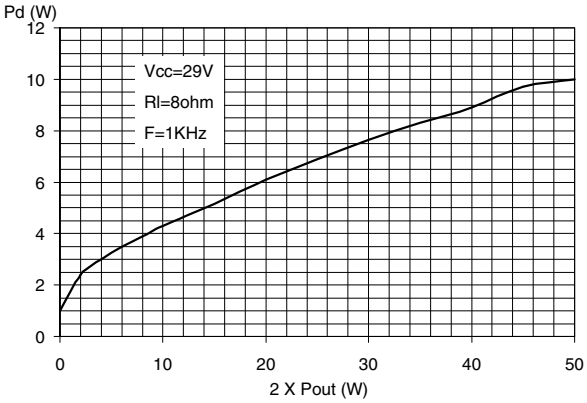
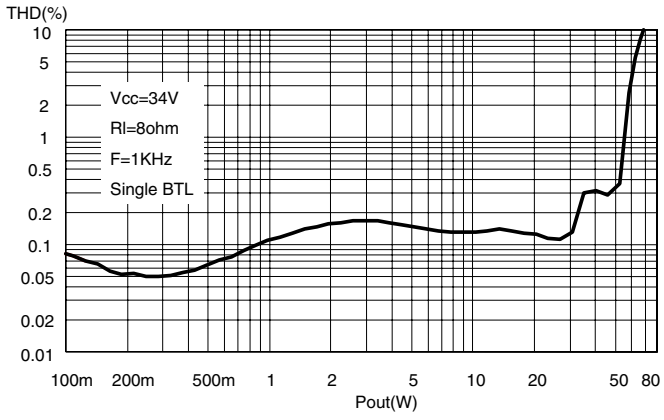


Figure 17. Power Dissipation vs Output Power



The following characterizations are obtained using the single BTL configuration (*Figure 9*) with STA308A controller.

Figure 18. THD+N vs Output Power



6 Package information

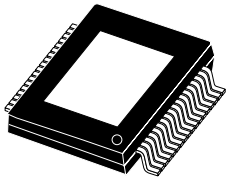
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 19. PSSO36 (Slug Up) Mechanical Data & Package Dimensions

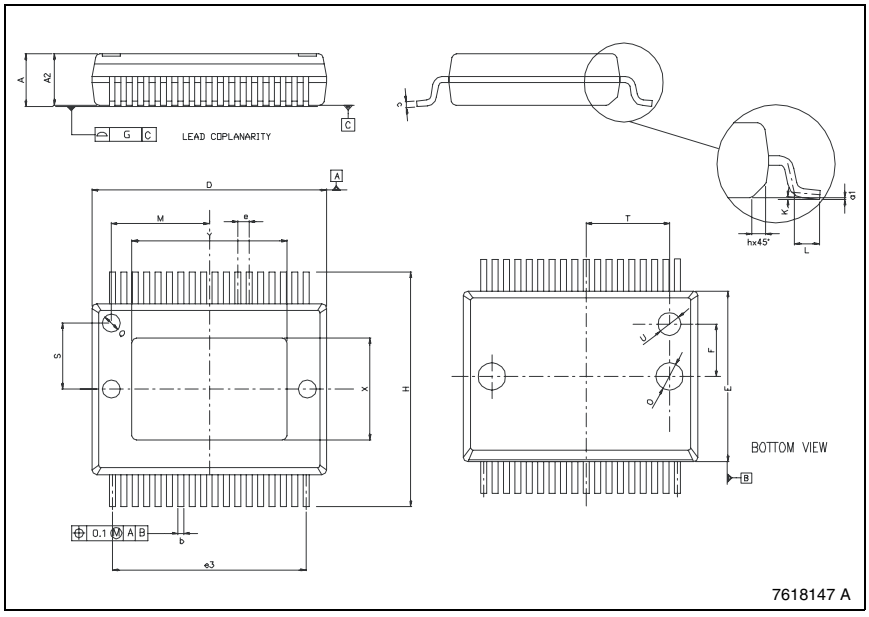
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.15		2.47	0.084		0.097
A2	2.15		2.40	0.084		0.094
a1	0		0.075	0		0.003
b	0.18		0.36	0.007		0.014
c	0.23		0.32	0.009		0.012
D (1)	10.10		10.50	0.398		0.413
E (1)	7.4		7.6	0.291		0.299
e		0.50			0.020	
e3		8.50			0.035	
F		2.3			0.090	
G			0.10			0.004
G1			0.06			0.002
H	10.10		10.50	0.398		0.413
h			0.40			0.016
L	0.55		0.85	0.022		0.033
M		4.3			0.169	
N	10° (max)					
O		1.2			0.047	
Q		0.8			0.031	
S		2.9			0.114	
T		3.65			0.144	
U		1.0			0.039	
X	4.10		4.70	0.161		0.185
Y	6.50		7.10	0.256		0.279

(1) "D and E" do not include mold flash or protusions.
Mold flash or protusions shall not exceed 0.15mm (0.006")
(2) No intrusion allowed inwards the leads.
(3) Flash or bleeds on exposed die pad shall not exceed 0.4 mm per side

OUTLINE AND MECHANICAL DATA



PowerSSO-36 (slug-up)



7 Revision history

Table 9. Document revision history

Date	Revision	Changes
19-Aug-2004	1	Initial release.
11-Nov-2004	2	Changed symbol in “Electrical Characteristics”.
18-May-2006	3	Changed operating temperature range value to -40 to 90°C (see *Table 3*).

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