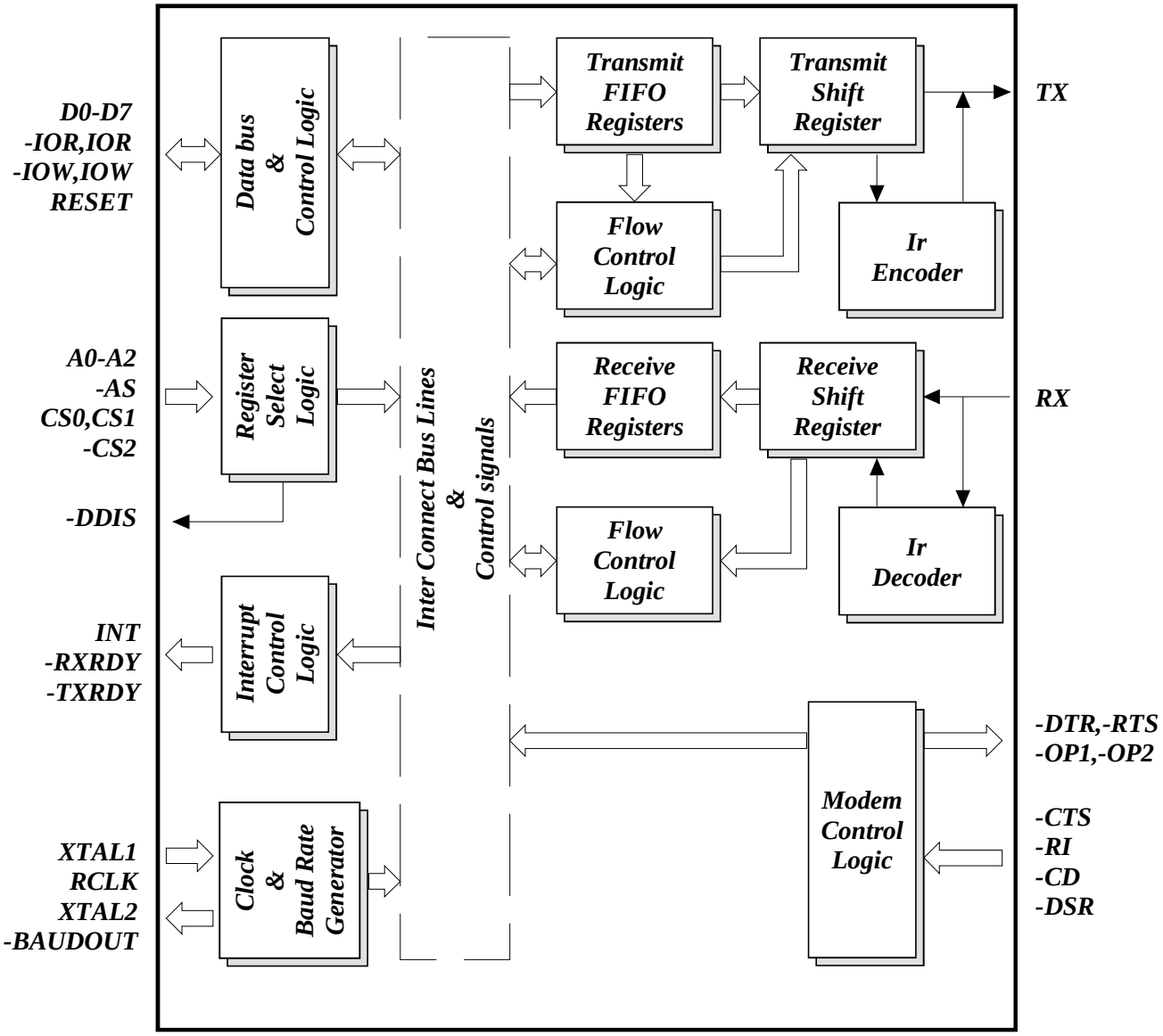
**Figure 2, BLOCK DIAGRAM**



## SYMBOL DESCRIPTION

| Symbol | Pin 48 | Signal type | Pin Description |
|---|---|---|---|
| A0 | 28 | I | Address-0 Select Bit - Internal registers address selection. |
| A1 | 27 | I | Address-1 Select Bit Internal registers address selection. |
| A2 | 26 | I | Address-2 Select Bit Internal registers address selection. |
| IOR | 20 | I | Read strobe. Its function is the same as -IOR (see -IOR), except it is active high. Either an active -IOR or IOR is required to transfer data from 580 to CPU during a read operation. |
| CS0 | 9 | I | Chip Select-0. A logical 1 on this pin provides the chip select 0 function. |
| CS1 | 10 | I | Chip Select-1. A logical 1 on this pin provides the chip select 1 function. |
| -CS2 | 11 | I | Chip Select -2. A logical 0 on this pin provides the chip select 2 function. |
| IOW | 17 | I | Write strobe. A logic 1 transition creates a write strobe. Its function is the same as -IOW (see -IOW), but it acts as an active high input signal. Either -IOW or IOW is required to transfer data from the CPU to 580 during a write operation. |
| -AS | 24 | I | Address Strobe. A logic 1 transition on -AS latches the state of the chip selects and the register select bits, A0-A2. This input is used when address and chip selects are not stable for the duration of a read or write operation, i.e., a microprocessor that needs to de-multiplex the address and data bits. If not required, the -AS input can be permanently tied to a logic 0 (it is edge triggered). |
| D0-D7 | 43-47<br>2-4 | I/O | Data Bus (Bi-directional) - These pins are the eight bit, three state data bus for transferring information to or from the controlling CPU. D0 is the least significant bit and the first data bit in a transmit or receive serial data stream. |
| GND | 18 | Pwr | Signal and Power Ground. |

## SYMBOL DESCRIPTION

| Symbol | Pin 48 | Signal type | Pin Description |
|---|---|---|---|
| -IOR | 19 | I | Read strobe (active low strobe). A logic 0 on this pin transfers the contents of the 580 data bus to the CPU. |
| -IOW | 16 | I | Write strobe (active low strobe) - A logic 0 on this pin transfers the contents of the CPU data bus to the addressed internal register. |
| INT | 30 | O | Interrupt Request. |
| -RXRDY | 29 | O | Receive Ready. A logic 0 indicates receive data ready status, i.e. the RHR is full or the FIFO has one or more RX characters available for unloading. This pin goes to a logic 0 when the FIFO/RHR is full or when there are more characters available in either the FIFO or RHR. |
| -TXRDY | 23 | O | Transmit Ready. Buffer ready status is indicated by a logic 0, i.e., at least one location is empty and available in the FIFO or THR. This pin goes to a logic 1 when there are no more empty locations in the FIFO or THR. |
| -BAUDOUT | 12 | O | Baud Rate Generator Output. This pin provides the 16X clock of the selected data rate from the baud rate generator. The RCLK pin must be connected externally to -BAUDOUT when the receiver is operating at the same data rate. |
| -DDIS | 22 | O | Drive Disable. This pin goes to a logic 0 when the external CPU is reading data from the 580. This signal can be used to disable external transceivers or other logic functions. |
| -OP1 | 34 | O | Output-1 (User Defined) - See bit-2 of modem control register (MCR bit-2). |
| -OP2 | 31 | O | Output-2 (User Defined). This pin provides the user a general purpose output. See bit-3 modem control register (MCR bit-3). |
| RCLK | 5 | I | Receive Clock Input. This pin is used as external 16X clock input to the receiver section. External connection to -Baudout pin is required in order to utilize the internal baud rate generator. |

## SYMBOL DESCRIPTION

| Symbol | Pin 48 | Signal type | Pin Description |
|---|---|---|---|
| RESET | 35 | I | Reset. (active high) - A logic 1 on this pin will reset the internal registers and all the outputs. The UART transmitter output and the receiver input will be disabled during reset time. (See ST16C580 External Reset Conditions for initialization details.) |
| VCC | 42 | Pwr | Power Supply Input. |
| XTAL1 | 14 | I | Crystal or External Clock Input - Functions as a crystal input or as an external clock input. A crystal can be connected between this pin and XTAL2 to form an internal oscillator circuit. An external 1 M□ resistor is required between the XTAL1 and XTAL2 pins (see figure 9). Alternatively, an external clock can be connected to this pin to provide custom data rates (Programming Baud Rate Generator section). |
| XTAL2 | 15 | O | Output of the Crystal Oscillator or Buffered Clock - (See also XTAL1). Crystal oscillator output or buffered clock output. |
| -CD | 40 | I | Carrier Detect (active low) - A logic 0 on this pin indicates that a carrier has been detected by the modem. |
| -CTS | 38 | I | Clear to Send (active low) - A logic 0 on the -CTS pin indicates the modem or data set is ready to accept transmit data from the 580. Status can be tested by reading MSR bit-4. This pin only affects the transmit and receive operations when Auto CTS function is enabled via the Enhanced Feature Register (EFR) bit-7, for hardware flow control operation. |
| -DSR | 39 | I | Data Set Ready (active low) - A logic 0 on this pin indicates the modem or data set is powered-on and is ready for data exchange with the UART. This pin has no effect on the UART's transmit or receive operation. |
| -DTR | 33 | O | Data Terminal Ready (active low) - A logic 0 on this pin indicates that the 580 is powered-on and ready. This pin can be controlled via the modem control register. Writing a logic 1 to MCR bit-0 will set the -DTR output to logic 0, enabling the modem. This pin will be a logic 1 after writing a logic 0 to MCR bit-0, or after a reset. This pin has no effect on the UART's transmit or receive operation. |

## SYMBOL DESCRIPTION

| Symbol | Pin 48 | Signal type | Pin Description |
|---|---|---|---|
| -RI | 41 | I | Ring Indicator (active low) - A logic 0 on this pin indicates the modem has received a ringing signal from the telephone line. A logic 1 transition on this input pin will generate an interrupt. |
| -RTS | 32 | O | Request to Send (active low) - A logic 0 on the -RTS pin indicates the transmitter has data ready and waiting to send. Writing a logic 1 in the modem control register (MCR bit-1) will set this pin to a logic 0 indicating data is available. After a reset this pin will be set to a logic 1. This pin only affects the transmit and receive operations when Auto RTS function is enabled via the Enhanced Feature Register (EFR) bit-6, for hardware flow control operation. |
| RX/IRRX | 7 | I | Receive Data - This pin provides the serial receive data input to the 580. Two user selectable interface options are available. The first option supports the standard modem interface. The second option provides an Infrared decoder interface, see figures 2/3. When using the standard modem interface, the RX signal will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. The inactive state (no data) for the Infrared decoder interface is a logic 0. MCR bit-6 selects the standard modem or infrared interface. During the local loopback mode, the RX input pin is disabled and TX data is internally connected to the UART RX Input, internally, see figure 12. |
| TX/IRTX | 8 | O | Transmit Data - This pin provides the serial transmit data from the 580. Two user selectable interface options are available. The first user option supports a standard modem interface. The second option provides an Infrared encoder interface, see figures 2/3. When using the standard modem interface, the TX signal will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. The inactive state (no data) for the Infrared encoder/ decoder interface is a Logic 0. MCR bit-6 selects the standard modem or infrared interface. During the local loop-back mode, the TX input pin is disabled and TX data is internally connected to the UART RX Input, see figure 12. |

## GENERAL DESCRIPTION

The 580 provides serial asynchronous receive data synchronization, parallel-to-serial and serial-to-parallel data conversions for both the transmitter and receiver sections. These functions are necessary for converting the serial data stream into parallel data that is required with digital data systems. Synchronization for the serial data stream is accomplished by adding start and stops bits to the transmit data to form a data character (character orientated protocol). Data integrity is insured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors. The electronic circuitry to provide all these functions is fairly complex especially when manufactured on a single integrated silicon chip. The ST16C580 represents such an integration with greatly enhanced features. The 580 is fabricated with an advanced CMOS process.

The 580 is an upward solution that provides 16 bytes of transmit and receive FIFO memory, instead of 16 bytes provided in the 16C550, or none in the 16C450. The 580 is designed to work with high speed modems and shared network environments, that require fast data processing time. Increased performance is realized in the 580 by the larger transmit and receive FIFO's. This allows the external processor to handle more networking tasks within a given time. In addition, the 4 selectable levels of FIFO trigger interrupt and automatic hardware/software flow control is uniquely provided for maximum data throughput performance especially when operating in a multi-channel environment. The combination of the above greatly reduces the bandwidth requirement of the external controlling CPU, increases performance, and reduces power consumption.

The 580 is capable of operation to 1.5Mbps with a 24 MHz crystal or external clock input.
With a crystal of 7.3728 MHz and through a software option, the user can select data rates up to 460.8Kbps.

The rich feature set of the 580 is available through internal registers. Automatic hardware/software flow control, selectable transmit and receive FIFO trigger levels, selectable TX and RX baud rates, infrared encoder/decoder interface, modem interface controls, and a sleep mode are all standard features. Following a power on reset or an external reset, the 580 is software compatible with previous generation of UARTs, 16C450 and 16C550.

## FUNCTIONAL DESCRIPTIONS

### Internal Registers

The 580 provides 15 internal registers for monitoring and control. These registers are shown in Table 3 below. Twelve registers are similar to those already available in the standard 16C550. These registers function as data holding registers (THR/RHR), interrupt status and control registers (IER/ISR), a FIFO control register (FCR), line status and control registers, (LCR/LSR), modem status and control registers (MCR/MSR), programmable data rate (clock) control registers (DLL/DLM), and a user assessable scratchpad register (SPR). Beyond the general 16C550 features and capabilities, the 580 offers an enhanced feature register set (EFR, Xon/Xoff 1-2) that provides on board hardware/software flow control. Register functions are more fully described in the following paragraphs.

### Table 3, INTERNAL REGISTER DECODE

| A2 | A1 | A0 | READ MODE | WRITE MODE |
|---|---|---|---|---|
| **General Register Set (THR/RHR, IER/ISR, MCR/MSR, LCR/LSR, SPR):** | | | | |
| 0 | 0 | 0 | Receive Holding Register | Transmit Holding Register |
| 0 | 0 | 1 | | Interrupt Enable Register |
| 0 | 1 | 0 | Interrupt Status Register | FIFO Control Register |
| 0 | 1 | 1 | | Line Control Register |
| 1 | 0 | 0 | | Modem Control Register |
| 1 | 0 | 1 | Line Status Register | |
| 1 | 1 | 0 | Modem Status Register | |
| 1 | 1 | 1 | Scratchpad Register | Scratchpad Register |
| **Baud Rate Register Set (DLL/DLM): Note *3** | | | | |
| 0 | 0 | 0 | LSB of Divisor Latch | LSB of Divisor Latch |
| 0 | 0 | 1 | MSB of Divisor Latch | MSB of Divisor Latch |
| **Enhanced Register Set (EFR, Xon/off 1-2): Note *4** | | | | |
| 0 | 1 | 0 | Enhanced Feature Register | Enhanced Feature Register |
| 1 | 0 | 0 | Xon-1 Word | Xon-1 Word |
| 1 | 0 | 1 | Xon-2 Word | Xon-2 Word |
| 1 | 1 | 0 | Xoff-1 Word | Xoff-1 Word |
| 1 | 1 | 1 | Xoff-2 Word | Xoff-2 Word |

Note *3: These registers are accessible only when LCR bit-7 is set to a logic 1.
Note *4: Enhanced Feature Register, Xon 1,2 and Xoff 1,2 are accessible only when the LCR is set to “BF” (HEX).

### FIFO Operation

The 16 byte transmit and receive data FIFO's are enabled by the FIFO Control Register (FCR) bit-0. With 16C550 devices, the user can set the receive trigger level but not the transmit trigger level. The 580 provides independent trigger levels for both receiver and transmitter. To remain compatible with ST16C550, the transmit interrupt trigger level is set to 1 following a reset. It should be noted that the user can set the transmit trigger levels by writing to the FCR register, but activation will not take place until EFR bit-4 is set to a logic 1. The receiver FIFO section includes a time-out function to ensure data is delivered to the external CPU. An interrupt is generated whenever the Receive Holding Register (RHR) has not been read following the loading of a character or the receive trigger level has not been reached. (see hardware flow control for a description of this timing).

### Hardware Flow Control

When automatic hardware flow control is enabled, the 580 monitors the -CTS pin for a remote buffer overflow indication and controls the -RTS pin for local buffer overflows. Automatic hardware flow control is selected by setting bits 6 (RTS) and 7 (CTS) of the EFR register to a logic 1. If -CTS transitions from a logic 0 to a logic 1 indicating a flow control request, ISR bit-5 will be set to a logic 1 (if enabled via IER bit 6-7), and the 580 will suspend TX transmissions as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the -CTS input returns to a logic 0, indicating more data may be sent.

With the Auto RTS function enabled, an interrupt is generated when the receive FIFO reaches the programmed trigger level. The -RTS pin will not be forced to a logic 1 (RTS Off), until the receive FIFO reaches the next trigger level**.** However, the -RTS pin will return to a logic 0 after the data buffer (FIFO) is unloaded to the next trigger level below the programmed trigger level. However, under the above described conditions the 580 will continue to accept data until the receive FIFO is full.

| Selected Trigger Level (characters) | INT Pin Activation | -RTS Logic "1" (characters) | -RTS Logic "0" (characters) |
|---|---|---|---|
| 1 | 1 | 4 | 0 |
| 4 | 4 | 8 | 1 |
| 8 | 8 | 14 | 4 |
| 14 | 14 | 14 | 8 |

### Software Flow Control

When software flow control is enabled, the 580 compares one or two sequential receive data characters with the programmed Xon or Xoff-1,2 character value(s). If receive character(s) (RX) match the programmed values, the 580 will halt transmission (TX) as soon as the current character(s) has completed transmission. When a match occurs, the receive ready (if enabled via Xoff IER bit-5) flags will be set and the interrupt output pin (if receive interrupt is enabled) will be activated. Following a suspension due to a match of the Xoff characters values, the 580 will monitor the receive data stream for a match to the Xon-1,2 character value(s). If a match is found, the 580 will resume operation and clear the flags (ISR bit-4).

Reset initially sets the contents of the Xon/Xoff 8-bit flow control registers to a logic 0. Following reset the user can write any Xon/Xoff value desired for software flow control. Different conditions can be set to detect Xon/Xoff characters and suspend/resume transmissions. When double 8-bit Xon/Xoff characters are selected, the 580 compares two consecutive receive characters with two software flow control 8-bit values (Xon1, Xon2, Xoff1, Xoff2) and controls TX transmissions accordingly. Under the above described flow control mechanisms, flow control characters are not placed (stacked) in the user accessible RX data buffer or FIFO.

In the event that the receive buffer is overfilling and flow control needs to be executed, the 580 automatically sends an Xoff message (when enabled) via the serial TX output to the remote modem. The 580 sends the Xoff-1,2 characters as soon as received data passes the programmed trigger level. To clear this condition, the 580 will transmit the programmed Xon-1,2 characters as soon as receive data drops below the programmed trigger level.

### Special Feature Software Flow Control

A special feature is provided to detect an 8-bit character when bit-5 is set in the Enhanced Feature Register (EFR). When this character is detected, it will be placed on the user accessible data stack along with normal incoming RX data. This condition is selected in conjunction with EFR bits 0-3. Note that software flow control should be turned off when using this special mode by setting EFR bit 0-3 to a logic 0.

The 580 compares each incoming receive character with Xoff-2 data. If a match exists, the received data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of special character (see Figure 9). Although the Internal Register Table shows each X-Register with eight bits of character information, the actual number of bits is dependent on the programmed word length. Line Control Register (LCR) bits 0-1 defines the number of character bits, i.e., either 5 bits, 6 bits, 7 bits, or 8 bits. The word length selected by LCR bits 0-1 also determines the number of bits that will be used for the special character comparison. Bit-0 in the X-registers corresponds with the LSB bit for the receive character.

### Time-out Interrupts

Three special interrupts have been added to monitor the hardware and software flow control. The interrupts are enabled by IER bits 5-7. Care must be taken when handling these interrupts. Following a reset the transmitter interrupt is enabled, the 580 will issue an interrupt to indicate that transmit holding register is empty. This interrupt must be serviced prior to continuing operations. The LSR register provides the current singular highest priority interrupt only. It could be noted that CTS and RTS interrupts have lowest interrupt priority. A condition can exist where a higher priority interrupt may mask the lower priority CTS/ RTS interrupt(s). Only after servicing the higher pending interrupt will the lower priority CTS/ RTS interrupt(s) be reflected in the status register. Servicing the interrupt without investigating further interrupt conditions can result in data errors.

When two interrupt conditions have the same priority, it is important to service these interrupts correctly. Receive Data Ready and Receive Time Out have the same interrupt priority (when enabled by IER bit-3). The receiver issues an interrupt after the number of characters have reached the programmed trigger

level. In this case the 580 FIFO may hold more characters than the programmed trigger level. Following the removal of a data byte, the user should recheck LSR bit-0 for additional characters. A Receive Time Out will not occur if the receive FIFO is empty. The time out counter is reset at the center of each stop bit received or each time the receive holding register (RHR) is read (see Figure 10, Receive Time-out Interrupt). The actual time out value is T (**T**ime out length in bits) = 4 X P (**P**rogrammed word length) + 12. To convert the time out value to a character value, the user has to consider the complete word length, including data information length, start bit, parity bit, and the size of stop bit, i.e., 1X, 1.5X, or 2X bit times.

Example -A: If the user programs a word length of 7, with no parity and one stop bit, the time out will be:
T = 4 X 7( programmed word length) +12 = 40 bit times. The character time will be equal to 40 / 9 = 4.4 characters, or as shown in the fully worked out example: T = [(programmed word length = 7) + (stop bit = 1) + (start bit = 1) = 9]. 40 (bit times divided by 9) = 4.4 characters.

Example -B: If the user programs the word length = 7, with parity and one stop bit, the time out will be:
T = 4 X 7(programmed word length) + 12 = 40 bit times. Character time = 40 / 10 [ (programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

**Programmable Baud Rate Generator**

The 580 supports high speed modem technologies that have increased input data rates by employing data compression schemes. For example a 33.6Kbps modem that employs data compression may require a 115.2Kbps input data rate. A 128.0Kbps ISDN modem that supports data compression may need an input data rate of 460.8Kbps. The 580 can support a standard data rate of 921.6Kbps.

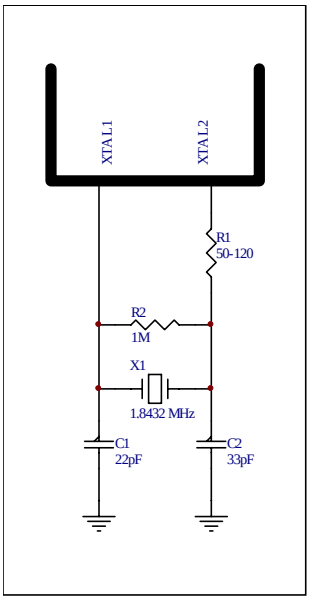
Single baud rate generator is provided for the transmitter and receiver, allowing independent TX/RX channel control. The programmable Baud Rate Generator is capable of accepting an input clock up to 24 MHz, as required for supporting a 1.5Mbps data rate.

The 580 can be configured for internal or external clock operation. For internal clock oscillator operation, an industry standard microprocessor crystal (parallel resonant/ 22-33 pF load) is connected externally between the XTAL1 and XTAL2 pins, with an external 1 M resistor across it. Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates.

The generator divides the input 16X clock by any divisor from 1 to $2^{16}$ -1. The 580 divides the basic crystal or external clock by 16. Further division of this 16X clock provides two table rates to support low and high data rate applications using the same system design. The two rate tables are selectable through the internal register, MCR bit-7. Setting MCR bit-7 to a logic 1 provides an additional divide by 4 whereas, setting MCR bit-7 to a logic 0 only divides by 1. (See Table 4 and Figure 11). The frequency of the -BAUDOUT output pin is exactly 16X (16 times) of the selected baud rate (-BAUDOUT =16 x Baud Rate). Customized Baud Rates can be achieved by selecting the proper divisor values for the MSB and LSB sections of baud rate generator.

Programming the Baud Rate Generator Registers

Crystal oscillator connection

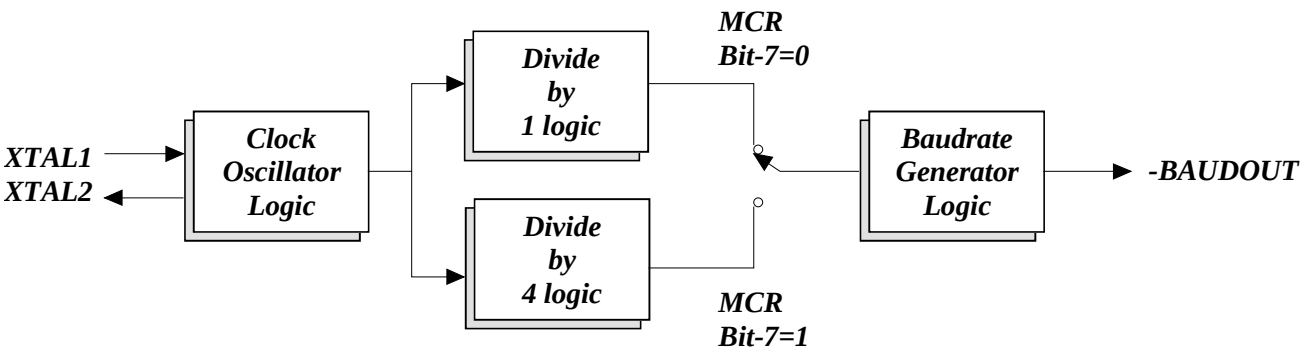


DLM (MSB) and DLL (LSB) provides a user capability for selecting the desired final baud rate. The example in Table 4 below, shows the two selectable baud rate tables available when using a 7.3728 MHz crystal.

**Table 4, BAUD RATE GENERATOR PROGRAMMING TABLE (7.3728 MHz CLOCK):**

| Output Baud Rate MCR BIT-7=1 | Output Baud Rate MCR Bit-7=0 | User 16 x Clock Divisor (Decimal) | User 16 x Clock Divisor (HEX) | DLM Program Value (HEX) | DLL Program Value (HEX) |
|---|---|---|---|---|---|
| 50 | 200 | 2304 | 900 | 09 | 00 |
| 75 | 300 | 1536 | 600 | 06 | 00 |
| 150 | 600 | 768 | 300 | 03 | 00 |
| 300 | 1200 | 384 | 180 | 01 | 80 |
| 600 | 2400 | 192 | C0 | 00 | C0 |
| 1200 | 4800 | 96 | 60 | 00 | 60 |
| 2400 | 9600 | 48 | 30 | 00 | 30 |
| 4800 | 19.2K | 24 | 18 | 00 | 18 |
| 7200 | 28.8K | 16 | 10 | 00 | 10 |
| 9600 | 38.4k | 12 | 0C | 00 | 0C |
| 19.2k | 76.8k | 6 | 06 | 00 | 06 |
| 38.4k | 153.6k | 3 | 03 | 00 | 03 |
| 57.6k | 230.4k | 2 | 02 | 00 | 02 |
| 115.2k | 460.8k | 1 | 01 | 00 | 01 |

Crystal oscillator or External clock 1X / 4X selection



### DMA Operation

The 580 FIFO trigger level provides additional flexibility to the user for block mode operation. LSR bits 5-6 provide an indication when the transmitter is empty or has an empty location(s). The user can optionally operate the transmit and receive FIFO's in the DMA mode (FCR bit-3). When the transmit and receive FIFO's are enabled and the DMA mode is deactivated (DMA Mode "0"), the 580 activates the interrupt output pin for each data transmit or receive operation. When DMA mode is activated (DMA Mode "1"), the user takes the advantage of block mode operation by loading or unloading the FIFO in a block sequence determined by the preset trigger level. In this mode, the 580 sets the interrupt output pin when characters in the transmit FIFO's are below the transmit trigger level, or the characters in the receive FIFO's are above the receive trigger level.

### Sleep Mode

The 580 is designed to operate with low power consumption. A special sleep mode is included to further reduce power consumption when the chip is not being used. With EFR bit-4 and IER bit-4 enabled (set to a logic 1), the 580 enters the sleep mode but resumes normal operation when a start bit is detected, a change of state on any of the modem input pins RX, -RI, -CTS, -DSR, -CD, or transmit data is provided by the user. If the sleep mode is enabled and the 580 is awakened by one of the conditions described above, it will return to the sleep mode automatically after the last character is transmitted or read by the user. In any case, the sleep mode will not be entered while an interrupt(s) is pending. The 580 will stay in the sleep mode of operation until it is disabled by setting IER bit-4 to a logic 0.

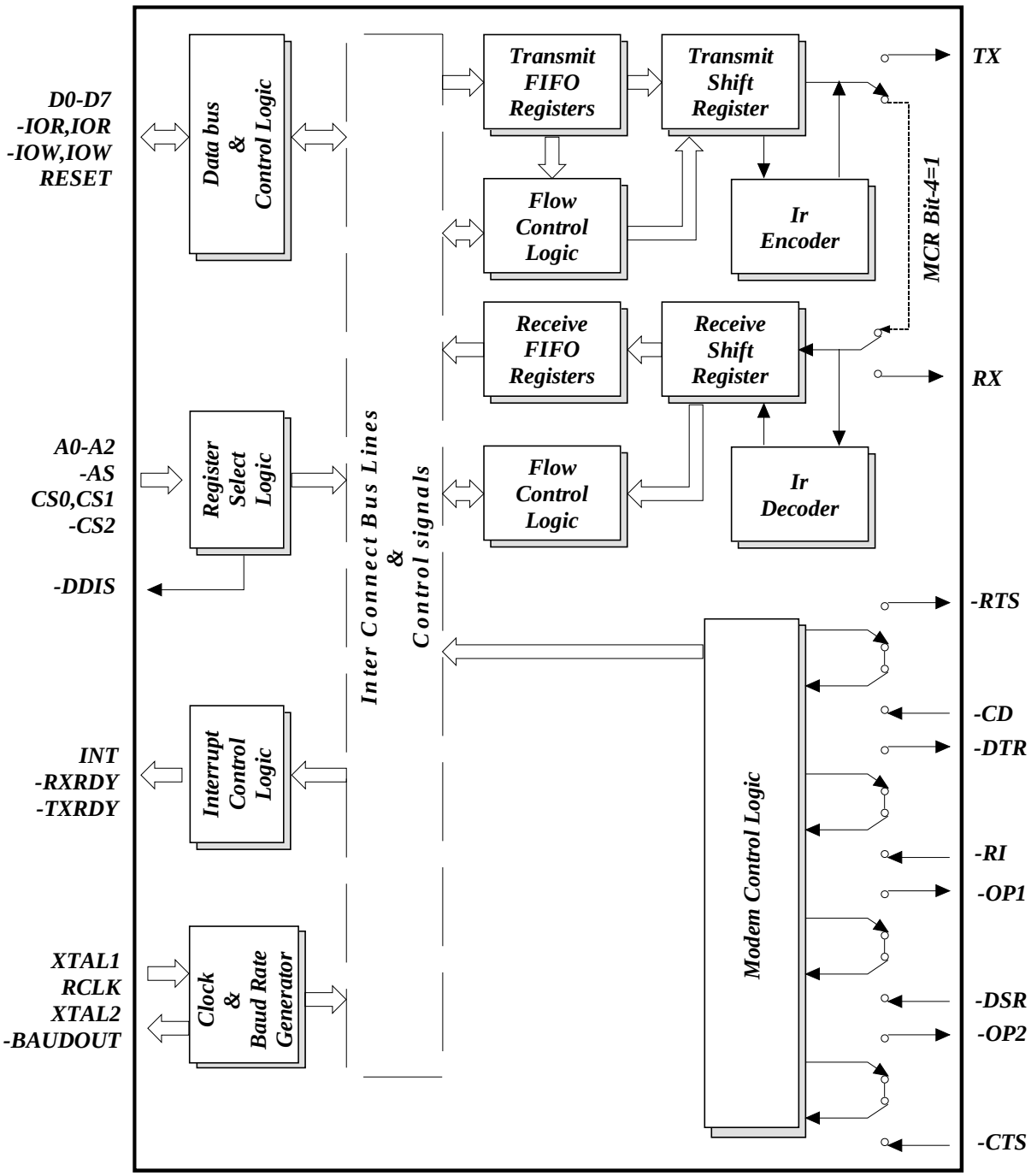
### Loop-back Mode

The internal loop-back capability allows onboard diagnostics. In the loop-back mode the normal modem interface pins are disconnected and reconfigured for loop-back internally. In this mode MSR bits 4-7 are also disconnected. However, MCR register bits 0-3 can be used for controlling loop-back diagnostic testing.

In the loop-back mode OP1 and OP2 in the MCR register (bits 0-1) control the modem -RI and -CD inputs respectively. MCR signals -DTR and -RTS (bits 0-1) are used to control the modem -CTS and -DSR inputs respectively. The transmitter output (TX) and the receiver input (RX) are disconnected from their associated interface pins, and instead are connected together internally (See Figure 12). The -CTS, -DSR, -CD, and -RI are disconnected from their normal modem control inputs pins, and instead are connected internally to -DTR, -RTS, -OP1 and -OP2. Loop-back test data is entered into the transmit holding register via the user data bus interface, D0-D7. The transmit UART serializes the data and passes the serial data to the receive UART via the internal loop-back connection. The receive UART converts the serial data back into parallel data that is then made available at the user data interface, D0-D7. The user optionally compares the received data to the initial transmitted data for verifying error free operation of the UART TX/RX circuits.

In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational. However, the interrupts can only be read using lower four bits of the Modem Control Register (MCR bits 0-3) instead of the four Modem Status Register bits 4-7. The interrupts are still controlled by the IER.

**Figure 12, INTERNAL LOOP-BACK MODE DIAGRAM**



## REGISTER FUNCTIONAL DESCRIPTIONS

The following table delineates the assigned bit functions for the fifteen 580 internal registers. The assigned bit functions are more fully defined in the following paragraphs.

### Table 5, ST16C580 INTERNAL REGISTERS

| A2 A1 A0 | Register [Default] Note *5 | BIT-7 | BIT-6 | BIT-5 | BIT-4 | BIT-3 | BIT-2 | BIT-1 | BIT-0 |
|---|---|---|---|---|---|---|---|---|---|
| **General Register Set** | | | | | | | | | |
| 0 0 0 | RHR [XX] | bit-7 | bit-6 | bit-5 | bit-4 | bit-3 | bit-2 | bit-1 | bit-0 |
| 0 0 0 | THR [XX] | bit-7 | bit-6 | bit-5 | bit-4 | bit-3 | bit-2 | bit-1 | bit-0 |
| 0 0 1 | IER [00] | CTS interrupt | RTS interrupt | Xoff interrupt | Sleep mode | modem status interrupt | receive line status interrupt | transmit holding register | receive holding register |
| 0 1 0 | FCR [00] | RCVR trigger (MSB) | RCVR trigger (LSB) | TX trigger (MSB) | TX trigger (LSB) | DMA mode select | XMIT FIFO reset | RCVR FIFO reset | FIFO enable |
| 0 1 0 | ISR [01] | FIFO's enabled | FIFO's enabled | INT priority bit-4 | INT priority bit-3 | INT priority bit-2 | INT priority bit-1 | INT priority bit-0 | INT status |
| 0 1 1 | LCR [00] | divisor latch enable | set break | set parity | even parity | parity enable | stop bits | word length bit-1 | word length bit-0 |
| 1 0 0 | MCR [00] | Clock select | IR enable | 0 | loop back | -OP2 | -OP1 | -RTS | -DTR |
| 1 0 1 | LSR [60] | FIFO data error | trans. empty | trans. holding empty | break interrupt | framing error | parity error | overrun error | receive data ready |
| 1 1 0 | MSR [X0] | CD | RI | DSR | CTS | delta -CD | delta -RI | delta -DSR | delta -CTS |
| 1 1 1 | SPR [FF] | bit-7 | bit-6 | bit-5 | bit-4 | bit-3 | bit-2 | bit-1 | bit-0 |
| **Special Register Set: Note *3** | | | | | | | | | |
| 0 0 0 | DLL [XX] | bit-7 | bit-6 | bit-5 | bit-4 | bit-3 | bit-2 | bit-1 | bit-0 |
| 0 0 1 | DLM [XX] | bit-15 | bit-14 | bit-13 | bit-12 | bit-11 | bit-10 | bit-9 | bit-8 |

| A2 A1 A0 | Register [Default] Note *5 | BIT-7 | BIT-6 | BIT-5 | BIT-4 | BIT-3 | BIT-2 | BIT-1 | BIT-0 |
|---|---|---|---|---|---|---|---|---|---|
| **Enhanced Register Set: Note *4** | | | | | | | | | |
| 0 1 0 | EFR [00] | Auto CTS | Auto RTS | Special Char. select | Enable IER Bits 4-7, ISR, FCR Bits 4-5, MCR Bits 5-7 | Cont-3 Tx,Rx Control | Cont-2 Tx,Rx Control | Cont-1 Tx,Rx Control | Cont-0 Tx,Rx Control |
| 1 0 0<br>1 0 1<br>1 1 0<br>1 1 1 | Xon-1 [00]<br>Xon-2 [00]<br>Xoff-1 [00]<br>Xoff-2 [00] | bit-7<br>bit-15<br>bit-7<br>bit-15 | bit-6<br>bit-14<br>bit-6<br>bit-14 | bit-5<br>bit-13<br>bit-5<br>bit-13 | bit-4<br>bit-12<br>bit-4<br>bit-12 | bit-3<br>bit-11<br>bit-3<br>bit-11 | bit-2<br>bit-10<br>bit-2<br>bit-10 | bit-1<br>bit-9<br>bit-1<br>bit-9 | bit-0<br>bit-8<br>bit-0<br>bit-8 |

Note *3: The Special register set is accessible only when LCR bit-7 is set to a logic 1.
Note *4: Enhanced Feature Register, Xon 1,2 and Xoff 1,2 are accessible only when LCR is set to “BF“ Hex
Note *5: The value represents the register’s initialized HEX value. An “X” signifies a 4-bit un-initialize nibble.

**Transmit and Receive Holding Register**

The serial transmitter section consists of an 8-bit Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the THR is provided in the Line Status Register (LSR). Writing to the THR transfers the contents of the data bus (D7-D0) to the THR, providing that the THR or TSR is empty. The THR empty flag in the LSR register will be set to a logic 1 when the transmitter is empty or when data is transferred to the TSR. Note that a write operation can be performed when the transmit holding register empty flag is set (logic 0 = FIFO full, logic 1= at least one FIFO location available).

The serial receive section also contains an 8-bit Receive Holding Register, RHR. Receive data is removed from the 580 and receive FIFO by reading the RHR register. The receive section provides a mechanism to prevent false starts. On the falling edge of a start or false start bit, an internal receiver counter starts counting clocks at 16x clock rate. After 7 1/2 clocks the start bit time should be shifted to the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. Receiver status codes will be posted in the LSR.

**Interrupt Enable Register (IER)**

The Interrupt Enable Register (IER) masks the interrupts from receiver ready, transmitter empty, line status and modem status registers. These interrupts would normally be seen on the 580 INT output pin.

***IER Vs Receive FIFO Interrupt Mode Operation***

When the receive FIFO (FCR BIT-0 = a logic 1) and receive interrupts (IER BIT-0 = logic 1) are enabled, the receive interrupts and register status will reflect the following:

A) The receive data available interrupts are issued to the external CPU when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.

B) FIFO status will also be reflected in the user accessible ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.

***IER Vs Receive/Transmit FIFO Polled Mode Operation***

When FCR BIT-0 equals a logic 1; resetting IER bits 0-3 enables the 580 in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

A) LSR BIT-0 will be a logic 1 as long as there is one byte in the receive FIFO.

B) LSR BIT 1-4 will indicate if an overrun error occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both the transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate any FIFO data errors.

*IER BIT-0:*
Logic 0 = Disable the receiver ready interrupt. (normal default condition)
Logic 1 = Enable the receiver ready interrupt.

*IER BIT-1:*
Logic 0 = Disable the transmitter empty interrupt. (normal default condition)
Logic 1 = Enable the transmitter empty interrupt.

*IER BIT-2:*
Logic 0 = Disable the receiver line status interrupt. (normal default condition)
Logic 1 = Enable the receiver line status interrupt.

*IER BIT-3:*
Logic 0 = Disable the modem status register interrupt. (normal default condition)
Logic 1 = Enable the modem status register interrupt.

*IER BIT -4:*
Logic 0 = Disable sleep mode. (normal default condition)
Logic 1 = Enable sleep mode. See Sleep Mode section for details

*IER BIT-5:*
Logic 0 = Disable the software flow control, receive Xoff interrupt. (normal default condition)
Logic 1 = Enable the software flow control, receive Xoff interrupt. See Software Flow Control section for details.

*IER BIT-6:*
Logic 0 = Disable the RTS interrupt. (normal default condition)
Logic 1 = Enable the RTS interrupt. The 580 issues an interrupt when the RTS pin transitions from a logic 0 to a logic 1.

*IER BIT-7:*
Logic 0 = Disable the CTS interrupt. (normal default condition)
Logic 1 = Enable the CTS interrupt. The 580 issues an interrupt when CTS pin transitions from a logic 0 to a logic 1.

**FIFO Control Register (FCR)**

This register is used to enable the FIFO's, clear the FIFO's, set the transmit/receive FIFO trigger levels, and select the DMA mode. The DMA, and FIFO modes are defined as follows:

*DMA MODE*
Mode 0 Set and enable the interrupt for each single transmit or receive operation, and is similar to the ST16C450 mode. Transmit Ready (-TXRDY) will go to a logic 0 when ever an empty transmit space is available in the Transmit Holding Register (THR). Receive Ready (-RXRDY) will go to a logic 0 whenever the Receive Holding Register (RHR) is loaded with a character.
Mode 1 Set and enable the interrupt in a block mode operation. The transmit interrupt is set when the transmit FIFO is below the programmed trigger level. -TXRDY remains a logic 0 as long as one empty FIFO location is available. The receive interrupt is set when the receive FIFO fills to the programmed trigger level. However the FIFO continues to fill regardless of the programmed level until the FIFO is full. -RXRDY remains a logic 0 as long as the FIFO fill level is above the programmed trigger level.

*FCR BIT-0:*
Logic 0 = Disable the transmit and receive FIFO. (normal default condition)
Logic 1 = Enable the transmit and receive FIFO. This bit must be a "1" when other FCR bits are written to or they will not be programmed.

*FCR BIT-1:*
Logic 0 = No FIFO receive reset. (normal default condition)
Logic 1 = Clears the contents of the receive FIFO and resets the FIFO counter logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO.

*FCR BIT-2:*
Logic 0 = No FIFO transmit reset. (normal default condition)
Logic 1 = Clears the contents of the transmit FIFO and resets the FIFO counter logic (the transmit shift register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO.

*FCR BIT-3:*
Logic 0 = Set DMA mode "0". (normal default condition)
Logic 1 = Set DMA mode "1."

*Transmit operation in mode "0":*
When the 580 is in the ST16C450 mode (FIFO's disabled, FCR bit-0 = logic 0) or in the FIFO mode (FIFO's enabled, FCR bit-0 = logic 1, FCR bit-3 = logic 0) and when there are no characters in the transmit FIFO or transmit holding register, the -TXRDY pin will be a

logic 0. Once active the -TXRDY pin will go to a logic 1 after the first character is loaded into the transmit holding register.

*Receive operation in mode "0":*
When the 580 is in mode "0" (FCR bit-0 = logic 0) or in the FIFO mode (FCR bit-0 = logic 1, FCR bit-3 = logic 0) and there is at least one character in the receive FIFO, the -RXRDY pin will be a logic 0. Once active the -RXRDY pin will go to a logic 1 when there are no more characters in the receiver.

*Transmit operation in mode "1":*
When the 580 is in FIFO mode ( FCR bit-0 = logic 1, FCR bit-3 = logic 1 ), the -TXRDY pin will be a logic 1 when the transmit FIFO is completely full. It will be a logic 0 if one or more FIFO locations are empty.

*Receive operation in mode "1":*
When the 580 is in FIFO mode (FCR bit-0 = logic 1, FCR bit-3 = logic 1) and the trigger level has been reached, or a Receive Time Out has occurred, the -RXRDY pin will go to a logic 0. Once activated, it will go to a logic 1 after there are no more characters in the FIFO.

*FCR BIT 4-5: (logic 0 or cleared is the default condition, TX trigger level = 1)*
These bits are used to set the trigger level for the transmit FIFO interrupt. The ST16C580 will issue a transmit empty interrupt when the number of characters in FIFO drops below the selected trigger level.

| BIT-5 | BIT-4 | TX FIFO trigger level |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 4 |
| 1 | 0 | 8 |
| 1 | 1 | 14 |

*FCR BIT 6-7: (logic 0 or cleared is the default condition, RX trigger level =8)*

These bits are used to set the trigger level for the receive FIFO interrupt.

An interrupt is generated when the number of characters in the FIFO equals the programmed trigger level. However the FIFO will continue to be loaded until it is full.

| BIT-7 | BIT-6 | RX FIFO trigger level |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 4 |
| 1 | 0 | 8 |
| 1 | 1 | 14 |

**Interrupt Status Register (ISR)**

The 580 provides six levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with six interrupt status bits. Performing a read cycle on the ISR will provide the user with the highest pending interrupt level to be serviced. No other interrupts are acknowledged until the pending interrupt is serviced. Whenever the interrupt status register is read, the interrupt status is cleared. However it should be noted that only the current pending interrupt is cleared by the read. A lower level interrupt may be seen after rereading the interrupt status bits. The Interrupt Source Table 6 (below) shows the data values (bit 0-5) for the six prioritized interrupt levels and the interrupt sources associated with each of these interrupt levels:

**Table 6, INTERRUPT SOURCE TABLE**

| Priority Level | [ ISR BITS ] Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | Source of the interrupt |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | LSR (Receiver Line Status Register) |
| 2 | 0 | 0 | 0 | 1 | 0 | 0 | RXRDY (Received Data Ready) |
| 2 | 0 | 0 | 1 | 1 | 0 | 0 | RXRDY (Receive Data time out) |
| 3 | 0 | 0 | 0 | 0 | 1 | 0 | TXRDY ( Transmitter Holding Register Empty) |
| 4 | 0 | 0 | 0 | 0 | 0 | 0 | MSR (Modem Status Register) |
| 5 | 0 | 1 | 0 | 0 | 0 | 0 | RXRDY (Received Xoff signal)/ Special character |
| 6 | 1 | 0 | 0 | 0 | 0 | 0 | CTS, RTS change of state |

*ISR BIT-0:*
Logic 0 = An interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
Logic 1 = No interrupt pending. (normal default condition)

*ISR BIT 1-3: (logic 0 or cleared is the default condition)*
These bits indicate the source for a pending interrupt at interrupt priority levels 1, 2, and 3 (See Interrupt Source Table).

*ISR BIT 4-5: (logic 0 or cleared is the default condition)*
These bits are enabled when EFR bit-4 is set to a logic 1. ISR bit-4 indicates that matching Xoff character(s) have been detected. ISR bit-5 indicates that CTS, RTS have been generated. Note that once set to a logic 1, the ISR bit-4 will stay a logic 1 until Xon character(s) are received.

*ISR BIT 6-7: (logic 0 or cleared is the default condition)*
These bits are set to a logic 0 when the FIFO is not being used. They are set to a logic 1 when the FIFO's are enabled

**Line Control Register (LCR)**

The Line Control Register is used to specify the asynchronous data communication format. The word length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

*LCR BIT 0-1: (logic 0 or cleared is the default condition)*
These two bits specify the word length to be transmitted or received.

| BIT-1 | BIT-0 | Word length |
|---|---|---|
| 0 | 0 | 5 |
| 0 | 1 | 6 |
| 1 | 0 | 7 |
| 1 | 1 | 8 |

*LCR BIT-2: (logic 0 or cleared is the default condition)*
The length of stop bit is specified by this bit in conjunction with the programmed word length.

| BIT-2 | Word length | Stop bit length (Bit time(s)) |
|---|---|---|
| 0 | 5,6,7,8 | 1 |
| 1 | 5 | 1-1/2 |
| 1 | 6,7,8 | 2 |

*LCR BIT-3:*
Parity or no parity can be selected via this bit.
Logic 0 = No parity (normal default condition)
Logic 1 = A parity bit is generated during the transmission, receiver checks the data and parity for transmission errors.

*LCR BIT-4:*
If the parity bit is enabled with LCR bit-3 set to a logic 1, LCR BIT-4 selects the even or odd parity format.
Logic 0 = ODD Parity is generated by forcing an odd number of logic 1's in the transmitted data. The receiver must be programmed to check the same format. (normal default condition)
Logic 1 = EVEN Parity is generated by forcing an even the number of logic 1's in the transmitted. The receiver must be programmed to check the same format.

*LCR BIT-5:*
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5 = logic 0, parity is not forced (normal default condition)
LCR BIT-5 = logic 1 and LCR BIT-4 = logic 0, parity bit is forced to a logical 1 for the transmit and receive data.
LCR BIT-5 = logic 1 and LCR BIT-4 = logic 1, parity bit is forced to a logical 0 for the transmit and receive data.

| LCR Bit-5 | LCR Bit-4 | LCR Bit-3 | Parity selection |
|---|---|---|---|
| X | X | 0 | No parity |
| 0 | 0 | 1 | Odd parity |
| 0 | 1 | 1 | Even parity |
| 1 | 0 | 1 | Force parity "1" |
| 1 | 1 | 1 | Forced parity "0" |

*LCR BIT-6:*
When enabled the Break control bit causes a break condition to be transmitted (the TX output is forced to a logic 0 state). This condition exists until disabled by setting LCR bit-6 to a logic 0.
Logic 0 = No TX break condition. (normal default condition)
Logic 1 = Forces the transmitter output (TX) to a logic 0 for alerting the remote receiver to a line break condition.

*LCR BIT-7:*
The internal baud rate counter latch and Enhance Feature mode enable.
Logic 0 = Divisor latch disabled. (normal default condition)
Logic 1 = Divisor latch and enhanced feature register enabled.

**Modem Control Register (MCR)**

This register controls the interface with the modem or a peripheral device.

*MCR BIT-0:*
Logic 0 = Force -DTR output to a logic 1. (normal default condition)
Logic 1 = Force -DTR output to a logic 0.

*MCR BIT-1:*
Logic 0 = Force -RTS output to a logic 1. (normal default condition)
Logic 1 = Force -RTS output to a logic 0.
Automatic RTS may be used for hardware flow control by enabling EFR bit-6 (See EFR bit-6).

*MCR BIT-2:*
Logic 0 = Set -OP1 output to a logic 1. (normal default condition)
Logic 1 = Set -OP1 output to a logic 0.

*MCR BIT-3:*
Logic 0 = Set -OP2 output to a logic 1. (normal default condition)
Logic 1 = Set -OP2 output to a logic 0.

*MCR BIT-4:*
Logic 0 = Disable loop-back mode. (normal default condition)
Logic 1 = Enable local loop-back mode (diagnostics).

*MCR BIT-5:*
Not used.

*MCR BIT-6:*
Logic 0 = Enable Modem receive and transmit input/output interface. (normal default condition)
Logic 1 = Enable infrared IrDA receive and transmit

inputs/outputs. While in this mode, the TX/RX output/ Inputs are routed to the infrared encoder/decoder. The data input and output levels will conform to the IrDA infrared interface requirement. As such, while in this mode the infrared TX output will be a logic 0 during idle data conditions.

*MCR BIT-7:*
Logic 0 = Divide by one. The input clock (crystal or external) is divided by sixteen and then presented to the Programmable Baud Rate Generator (BGR) without further modification, i.e., divide by one. (normal, default condition)
Logic 1 = Divide by four. The divide by one clock described in MCR bit-7 equals a logic 0, is further divided by four (also see Programmable Baud Rate Generator section).

**Line Status Register (LSR)**

This register provides the status of data transfers between. the 580 and the CPU.

*LSR BIT-0:*
Logic 0 = No data in receive holding register or FIFO. (normal default condition)
Logic 1 = Data has been received and is saved in the receive holding register or FIFO.

*LSR BIT-1:*
Logic 0 = No overrun error. (normal default condition)
Logic 1 = Overrun error. A data overrun error occurred in the receive shift register. This happens when additional data arrives while the FIFO is full. In this case the previous data in the shift register is overwritten. Note that under this condition the data byte in the receive shift register is not transfer into the FIFO, therefore the data in the FIFO is not corrupted by the error.

*LSR BIT-2:*
Logic 0 = No parity error (normal default condition)
Logic 1 = Parity error. The receive character does not have correct parity information and is suspect. In the FIFO mode, this error is associated with the character at the top of the FIFO.

*LSR BIT-3:*
Logic 0 = No framing error (normal default condition).
Logic 1 = Framing error. The receive character did not have a valid stop bit(s). In the FIFO mode this error is associated with the character at the top of the FIFO.

*LSR BIT-4:*
Logic 0 = No break condition (normal default condition)
Logic 1 = The receiver received a break signal (RX was a logic 0 for one character frame time). In the FIFO mode, only one break character is loaded into the FIFO.

*LSR BIT-5:*
This bit is the Transmit Holding Register Empty indicator. This bit indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to CPU when the THR interrupt enable is set. The THR bit is set to a logic 1 when a character is transferred from the transmit holding register into the transmitter shift register. The bit is reset to logic 0 concurrently with the loading of the transmitter holding register by the CPU. In the FIFO mode this bit is set when the transmit FIFO is empty; it is cleared when at least 1 byte is written to the transmit FIFO.

*LSR BIT-6:*
This bit is the Transmit Empty indicator. This bit is set to a logic 1 whenever the transmit holding register and the transmit shift register are both empty. It is reset to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to one whenever the transmit FIFO and transmit shift register are both empty.

*LSR BIT-7:*
Logic 0 = No Error (normal default condition)
Logic 1 = At least one parity error, framing error or break indication is in the current FIFO data. This bit is cleared when LSR register is read.

**Modem Status Register (MSR)**

This register provides the current state of the control interface signals from the modem, or other peripheral

device that the 580 is connected to. Four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a control input from the modem changes state. These bits are set to a logic 0 whenever the CPU reads this register.

*MSR BIT-0:*
Logic 0 = No -CTS Change (normal default condition)
Logic 1 = The -CTS input to the 580 has changed state since the last time it was read. A modem Status Interrupt will be generated.

*MSR BIT-1:*
Logic 0 = No -DSR Change (normal default condition)
Logic 1 = The -DSR input to the 580 has changed state since the last time it was read. A modem Status Interrupt will be generated.

*MSR BIT-2:*
Logic 0 = No -RI Change (normal default condition)
Logic 1 = The -RI input to the 580 has changed from a logic 0 to a logic 1. A modem Status Interrupt will be generated.

*MSR BIT-3:*
Logic 0 = No -CD Change (normal default condition)
Logic 1 = Indicates that the -CD input to the has changed state since the last time it was read. A modem Status Interrupt will be generated.

*MSR BIT-4:*
-CTS functions as hardware flow control signal input if it is enabled via EFR bit-7. The transmit holding register flow control is enabled/disabled by MSR bit-4. Flow control (when enabled) allows the starting and stopping the transmissions based on the external modem -CTS signal. A logic 1 at the -CTS pin will stop 580 transmissions as soon as current character has finished transmission.

Normally MSR bit-4 bit is the compliment of the -CTS input. However in the loop-back mode, this bit is equivalent to the RTS bit in the MCR register.

*MSR BIT-5:*
DSR (active high, logical 1). Normally this bit is the compliment of the -DSR input. In the loop-back mode, this bit is equivalent to the DTR bit in the MCR register.

*MSR BIT-6:*
RI (active high, logical 1). Normally this bit is the compliment of the -RI input. In the loop-back mode this bit is equivalent to the OP1 bit in the MCR register.

*MSR BIT-7:*
CD (active high, logical 1). Normally this bit is the compliment of the -CD input. In the loop-back mode this bit is equivalent to the OP2 bit in the MCR register.

**Scratchpad Register (SPR)**

The ST16C580 provides a temporary data register to store 8 bits of user information.

**Enhanced Feature Register (EFR)**

Enhanced features are enabled or disabled using this register.

Bits-0 through 4 provide single or dual character software flow control selection. When the Xon1 and Xon2 and/or Xoff1 and Xoff2 modes are selected, the double 8-bit words are concatenated into two sequential characters.

*EFR BIT 0-3: (logic 0 or cleared is the default condition)*
Combinations of software flow control can be selected by programming these bits.

**Table 7, SOFTWARE FLOW CONTROL FUNCTIONS**

| Cont-3 | Cont-2 | Cont-1 | Cont-0 | TX, RX software flow controls |
|---|---|---|---|---|
| 0 | 0 | X | X | No transmit flow control |
| 1 | 0 | X | X | Transmit Xon1/Xoff1 |
| 0 | 1 | X | X | Transmit Xon2/Xoff2 |
| 1 | 1 | X | X | Transmit Xon1 and Xon2/Xoff1 and Xoff2 |
| X | X | 0 | 0 | No receive flow control |
| X | X | 1 | 0 | Receiver compares Xon1/Xoff1 |
| X | X | 0 | 1 | Receiver compares Xon2/Xoff2 |
| 1 | 0 | 1 | 1 | Transmit Xon1/ Xoff1.<br>Receiver compares Xon1 and Xon2,<br>Xoff1 and Xoff2 |
| 0 | 1 | 1 | 1 | Transmit Xon2/Xoff2<br>Receiver compares Xon1 and Xon2/Xoff1 and Xoff2 |
| 1 | 1 | 1 | 1 | Transmit Xon1 and Xon2/Xoff1 and Xoff2<br>Receiver compares Xon1 and Xon2/Xoff1 and Xoff2 |
| 0 | 0 | 1 | 1 | No transmit flow control<br>Receiver compares Xon1 and Xon2/Xoff1 and Xoff2 |

*EFR BIT-4:*
Enhanced function control bit. The content of the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 can be modified and latched. After modifying any bits in the enhanced registers, EFR bit-4 can be set to a logic 0 to latch the new values. This feature prevents existing software from altering or overwriting the 580 enhanced functions.

Logic 0 = disable/latch enhanced features. IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 are saved to retain the user settings, then IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 are initialized to the default values shown in the Internal Resister Table. After a reset, the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 are set to a logic 0 to be compatible with ST16C550 mode. (normal default condition).
Logic 1 = Enables the enhanced functions. When this bit is set to a logic 1 all enhanced features of the 580 are enabled and user settings stored during a reset will be restored.

*EFR BIT-5:*
Logic 0 = Special Character Detect Disabled (normal default condition)
Logic 1 = Special Character Detect Enabled. The 580 compares each incoming receive character with Xoff-2 data. If a match exists, the received data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of special character. Bit-0 in the X-registers corresponds with the LSB bit for the receive character. When this feature is enabled, the normal software flow control must be disabled (EFR bits 0-3 must be set to a logic 0).

*EFR BIT-6:*
Automatic RTS may be used for hardware flow control by enabling EFR bit-6. When AUTO RTS is selected, an interrupt will be generated when the receive FIFO is filled to the programmed trigger level and -RTS will go to a logic 1 at the next trigger level. -RTS will return to a logic 0 when data is unloaded below the next lower trigger level (Programmed trigger level -1). The state of this register bit changes with the status of the

hardware flow control. -RTS functions normally when hardware flow control is disabled.

0 = Automatic RTS flow control is disabled. (normal default condition)
1 = Enable Automatic RTS flow control.

*EFR bit-7:*
Automatic CTS Flow Control.
Logic 0 = Automatic CTS flow control is disabled. (normal default condition)
Logic 1 = Enable Automatic CTS flow control. Transmission will stop when -CTS goes to a logical 1. Transmission will resume when the -CTS pin returns to a logical 0.

**ST16C580 EXTERNAL RESET CONDITIONS**

| REGISTERS | RESET STATE |
|---|---|
| IER | IER BITS 0-7 = logic 0 |
| ISR | ISR BIT-0=1, ISR BITS 1-7 = logic 0 |
| LCR, MCR | BITS 0-7 = logic 0 |
| LSR | LSR BITS 0-4 = logic 0, LSR BITS 5-6 = logic 1 LSR, BIT 7 = logic 0 |
| MSR | MSR BITS 0-3 = logic 0, MSR BITS 4-7 = logic levels of the input signals |
| FCR, EFR | BITS 0-7 = logic 0 |

| SIGNALS | RESET STATE |
|---|---|
| TX | Logic 1 |
| -OP1 | Logic 1 |
| -OP2 | Logic 1 |
| -RTS | Logic 1 |
| -DTR | Logic 1 |
| -RXRDY | Logic 1 |
| -TXRDY | Logic 0 |
| INT | Logic 0 |

## AC ELECTRICAL CHARACTERISTICS

$T_A$=0° - 70°C (-40° - +85°C for Industrial grade packages), Vcc=3.3 - 5.0 V ± 10% unless otherwise specified.

| Symbol | Parameter | Limits 3.3 | | Limits 5.0 | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| $T_{1w}$,$T_{2w}$ | Clock pulse duration | 17 | | 17 | | ns | |
| $T_{3w}$ | Oscillator/Clock frequency | | 8 | | 24 | MHz | |
| $T_{4w}$ | Address strobe width | 35 | | 25 | | ns | |
| $T_{5s}$ | Address setup time | 5 | | 0 | | ns | |
| $T_{5h}$ | Address hold time | 5 | | 5 | | ns | |
| $T_{6s}$ | Address setup time | 5 | | 0 | | ns | |
| $T_{6h}$ | Chip select hold time | 0 | | 0 | | ns | |
| $T_{7d}$ | -IOR delay from chip select | 10 | | 10 | | ns | Note 1: |
| $T_{7w}$ | -IOR strobe width | 35 | | 25 | | ns | |
| $T_{7h}$ | Chip select hold time from -IOR | 0 | | 0 | | ns | Note 1: |
| $T_{8d}$ | -IOR delay from address | 10 | | 10 | | ns | Note 1: |
| $T_{9d}$ | Read cycle delay | 40 | | 30 | | ns | |
| $T_{11d}$ | -IOR to -DDIS delay | | 15 | | 10 | ns | 100 pF load |
| $T_{12d}$ | Delay from -IOR to data | | 35 | | 25 | ns | |
| $T_{12h}$ | Data disable time | | 25 | | 15 | ns | |
| $T_{13d}$ | -IOW delay from chip select | 10 | | 10 | | ns | Note 1: |
| $T_{13w}$ | -IOW strobe width | 40 | | 25 | | ns | |
| $T_{13h}$ | Chip select hold time from -IOW | 0 | | 0 | | ns | |
| $T_{14d}$ | -IOW delay from address | 10 | | 10 | | ns | Note 1: |
| $T_{15d}$ | Write cycle delay | 40 | | 30 | | ns | |
| $T_{16s}$ | Data setup time | 20 | | 15 | | ns | |
| $T_{16h}$ | Data hold time | 5 | | 5 | | ns | |
| $T_{17d}$ | Delay from -IOW to output | | 50 | | 40 | ns | 100 pF load |
| $T_{18d}$ | Delay to set interrupt from MODEM input | | 40 | | 35 | ns | 100 pF load |
| $T_{19d}$ | Delay to reset interrupt from -IOR | | 40 | | 35 | ns | 100 pF load |
| $T_{20d}$ | Delay from stop to set interrupt | | 1 | | 1 | Rclk | |
| $T_{21d}$ | Delay from -IOR to reset interrupt | | 45 | | 40 | ns | 100 pF load |
| $T_{22d}$ | Delay from stop to interrupt | | 45 | | 40 | ns | |
| $T_{23d}$ | Delay from initial INT reset to transmit start | 8 | 24 | 8 | 24 | Rclk | |
| $T_{24d}$ | Delay from -IOW to reset interrupt | | 45 | | 40 | ns | |
| $T_{25d}$ | Delay from stop to set -RxRdy | | 1 | | 1 | Rclk | |
| $T_{26d}$ | Delay from -IOR to reset -RxRdy | | 45 | | 40 | ns | |
| $T_{27d}$ | Delay from -IOW to set -TxRdy | | 45 | | 40 | ns | |
| $T_{28d}$ | Delay from start to reset -TxRdy | | 8 | | 8 | Rclk | |
| $T_R$ | Reset pulse width | 40 | | 40 | | ns | |
| N | Baud rate devisor | 1 | $2^{16}$-1 | 1 | $2^{16}$-1 | Rclk | |

Note 1: Applicable only when -AS is tied low.

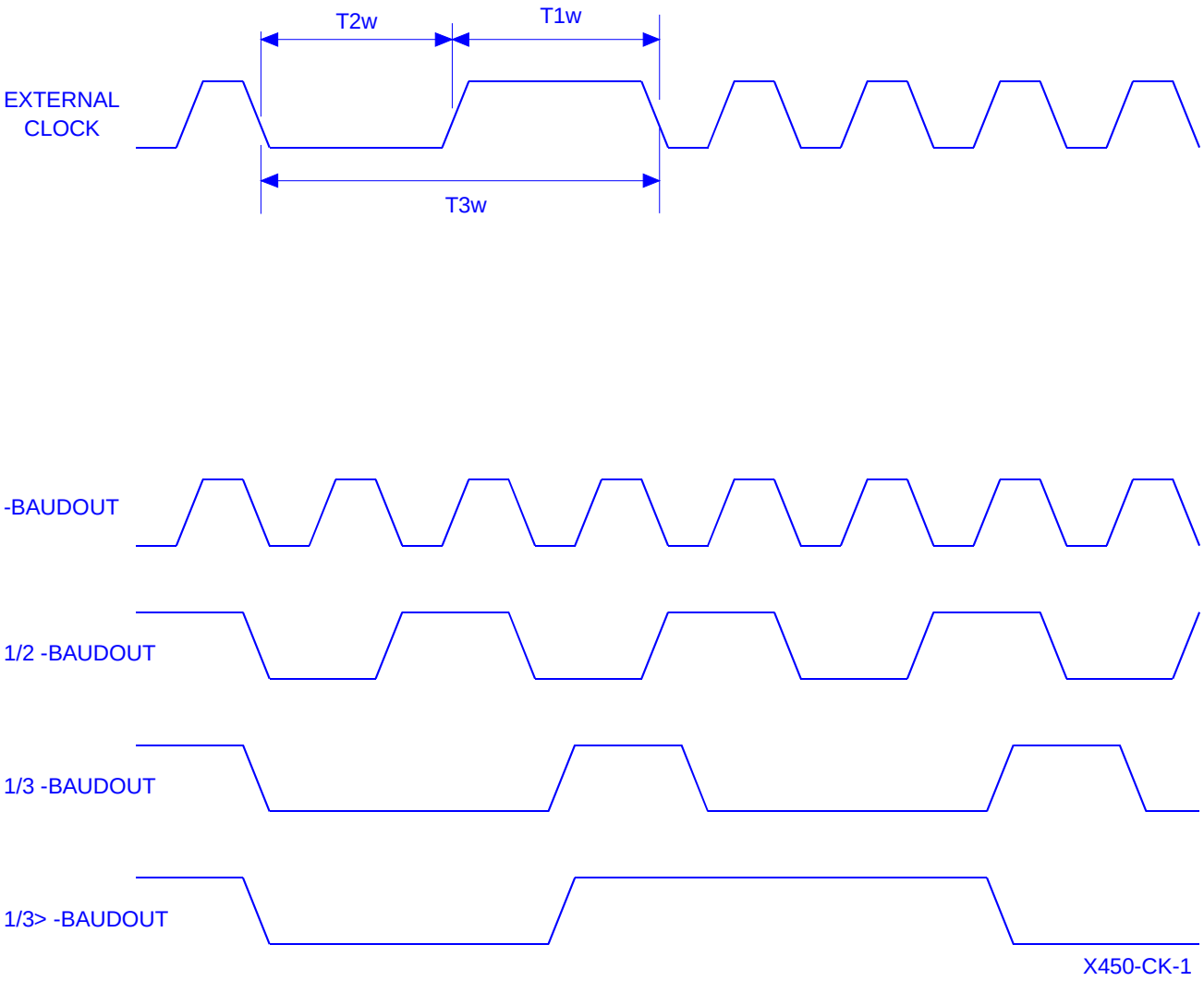
## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply range | 7 Volts |
| Voltage at any pin | GND - 0.3 V to VCC +0.3 V |
| Operating temperature | -40° C to +85° C |
| Storage temperature | -65° C to 150° C |
| Package dissipation | 500 mW |

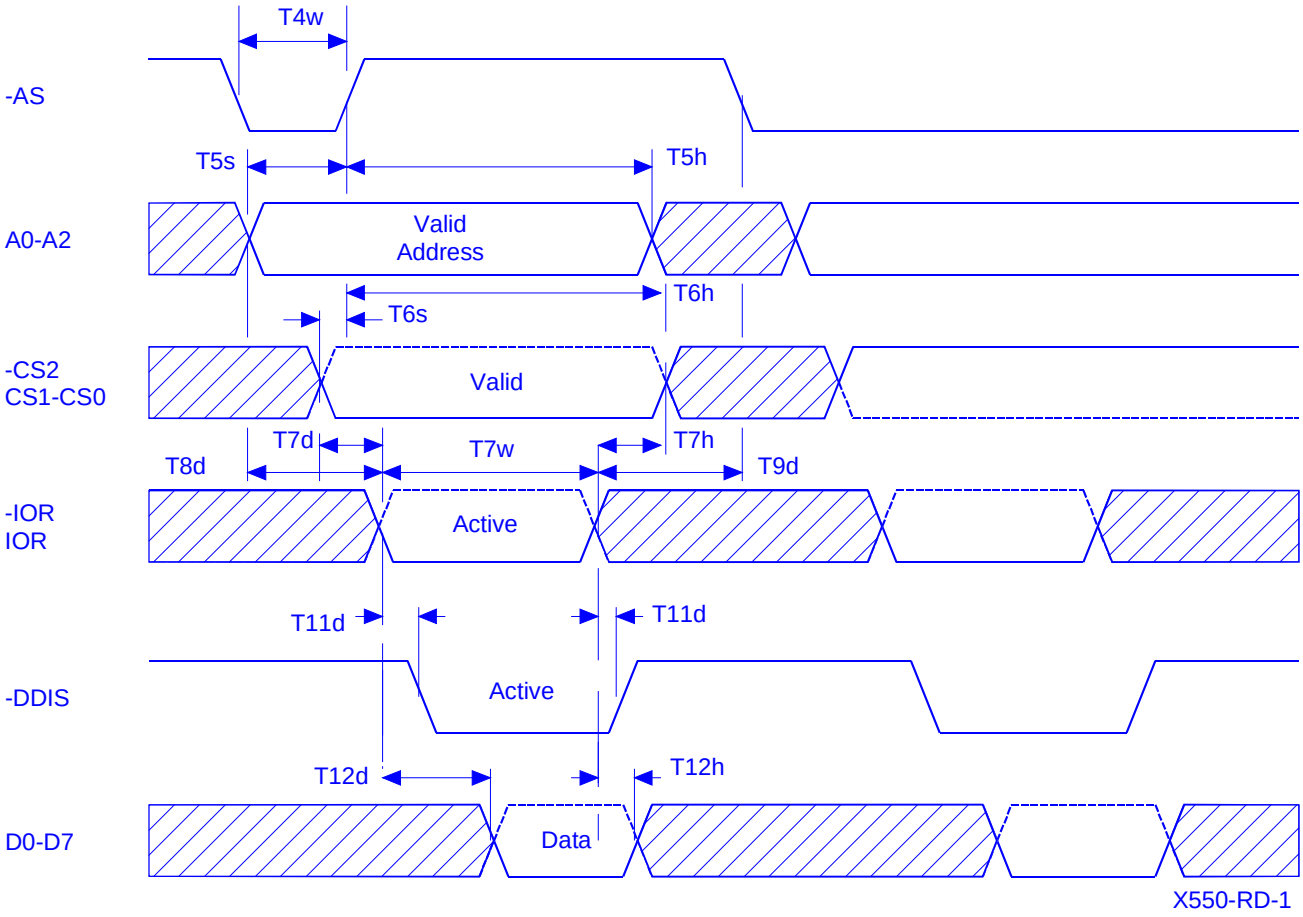
## DC ELECTRICAL CHARACTERISTICS

$T_A$=0° - 70°C (-40° - +85°C for Industrial grade packages), Vcc=3.3 - 5.0 V ± 10% unless otherwise specified.

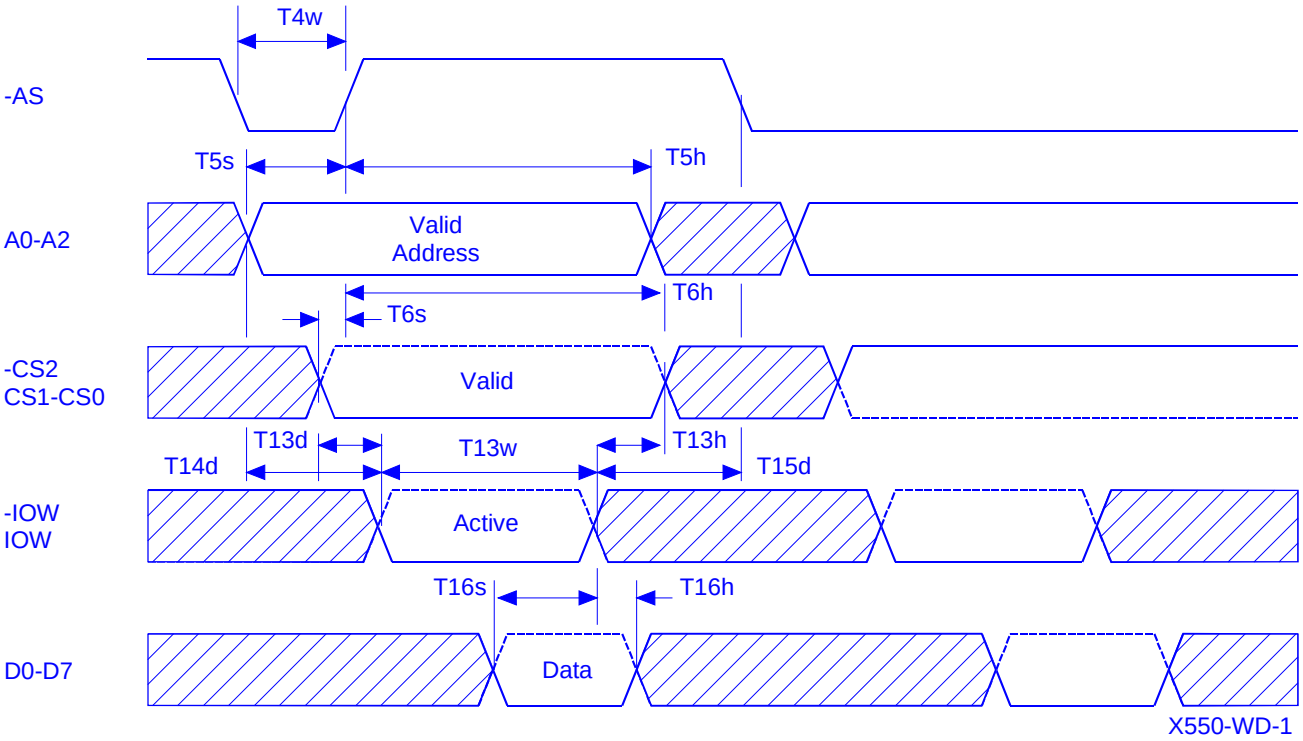
| Symbol | Parameter | Limits 3.3 | | Limits 5.0 | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| $V_{ILCK}$ | Clock input low level | -0.3 | 0.6 | -0.5 | 0.6 | V | |
| $V_{IHCK}$ | Clock input high level | 2.4 | VCC | 3.0 | VCC | V | |
| $V_{IL}$ | Input low level | -0.3 | 0.8 | -0.5 | 0.8 | V | |
| $V_{IH}$ | Input high level | 2.0 | | 2.2 | VCC | V | |
| $V_{OL}$ | Output low level on all outputs | | | | 0.4 | V | $I_{OL}$= 5 mA |
| $V_{OL}$ | Output low level on all outputs | | 0.4 | | | V | $I_{OL}$= 4 mA |
| $V_{OH}$ | Output high level | | | 2.4 | | V | $I_{OH}$= -5 mA |
| $V_{OH}$ | Output high level | 2.0 | | | | V | $I_{OH}$= -1 mA |
| $I_{IL}$ | Input leakage | | ±10 | | ±10 | µA | |
| $I_{CL}$ | Clock leakage | | ±10 | | ±10 | µA | |
| $I_{CC}$ | Avg power supply current | | 1.3 | | 3 | mA | |
| $C_P$ | Input capacitance | | 5 | | 5 | pF | |



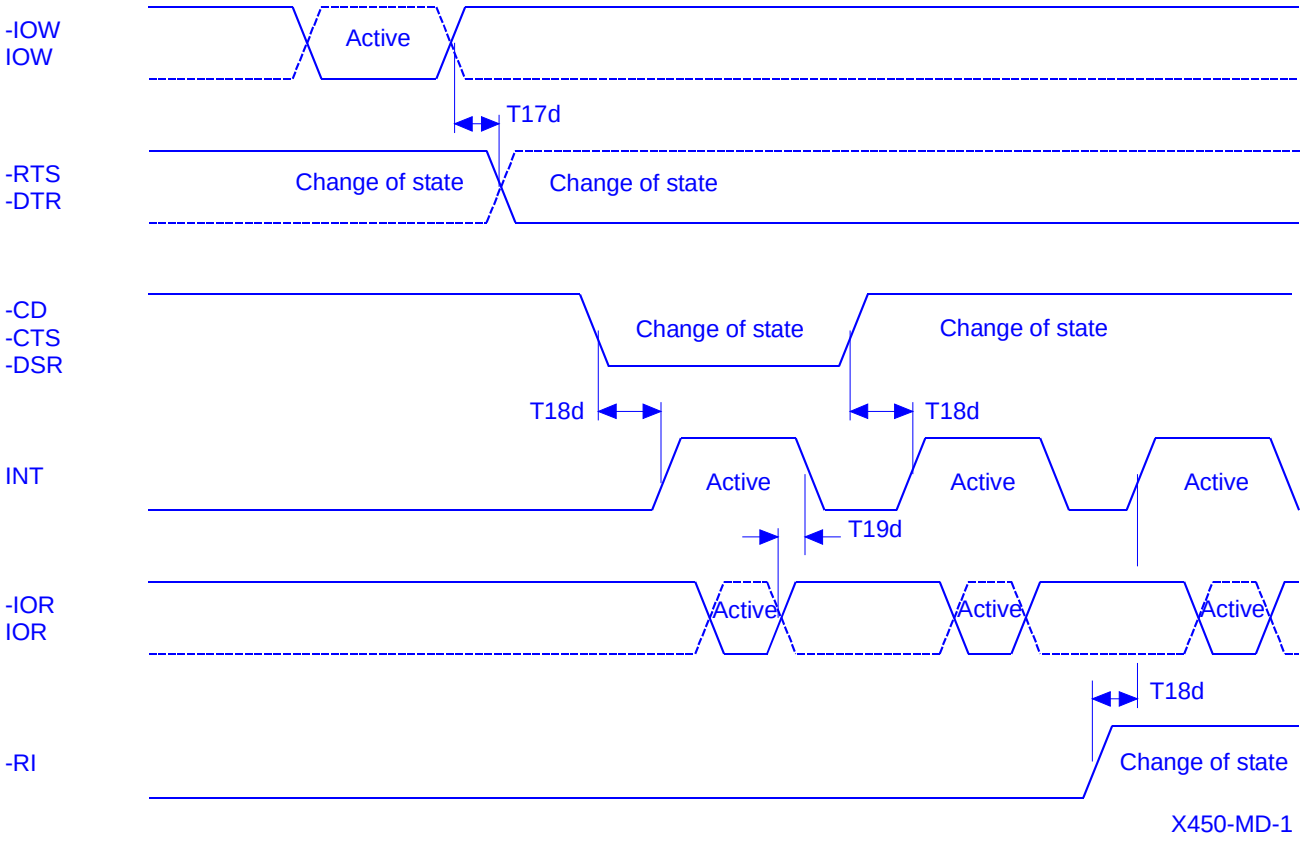

Clock timing



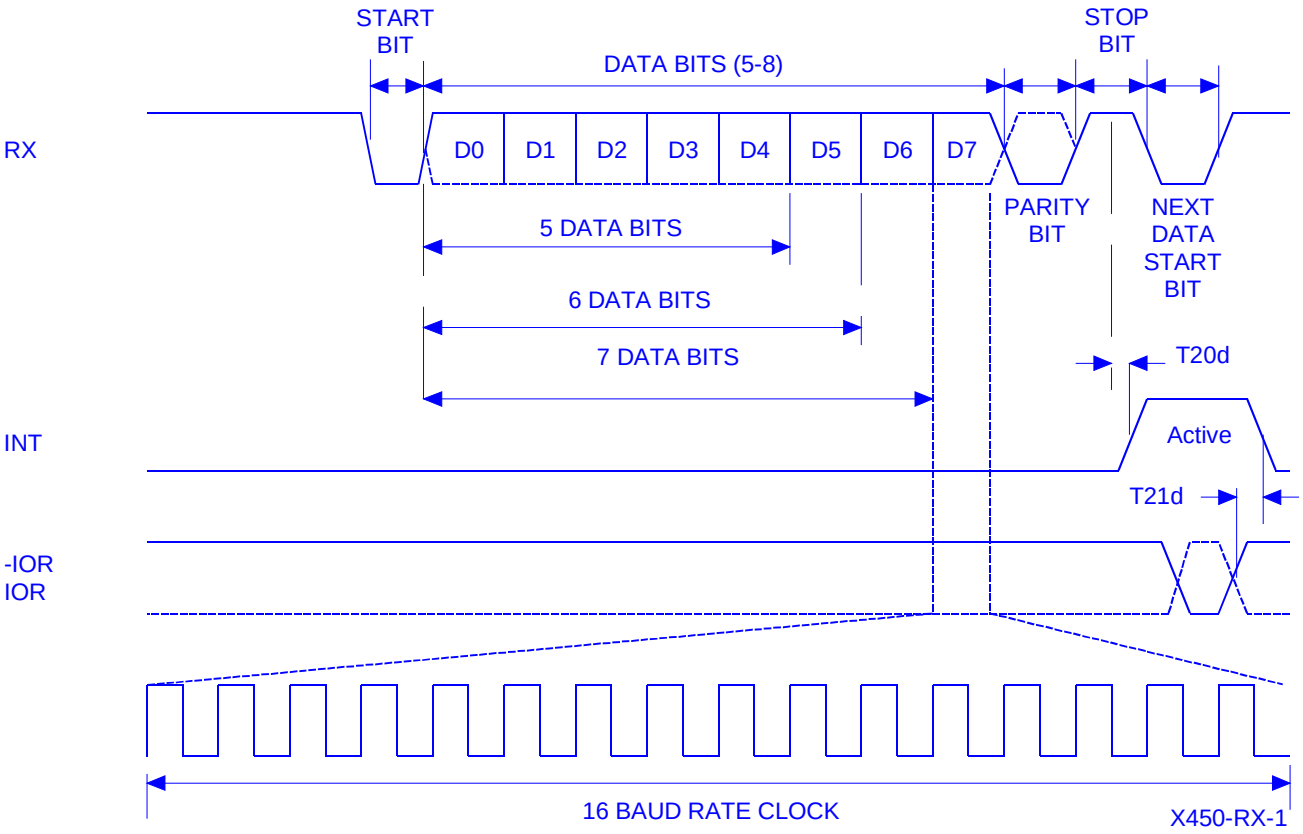

General read timing



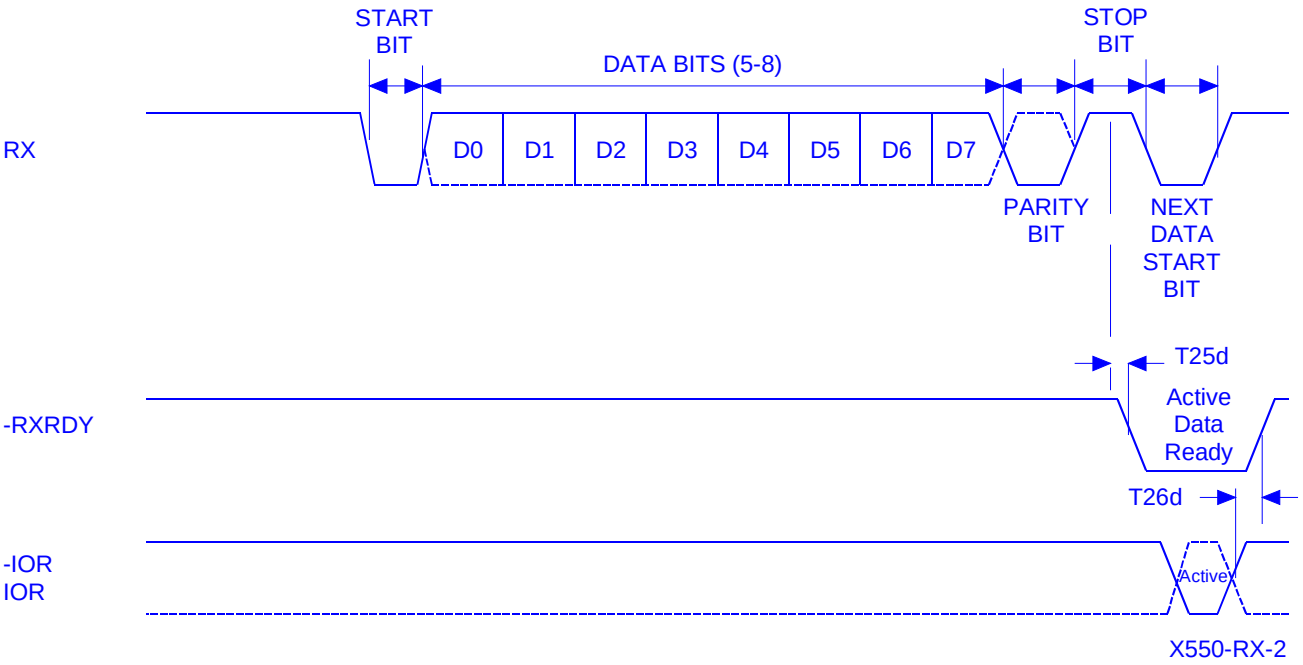

General write timing



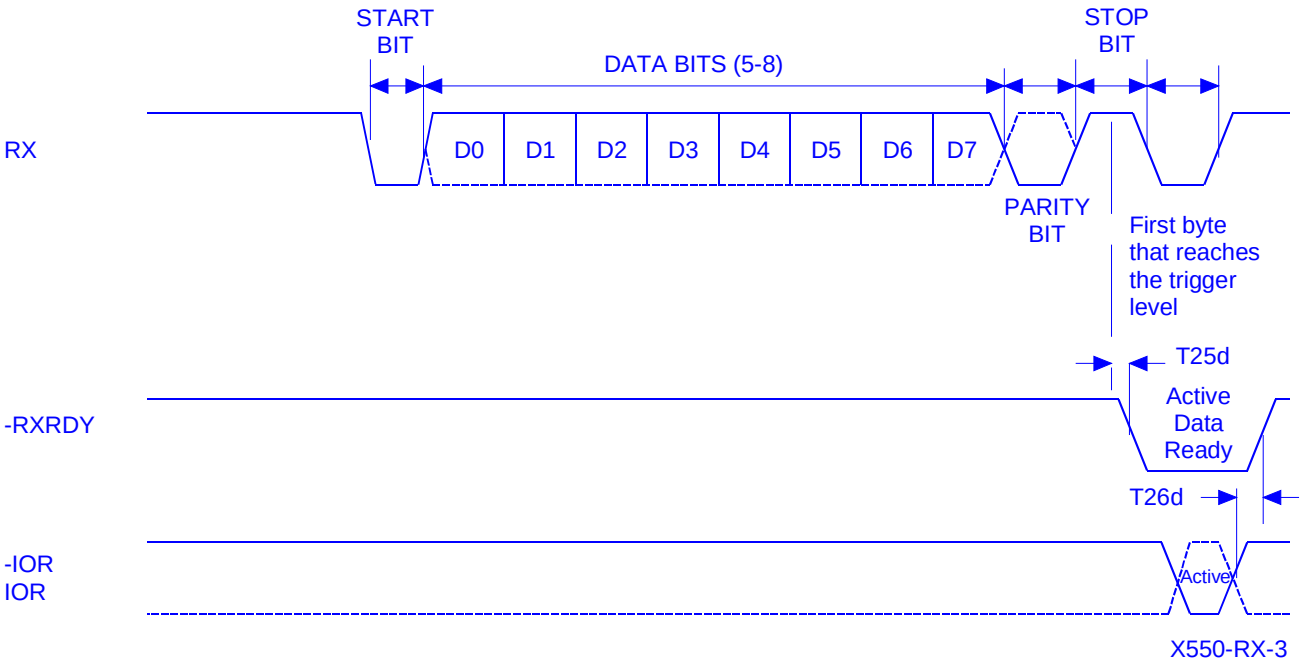

Modem input/output timing



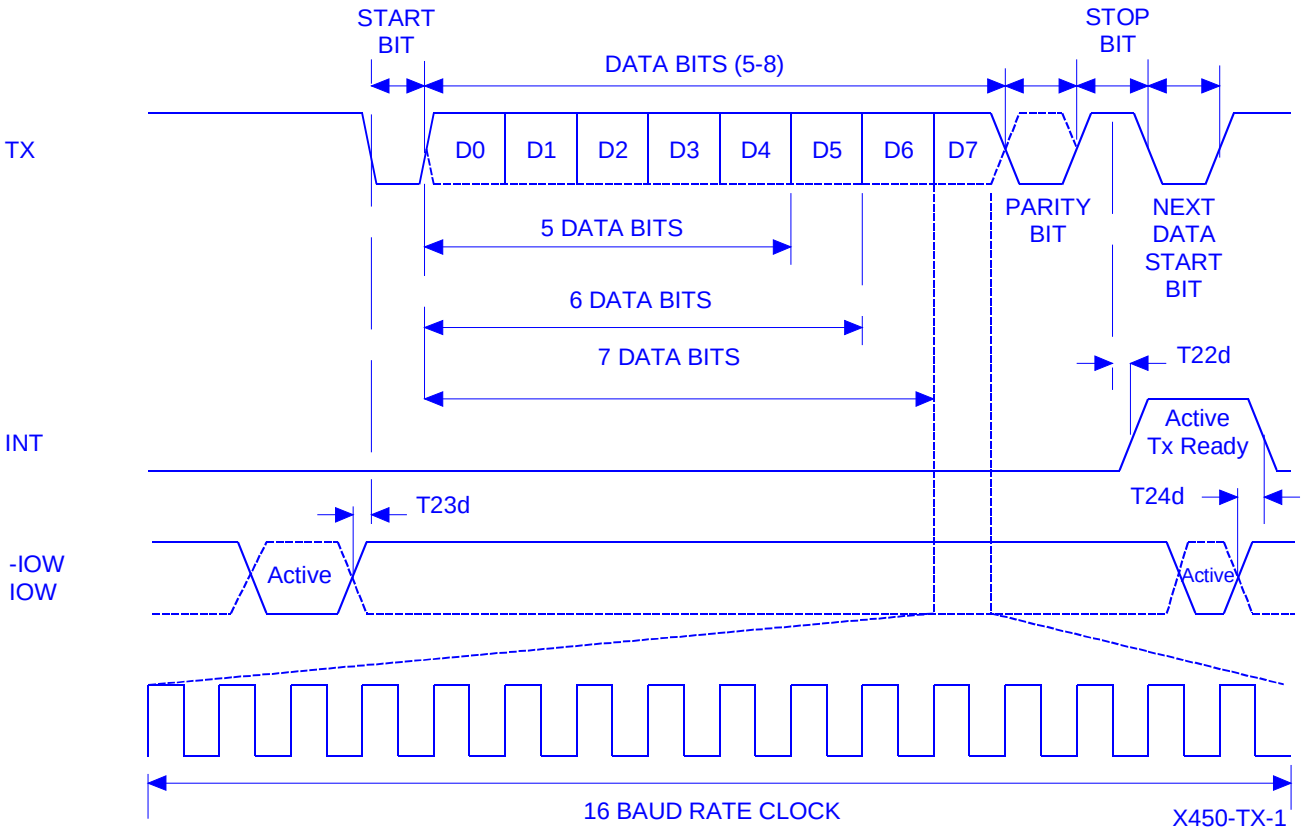

Receive timing



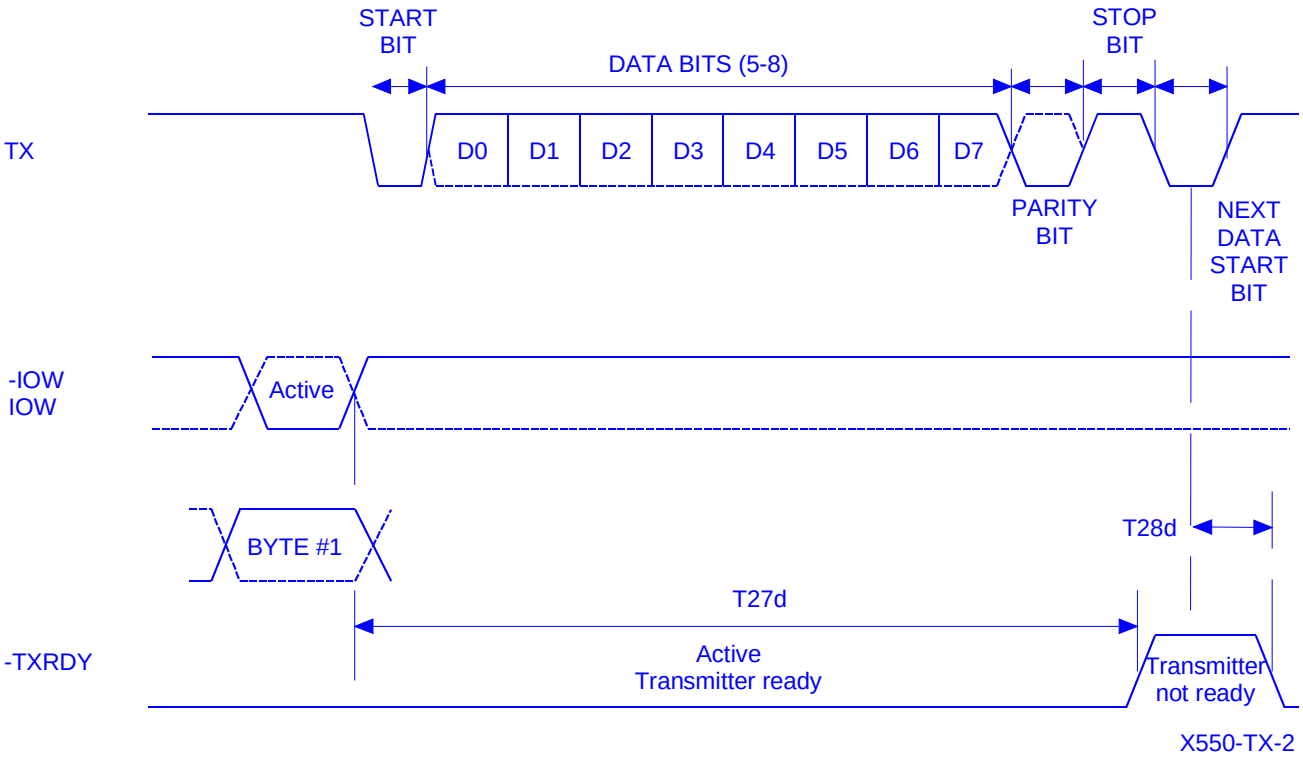

Receive ready timing in none FIFO mode



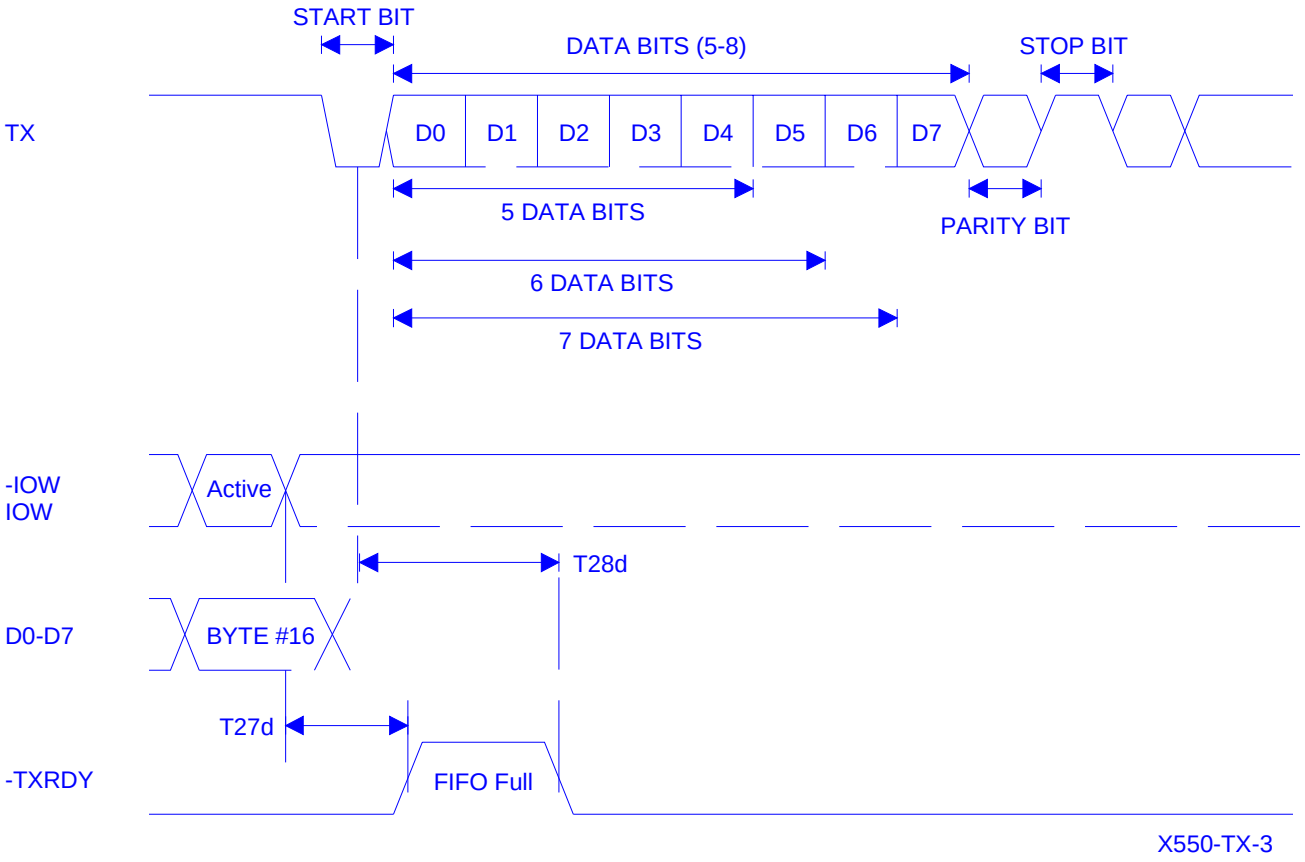

Receive ready timing in FIFO mode




Transmit timing



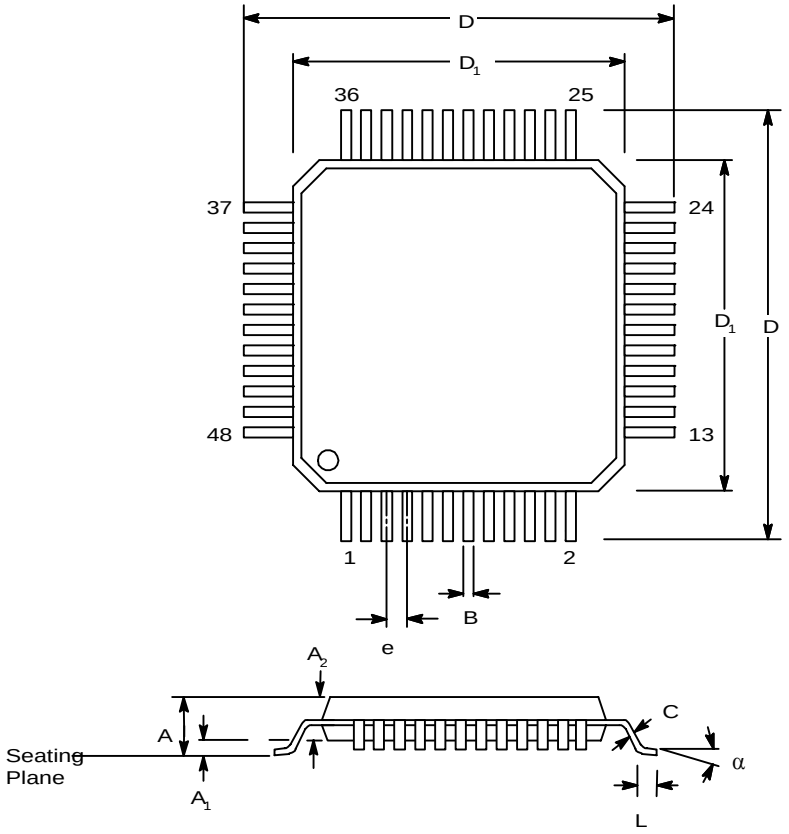

Transmit ready timing in none FIFO mode




Transmit ready timing in FIFO mode

## PACKAGE OUTLINE DRAWING

**48 LEAD THIN QUAD FLAT PACK**
**(TQFP)**




| *Note: The control dimension is the millimeter column* | | | | |
|---|---|---|---|---|
| SYMBOL | INCHES | | MILLIMETERS | |
| | MIN | MAX | MIN | MAX |
| A | 0.039 | 0.047 | 1.00 | 1.20 |
| $A_1$ | 0.002 | 0.006 | 0.05 | 0.15 |
| $A_2$ | 0.037 | 0.041 | 0.95 | 1.05 |
| B | 0.007 | 0.011 | 0.17 | 0.27 |
| C | 0.004 | 0.008 | 0.09 | 0.20 |
| D | 0.346 | 0.362 | 8.80 | 9.20 |
| $D_1$ | 0.272 | 0.280 | 6.90 | 7.10 |
| e | 0.20 BSC | | 0.50BSC | |
| L | 0.018 | 0.030 | 0.45 | 0.75 |
| α | 0° | 7° | 0° | 7° |

EXPLANATION OF DATA SHEET REVISIONS:

| FROM | TO | CHANGES | DATE |
|---|---|---|---|
| 1.10 | 1.20 | Added Patent Number. Added revision history.<br>Added Device Status to front page. | Sept 2003 |
| 1.20 | 1.21 | Corrected -AS pin description. | May 2005 |
| 1.21 | 1.22 | Removed discontinued packages (40-pin PDIP and 44-pin PLCC) from Ordering Information. | August 2005 |

**NOTICE**


Datasheet August 2005

Send your UART technical inquiry with technical details to hotline: *uarttechsupport@exar.com*