ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC}...+7V

Input Voltages

Logic.........................-0.3V to (Vcc + 0.5V)

Drivers......................-0.3V to (Vcc + 0.5V)

Receivers..+/-15V

Output Voltages

Logic.........................-0.3V to (Vcc + 0.5V)

Drivers..+/-15V

Receivers..................-0.3V to (Vcc + 0.5V)

Storage Temperature.......................-65˚C to +150˚C

Power Dissipation...500mW

ELECTRICAL CHARACTERISTICS

T_{MIN} to T_{MAX} and V_{CC} = +5.0V +/-5% unless otherwise noted.

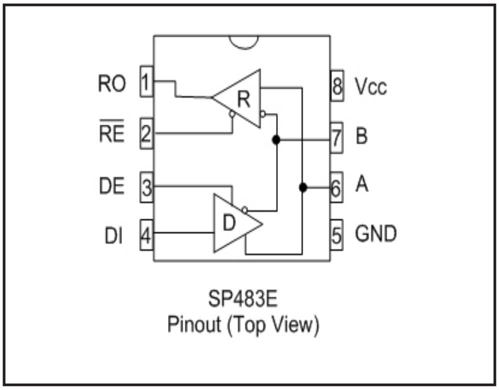
PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
SP483E DRIVER					
DC Characteristics					
Differential Output Voltage	GND		Vcc	Volts	Unloaded; R = ∞ ; See Figure 1
Differential Output Voltage	2		Vcc	Volts	With Load; R = 50Ω (RS-422); See Figure 1
Differential Output Voltage	1.5		Vcc	Volts	With Load; R = 27Ω (RS-485); See Figure 1
Change in Magnitude of Driver Differential Output Voltage for Complimentary states			0.2	Volts	R = 27Ω or R = 50Ω; See Figure 1
Driver Common Mode Output Voltage			3	Volts	R = 27Ω or R = 50Ω; See Figure 1
Input High Voltage	2.0			Volts	Applies to DE, DI, $\overline{RE}$
Input Low Voltage			0.8	Volts	Applies to DE, DI, $\overline{RE}$
Input Current, Driver Input			10	µA	Applies to DI
Input Current, Control Lines			1	µA	Applies to DE, $\overline{RE}$
Driver Short Circuit Current					
V_{OUT} = HIGH			+/-250	mA	$-7V \leq V_O \leq +12V$
V_{OUT} = LOW			+/-250	mA	$-7V \leq V_O \leq +12V$
SP483E DRIVER					
AC Characteristics					
Max. Transmission Rate	250			kbps	$\overline{RE}$ = 5V, DE = 5V; R_{DIFF} = 54Ω, $C_{L1} = C_{L2}$ = 100pF
Driver Input to Output, t_{PLH}	250	800	2000	ns	See Figures 3 & 5, R_{DIFF} = 54Ω, $C_{L1} = C_{L2}$ = 100pF
Driver Input to Output, t_{PHL}	250	800	2000	ns	See Figures 3 & 5, R_{DIFF} = 54Ω, $C_{L1} = C_{L2}$ = 100pF
Driver Skew		100	800	ns	See Figures 3 and 5, $t_{SKEW} = \lvert t_{DPHL} - t_{DPLH} \rvert$
Driver Rise or Fall Time	250		2000	ns	From 10%-90%; R_{DIFF} = 54Ω $C_{L1} = C_{L2}$ = 100pF; See Figures 3 and 6

T_{MIN} to T_{MAX} and V_{CC} = +5.0V +/-5% unless otherwise noted.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
SP483E DRIVER (continued)					
AC Characteristics					
Driver Enable to Output High	250		2000	ns	C_L = 100pF, See Figures 4 and 6, S_2 closed
Driver Enable to Output Low	250		2000	ns	C_L = 100pF, See Figures 4 and 6, S_1 closed
Driver Disable Time from High	300		3000	ns	C_L = 15pF, See Figures 4 and 6, S_2 closed
Driver Disable Time from Low	300		3000	ns	C_L = 15pF, See Figures 4 and 6, S_1 closed
SP483E RECEIVER					
DC Characteristics					
Differential Input Threshold	-0.2		+0.2	Volts	$-7V \leq V_{CM} \leq +12V$
Input Hysteresis		20		mV	V_{CM} = 0V
Output Voltage High	3.5			Volts	I_O = -4mA, V_{ID} = +200mV
Output Voltage Low			0.4	Volts	I_O = +4mA, V_{ID} = +200mV
Three-State (High Impedance) Output Current			+/-1	µA	$0.4V \leq V_O \leq 2.4V$; $\overline{RE}$ = 5V
Input Resistance	12	15		kΩ	$-7V \leq V_{CM} \leq +12V$
Input Current (A, B); V_{IN} = 12V			+1.0	mA	DE = 0V, V_{CC} = 0V or 5.25V, V_{IN} = 12V
Input Current (A, B); V_{IN} = -7V			-0.8	mA	DE = 0V, V_{CC} = 0V or 5.25V, V_{IN} = -7V
Short Circuit Current	7		95	mA	$0V \leq V_O \leq V_{CC}$
SP483E RECEIVER					
AC Characteristics					
Max. Transmission Rate	250			kbps	$\overline{RE}$ = 0V, DE = 0V
Receiver Input to Output	250		2000	ns	t_{PLH}; See Figures 3 & 7, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF
Receiver Input to Output	250		2000	ns	t_{PHL}; See Figures 3 & 7, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF
Differential Receiver Skew $\|t_{PHL} - t_{PLH}\|$		100		ns	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF, See Figures 3 and 7
Receiver Enable to Output Low		45	70	ns	C_{RL} = 15pF, Figures 2 & 8; S_1 Closed
Receiver Enable to Output High		45	70	ns	C_{RL} = 15pF, Figures 2 & 8; S_2 Closed
Receiver Disable from LOW		45	70	ns	C_{RL} = 15pF, Figures 2 & 8; S_1 Closed
Receiver Disable from High		45	70	ns	C_{RL} = 15pF, Figures 2 & 8; S_2 Closed

T_{MIN} to T_{MAX} and V_{CC} = +5.0V +/-5% unless otherwise noted.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
SP483E					
Shutdown Timing					
Time to Shutdown	50	200	600	ns	$\overline{RE}$ = 5V, DE = 0V
Driver Enable from Shutdown to Output High			2000	ns	C_L = 100pF; See Figures 4 and 6; S_2 Closed
Driver Enable from Shutdown to Output Low			2000	ns	C_L = 100pF; See Figures 4 and 6; S_1 Closed
Receiver Enable from Shutdown to Output High		300	2500	ns	C_L = 15pF; See Figures 2 and 8; S_2 Closed
Receiver Enable from Shutdown to Output Low		300	2500	ns	C_L = 15pF; See Figures 2 and 8; S_1 Closed
POWER REQUIREMENTS					
Supply Voltage V_{CC}	+4.75		+5.25	Volts	
Supply Current					
No Load		900		µA	$\overline{RE}$, DI = 0V or V_{CC}; DE = V_{CC}
		600		µA	$\overline{RE}$ = 0V, DI = 0V or 5V; DE = 0V
Shutdown Mode		1	10	µA	DE = 0V, $\overline{RE}$ = V_{CC}
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature					
Commercial (_C_)	0		70	ºC	
Industrial (_E_)	-40		+85	ºC	
Storage Temperature	-65		+150	ºC	
Package					
Plastic DIP (_P)					
NSOIC (_N)					



Pin 1 - RO - Receiver Output

Pin 2 - $\overline{RE}$ - Receiver Output Enable Active LOW

Pin 3 - DE - Driver Output Enable Active HIGH

Pin 4 - DI - Driver Input

Pin 5 - GND - Ground Connection

Pin 6 - A - Driver Output / Receiver input Non-Inverting

Pin 7 - B - Driver Output / Receiver Input Inverting

Pin 8 - Vcc - Positive Supply 4.75V ≤ Vcc ≤ 5.25V

TEST CIRCUITS

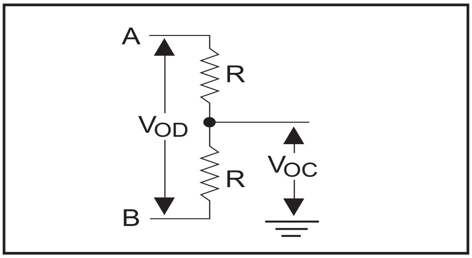


Figure 1. RS-485 Driver DC Test Load Circuit

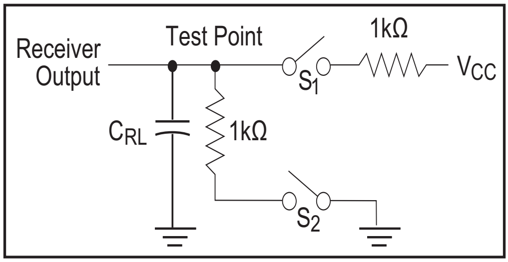


Figure 2. Receiver Timing Test Load Circuit

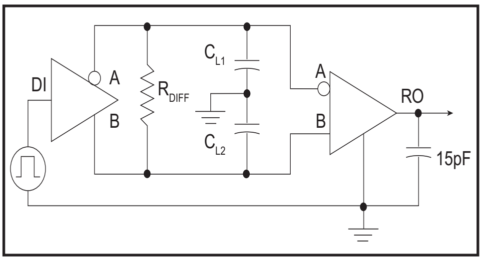


Figure 3. RS-485 Driver/Receiver Timing Test

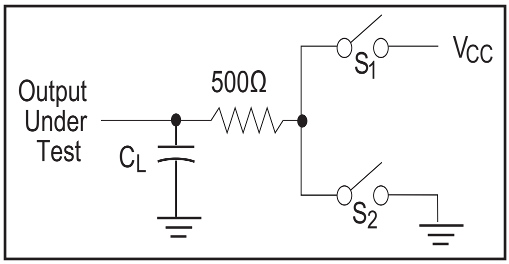


Figure 4. Driver Timing Test Load #2 Circuit

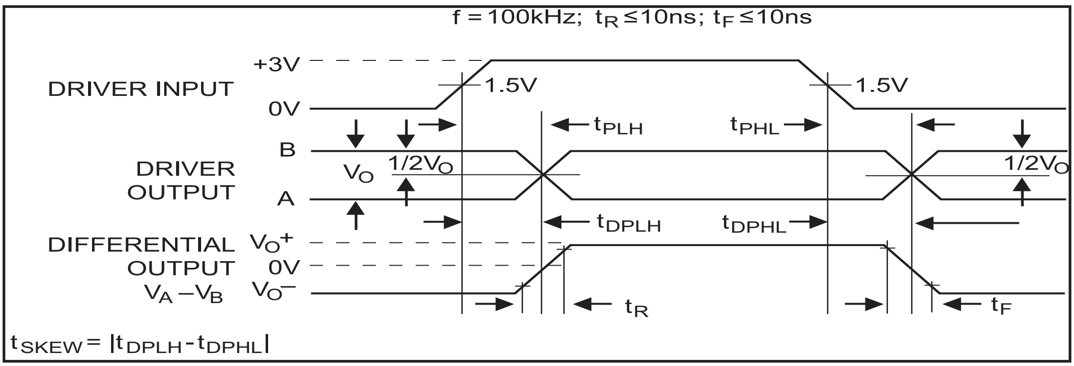


Figure 5. Driver Propagation Delays

FUNCTION TRUTH TABLES

INPUTS				OUTPUTS	
$\overline{RE}$	DE	DI	LINE CONDITION	A	B
X	1	1	No Fault	1	0
X	1	0	No Fault	0	1
X	0	X	X	Z	Z
X	1	X	Fault	Z	Z

Table 1. Transmit Function Truth Table

INPUTS			OUTPUTS
$\overline{RE}$	DE	A - B	R
0	0	+0.2V	1
0	0	-0.2V	0
0	0	Inputs Open	1
1	0	X	Z

Table 2. Receive Function Truth Table

SWITCHING WAVEFORMS

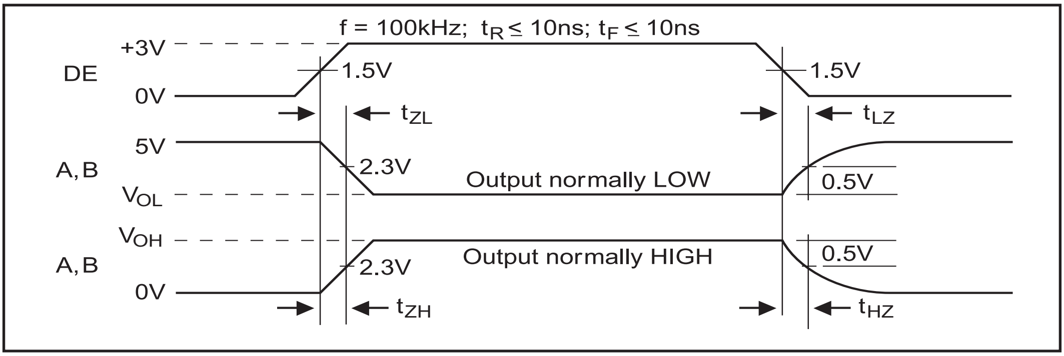


Figure 6. Driver Enable and Disable Times

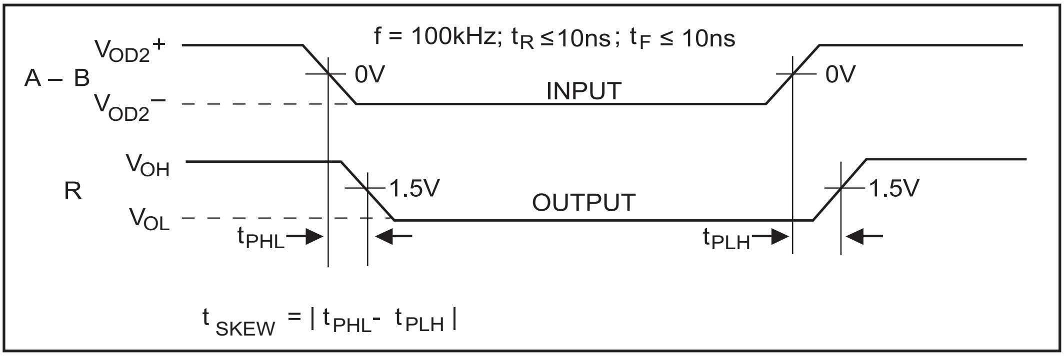


Figure 7. Receiver Propagation Delays

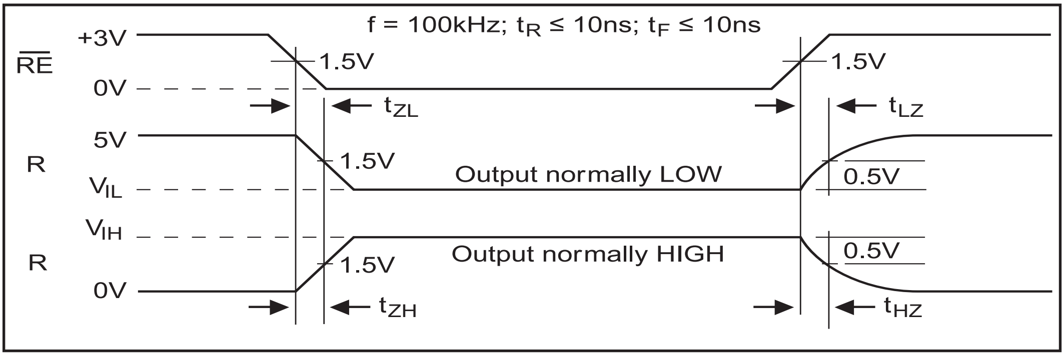


Figure 8. Receiver Enable and Disable Times

The **SP483E** is a half-duplex differential transceiver that meets the requirements of RS-485 and RS-422. Fabricated with an **Exar** proprietary BiCMOS process, this product requires a fraction of the power of older bipolar designs.

The RS-485 standard is ideal for multi-drop applications and for long-distance interfaces. RS-485 allows up to 32 drivers and 32 receivers to be connected to a data bus, making it an ideal choice for multi-drop applications. Since the cabling can be as long as 4,000 feet, RS-485 transceivers are equipped with a wide (-7V to +12V) common mode range to accommodate ground potential differences. Because RS-485 is a differential interface, data is virtually immune to noise in the transmission line.

Drivers

The driver outputs of the **SP483E** are differential outputs meeting the RS-485 and RS-422 standards. The typical voltage output swing with no load will be 0 Volts to +5 Volts. With worst case loading of 54Ω across the differential outputs, the drivers can maintain greater than 1.5V voltage levels. The drivers have an enable control line which is active HIGH. A logic HIGH on DE (pin 3) will enable the differential driver outputs. A logic LOW on the DE (pin 3) will tri-state the driver outputs.

The **SP483E** has internally slew rate limited driver outputs to minimize EMI. The maximum data rate for the **SP483E** drivers is 250kbps under load.

Receivers

The **SP483E** receivers have differential inputs with an input sensitivity as low as ±200mV. Input impedance of the receivers is typically 15kΩ (12kΩ minimum). A wide common mode range of -7V to +12V allows for large ground potential differences between systems. The receivers have a tri-state enable control pin. A logic LOW on $\overline{RE}$ (pin 2) will enable the receiver, a logic HIGH on $\overline{RE}$ (pin 2) will disable the receiver.

The **SP483E** receiver is rated for data rates up to 250kbps. The receivers are equipped with the fail-safe feature. Fail-safe guarantees that the receiver output will be in a HIGH state when the input is left unconnected.

Shutdown Mode

The **SP483E** is equipped with a Shutdown mode. To enable the shutdown state, both driver and receiver must be disabled simultaneously. A logic LOW on DE (pin 3) and a Logic HIGH on $\overline{RE}$ (pin 2) will put the **SP483E** into Shutdown mode. In Shutdown, supply current will drop to typically 1µA.

ESD TOLERANCE

The **SP483E** incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electro-static discharges and associated transients. The improved ESD tolerance is at least ±15kV without damage or latch-up.

There are different methods of ESD testing applied:

a) MIL-STD-883, Method 3015.7
b) IEC61000-4-2 Air-Discharge
c) IEC61000-4-2 Direct Contact

The Human Body Model has been the generally accepted ESD testing method for semiconductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in Figure 9. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the IC's tend to be handled frequently. The IEC61000-4-2, formerly IEC801-2, is generally used for testing ESD on equipment and systems.

For system manufacturers, they must guarantee a certain amount of ESD protection since the system itself is exposed to the outside environment and human presence. The premise with IEC61000-4-2 is that the system is required to withstand an amount of static electricity when ESD is applied to points and surfaces of the equipment that are accessible to personnel during normal usage. The transceiver IC receives most of the ESD current when the ESD source is applied to the connector pins. The test circuit for IEC61000-4-2 is shown on Figure 10. There are two methods within IEC61000-4-2, the Air Discharge method and the Contact Discharge method.

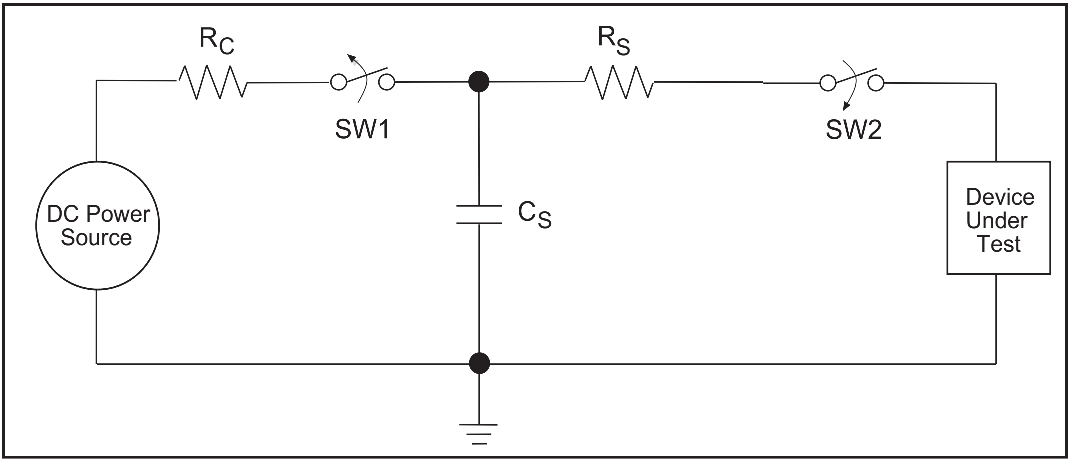


Figure 9. ESD Test Circuit for Human Body Model

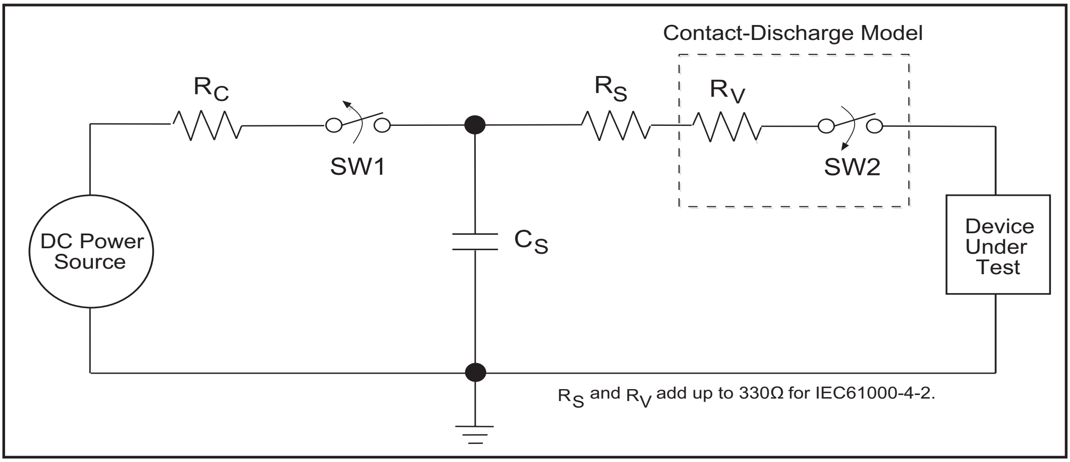


Figure 10. ESD Test Circuit for IEC61000-4-2

With the Air Discharge Method, an ESD voltage is applied to the equipment under test (EUT) through air. This simulates an electrically charged person ready to connect a cable onto the rear of the system only to find an unpleasant zap just before the person touches the back panel. The high energy potential on the person discharges through an arcing path to the rear panel of the system before he or she even touches the system. This energy, whether discharged directly or through air, is predominantly a function of the discharge current rather than the discharge voltage. Variables with an air discharge such as approach speed of the object carrying the ESD potential to the system and humidity will tend to change the discharge current. For example, the rise time of the discharge current varies with the approach speed.

The Contact Discharge Method applies the ESD current directly to the EUT. This method was devised to reduce the unpredictability of the ESD arc. The discharge current rise time is constant since the energy is directly transferred without the air-gap arc. In situations such as hand held systems, the ESD charge can be directly discharged to the equipment from a person already holding the equipment. The current is transferred on to the keypad or the serial port of the equipment directly and then travels through the PCB and finally to the IC.

The circuit model in Figures 9 and 10 represent the typical ESD testing circuit used for all three methods. The C_S is initially charged with the DC power supply when the first switch (SW1) is on. Now that the capacitor is charged, the second switch (SW2) is on while SW1 switches off.

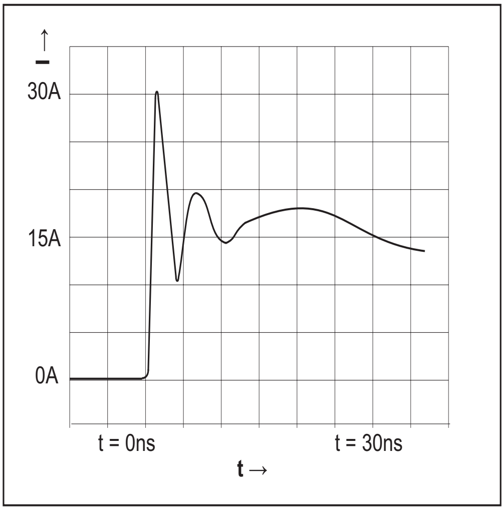


Figure 11. ESD Test Waveform for IEC61000-4-2

The voltage stored in the capacitor is then applied through R_S, the current limiting resistor, onto the device under test (DUT). In ESD tests, the SW2 switch is pulsed so that the device under test receives a duration of voltage.

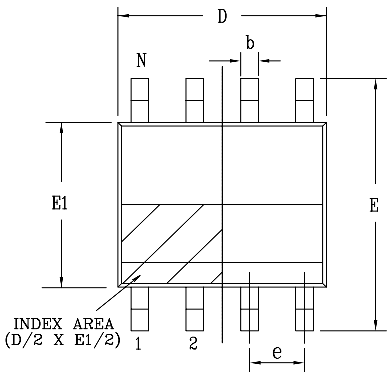
For the Human Body Model, the current limiting resistor (R_S) and the source capacitor (C_S) are 1.5kΩ an 100pF, respectively. For IEC-61000-4-2, the current limiting resistor (R_S) and the source capacitor (C_S) are 330Ω an 150pF, respectively.

The higher C_S value and lower R_S value in the IEC61000-4-2 model are more stringent than the Human Body Model. The larger storage capacitor injects a higher voltage to the test point when SW2 is switched on. The lower current limiting resistor increases the current charge onto the test point.

DEVICE PIN TESTED	HUMAN BODY MODEL	IEC61000-4-2		
		Air Discharge	Direct Contact	Level
Driver Outputs	+/-15kV	+/-15kV	+/-8kV	4
Receiver Inputs	+/-15kV	+/-15kV	+/-8kV	4

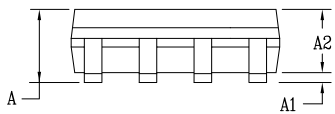
Table 1. Transceiver ESD Tolerance levels

REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	08/16/05	JL
B	DRAWING FORMAT MODIFICATION	07/19/06	JL
C	CHANGE DRAWING LOGO ADN COMPANY NAME	11/16/07	JL

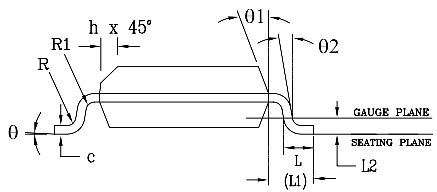


Top View

8 Pin SOICN JEDEC MS-012 Variation AA						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	—	1.75	0.053	—	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	1.25	—	1.65	0.049	—	0.065
b	0.31	—	0.51	0.012	—	0.020
c	0.17	—	0.25	0.007	—	0.010
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25	—	0.50	0.010	—	0.020
L	0.40	—	1.27	0.016	—	0.050
L1	1.04 REF			0.041 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
θ2	0°	—	—	0°	—	—
D	4.90 BSC			0.193 BSC		
N	8			8		



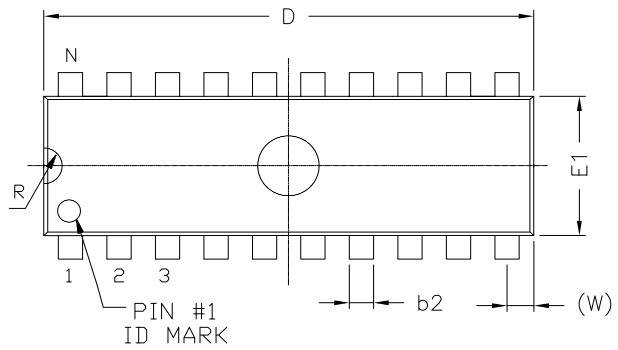
Side View



Front View

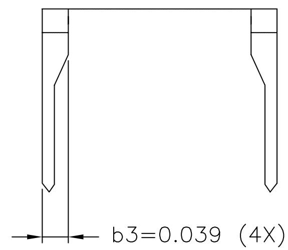
EXAR CORPORATION			
8 PIN SOICN PACKAGE OUTLINE			
Packaging Approval:		Drawing No:	8-PIN SOICN
By: JL	Date: 11/16/07	Revision: C	Sheet: 1 OF 1

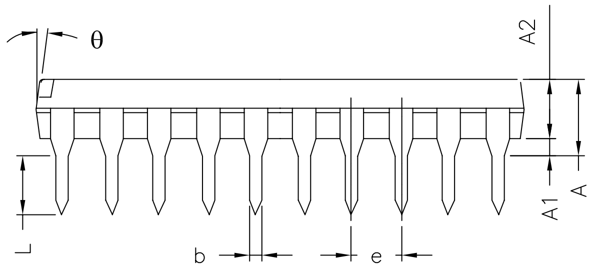
REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	04/26/06	JL
B	CHNAGE DRAWING LOGO AND COMPANY NAME	11/28/07	JL



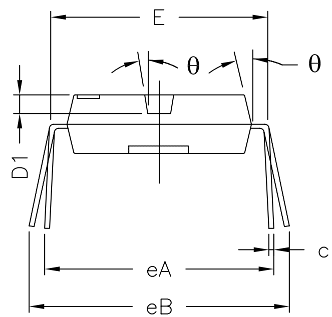
Top View

REMARKS:
FOR 8LD AND 16LD
ALL END LEADS (4X)
ARE HALF LEAD TYPES





Side View



Front View

8 Pin PDIP JEDEC MS-001 Variation BA						
SYMBOLS	DIMENSIONS IN INCH (Control Unit)			DIMENSIONS IN MM (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	0.210	—	—	5.33
A1	0.015	—	—	0.38	—	—
A2	0.115	0.130	0.195	2.92	3.30	4.95
b	0.014	0.018	0.022	0.36	0.46	0.56
b2	0.045	0.060	0.070	1.14	1.52	1.78
c	0.008	0.010	0.014	0.20	0.25	0.36
D1	0.030	—	0.060	0.76	—	1.52
E	0.300	0.310	0.325	7.62	7.87	8.26
E1	0.240	0.250	0.280	6.10	6.35	7.11
e	0.100 BSC			2.54 BSC		
eA	0.300 BSC			7.62 BSC		
eB	—	—	0.430	—	—	10.92
L	0.115	0.130	0.150	2.92	3.30	3.81
W	0.075 REF			1.91 REF		
R	0.030 BSC			0.76 BSC		
θ	4°	7°	10°	4°	7°	10°
D	0.355	0.365	0.400	9.02	9.27	10.16
N	8			8		

EXAR Powering Connectivity	EXAR CORPORATION		
	8 PIN PDIP PACKAGE OUTLINE		
Packaging Approval:	Drawing No: 8-PIN PDIP		
By: JL	Date: 11/28/07	Revision: B	Sheet: 1 OF 1

ORDERING INFORMATION

Model	Temperature Range	Package Types
SP483ECN-L	0°C to +70°C	8-pin NSOIC
SP483ECN-L/TR	0°C to +70°C	8-pin NSOIC
SP483EEN-L	-40°C to +85°C	8-pin NSOIC
SP483EEN-L/TR	-40°C to +85°C	8-pin NSOIC
SP483ECP-L	0°C to +70°C	8-pin PDIP
SP483EEP-L	-40°C to +85°C	8-pin PDIP

Note: /TR = Tape and Reel

REVISION HISTORY

DATE	REVISION	DESCRIPTION
2000	05	Legacy Sipex Datasheet
02/09/12	1.0.0	Convert to Exar Format. Update ordering information. Change ESD specification to IEC61000-4-2.

Datasheet February 2012

Send your serial transceiver technical questions with technical details to: serialtechsupport@exar.com