

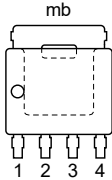
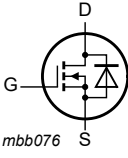
N-channel 25 V, 2.09 mΩ, 179 A logic level MOSFET in LFPAK56 using NextPowerS3 Technology

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 12 V; V _{GS} = 10 V; Fig. 12; Fig. 13	-	34.1	-	nC
		I _D = 25 A; V _{DS} = 12 V; V _{GS} = 4.5 V; Fig. 12; Fig. 13	-	15.7	-	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V	-	15.2	-	nC
Q _{GD}	gate-drain charge	I _D = 25 A; V _{DS} = 12 V; V _{GS} = 4.5 V; Fig. 12; Fig. 13	-	3.6	-	nC
Source-drain diode						
S	softness factor	I _S = 25 A; dI _S /dt = -100 A/s; V _{GS} = 0 V; V _{DS} = 12 V; Fig. 16	-	1	-	

[1] 179A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LFPAK56; Power-SO8 (SOT669)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN2R0-25YLD	LFPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN2R0-25YLD	2D025L

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	25	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$		-	25	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	115	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	179	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2		-	127	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3		-	722	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
V_{ESD}	electrostatic discharge voltage	HBM (JEDEC)		600	-	V
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$		-	95	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$		-	722	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 25\text{ A}$; $V_{sup} \leq 25\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; $t_p = 1.01\text{ ms}$		-	410	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} = 25\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; $R_{GS} = 50\text{ }\Omega$	[2]	-	118	A

[1] 179A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

[2] Protected by 100% test

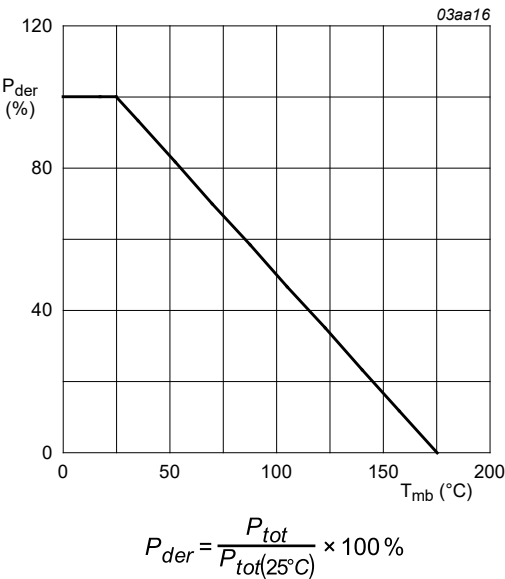
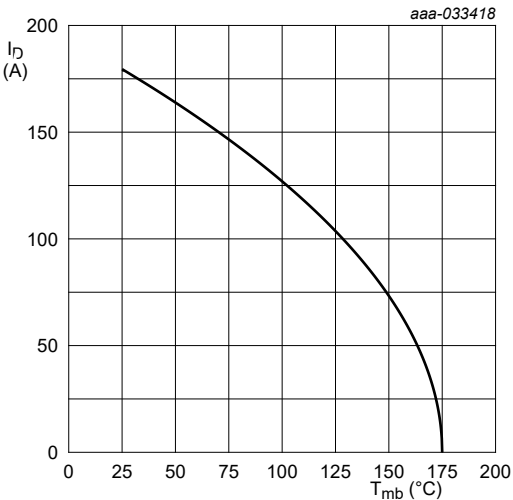


Fig. 1. Normalized total power dissipation as a function of mounting base temperature



$V_{GS} \geq 10\text{ V}$
(1) 179A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 2. Continuous drain current as a function of mounting base temperature

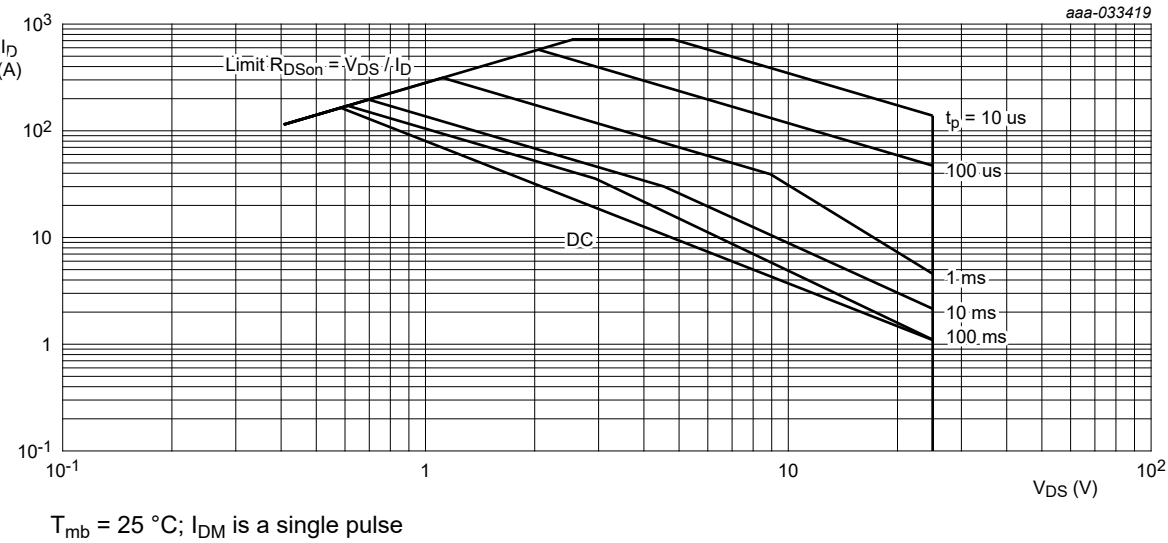


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	1.09	1.31	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5	-	50	-	K/W
		Fig. 6	-	125	-	K/W

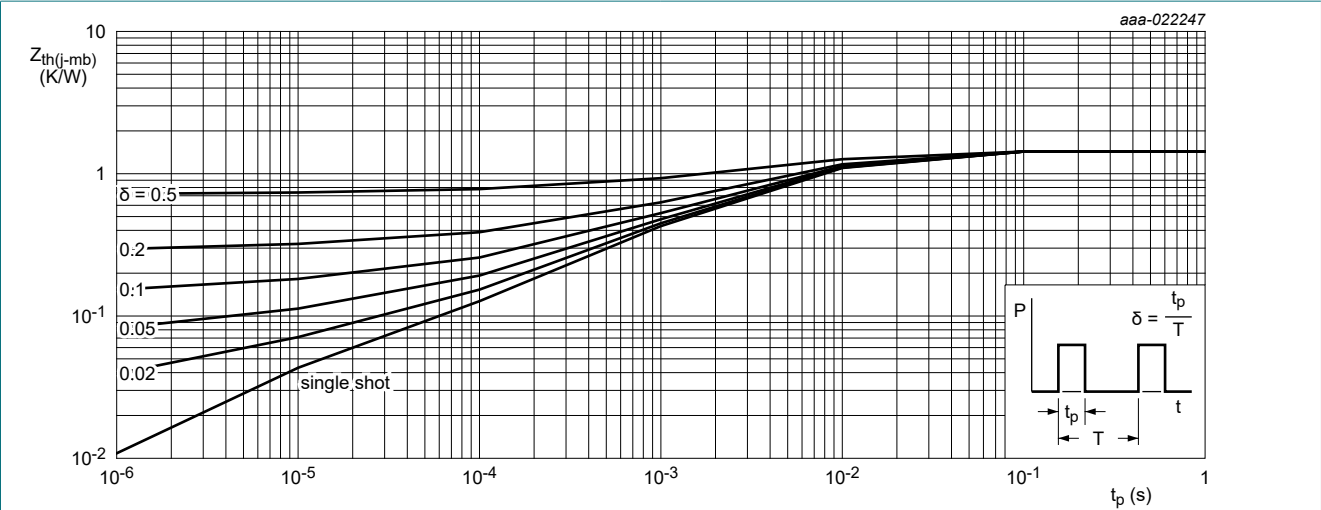


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

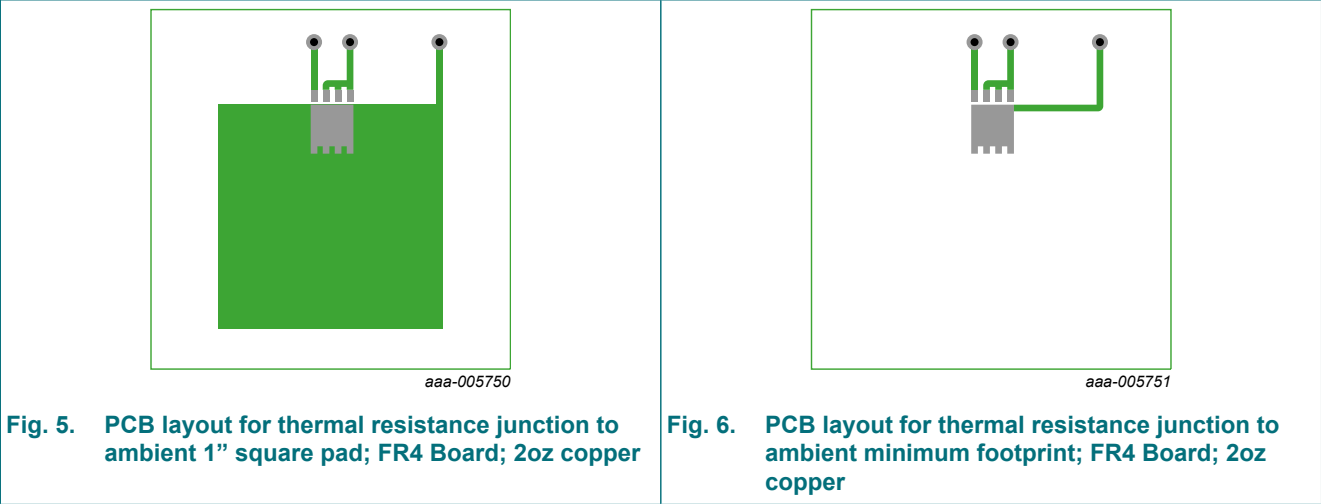


Fig. 5. PCB layout for thermal resistance junction to ambient 1” square pad; FR4 Board; 2oz copper

Fig. 6. PCB layout for thermal resistance junction to ambient minimum footprint; FR4 Board; 2oz copper

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C	25	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C	22.5	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} =V _{GS} ; T _j = 25 °C	1.2	1.68	2.2	V
ΔV _{GS(th)} /ΔT	gate-source threshold voltage variation with temperature	25 °C ≤ T _j ≤ 175 °C	-	-4.5	-	mV/K
I _{DSS}	drain leakage current	V _{DS} = 20 V; V _{GS} = 0 V; T _j = 25 °C	-	-	1	μA
		V _{DS} = 20 V; V _{GS} = 0 V; T _j = 125 °C	-	3.9	-	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	-	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	-	100	nA

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 25 A; T _J = 25 °C; Fig. 10		-	2.41	2.91	mΩ
		V _{GS} = 4.5 V; I _D = 25 A; T _J = 175 °C; Fig. 10 ; Fig. 11		-	-	4.95	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 25 °C; Fig. 10		-	1.82	2.09	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 175 °C; Fig. 10 ; Fig. 11		-	-	3.52	mΩ
R _G	gate resistance	f = 1 MHz		-	0.849	-	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 12 V; V _{GS} = 10 V; Fig. 12 ; Fig. 13		-	34.1	-	nC
		I _D = 25 A; V _{DS} = 12 V; V _{GS} = 4.5 V; Fig. 12 ; Fig. 13		-	15.7	-	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V		-	15.2	-	nC
Q _{GS}	gate-source charge	I _D = 25 A; V _{DS} = 12 V; V _{GS} = 4.5 V; Fig. 12 ; Fig. 13		-	6.4	-	nC
Q _{GS(th)}	pre-threshold gate-source charge			-	3.8	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge			-	2.6	-	nC
Q _{GD}	gate-drain charge			-	3.6	-	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 25 A; V _{DS} = 12 V; Fig. 12 ; Fig. 13		-	2.8	-	V
C _{iss}	input capacitance	V _{DS} = 12 V; V _{GS} = 0 V; f = 1 MHz; T _J = 25 °C; Fig. 14		-	2485	-	pF
C _{oss}	output capacitance			-	1142	-	pF
C _{rss}	reverse transfer capacitance			-	152	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 12 V; R _L = 0.6 Ω; V _{GS} = 4.5 V; R _{G(ext)} = 5 Ω		-	15.7	-	ns
t _r	rise time			-	18.7	-	ns
t _{d(off)}	turn-off delay time			-	18.7	-	ns
t _f	fall time			-	12.4	-	ns
Q _{oss}	output charge	V _{GS} = 0 V; V _{DS} = 12 V; f = 1 MHz; T _J = 25 °C		-	23	-	nC
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 20 A; V _{GS} = 0 V; T _J = 25 °C; Fig. 15		-	0.8	1.2	V
t _{rr}	reverse recovery time	I _S = 25 A; dI _S /dt = -100 A/s; V _{GS} = 0 V; V _{DS} = 12 V; Fig. 16		-	26	-	ns
Q _r	recovered charge		[1]	-	16.8	-	nC
t _a	reverse recovery rise time			-	13	-	ns
t _b	reverse recovery fall time			-	13	-	ns
S	softness factor			-	1	-	

[1] Includes capacitive recovery

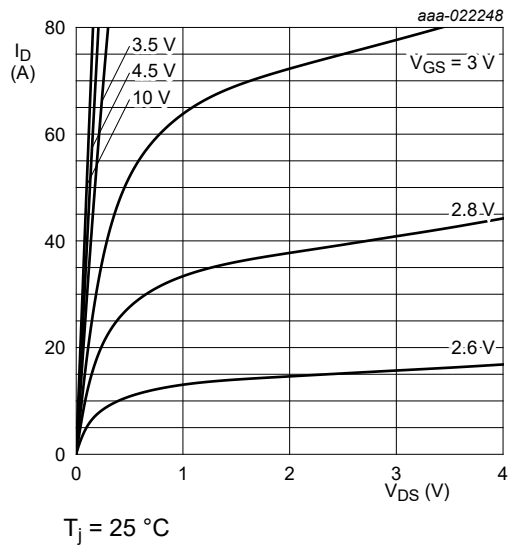


Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values

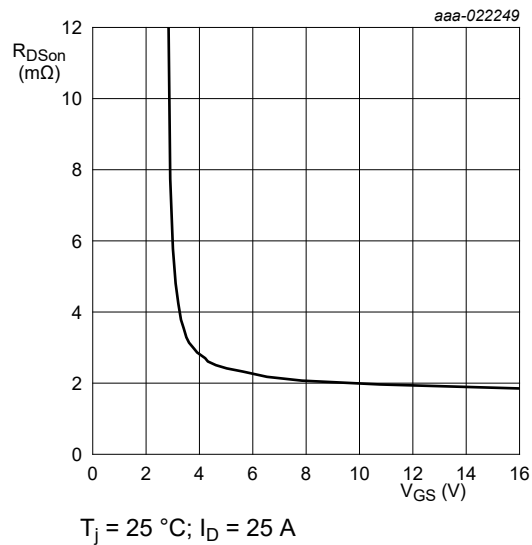


Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

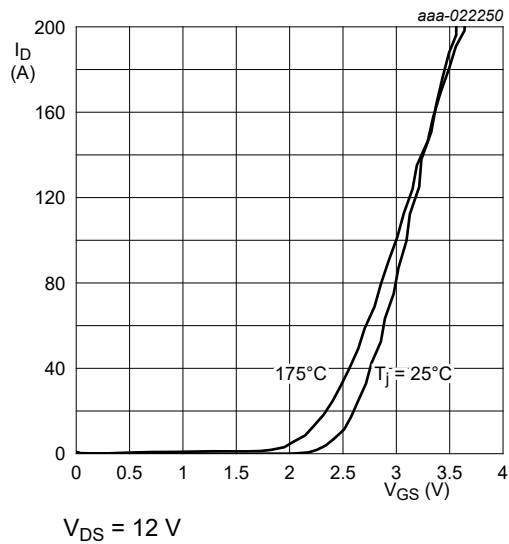


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

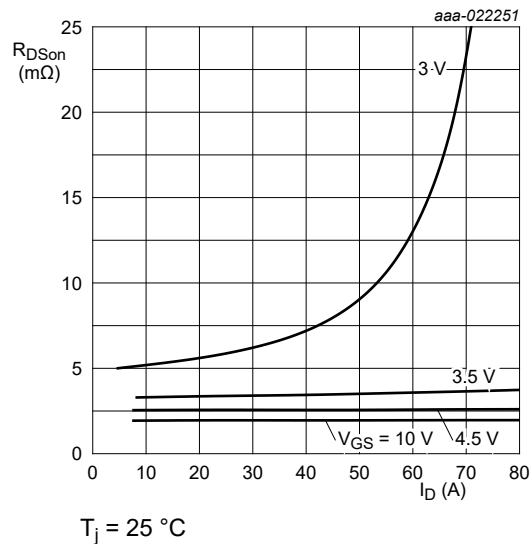


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

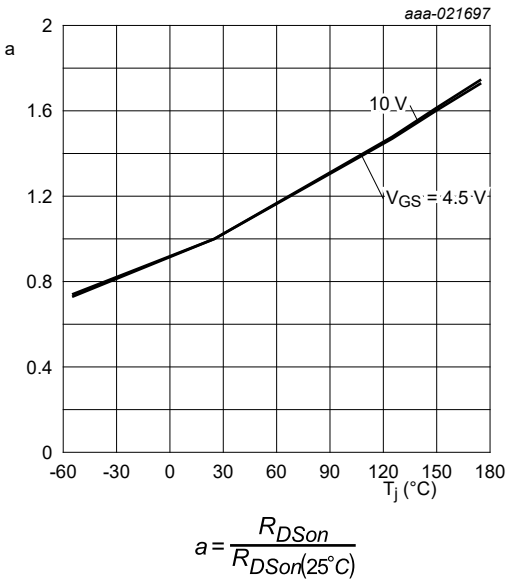


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

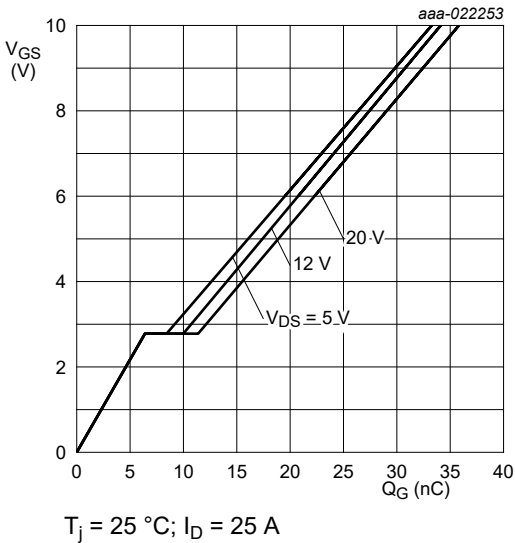


Fig. 12. Gate-source voltage as a function of gate charge; typical values

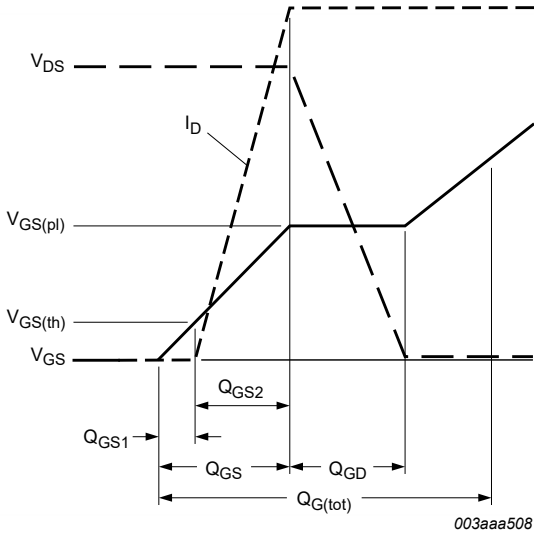


Fig. 13. Gate charge waveform definitions

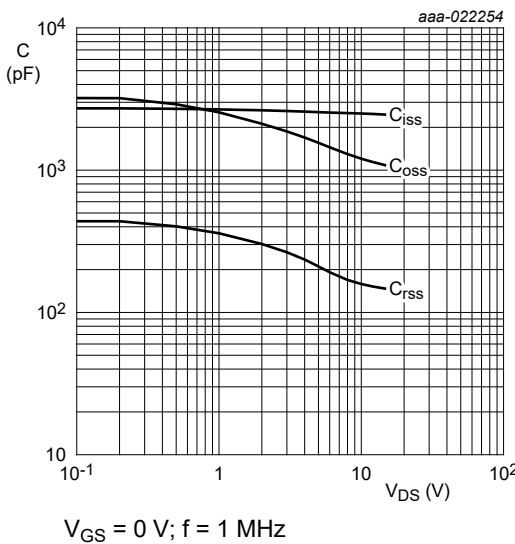


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

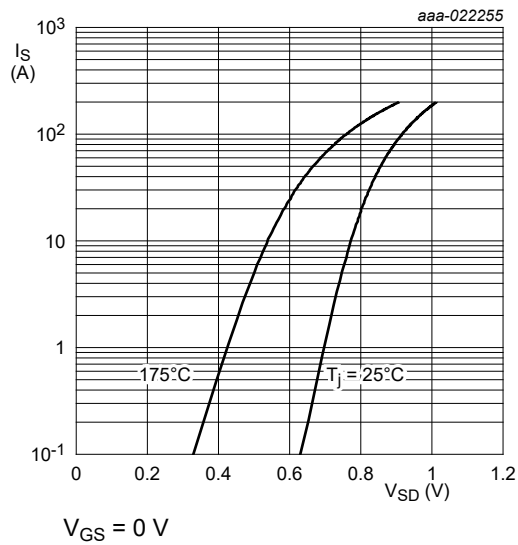


Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

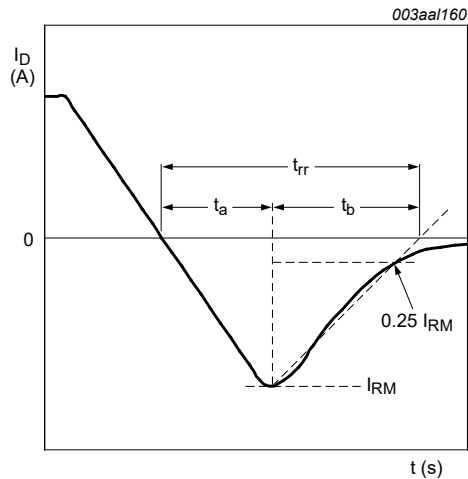


Fig. 16. Reverse recovery timing definition

11. Package outline

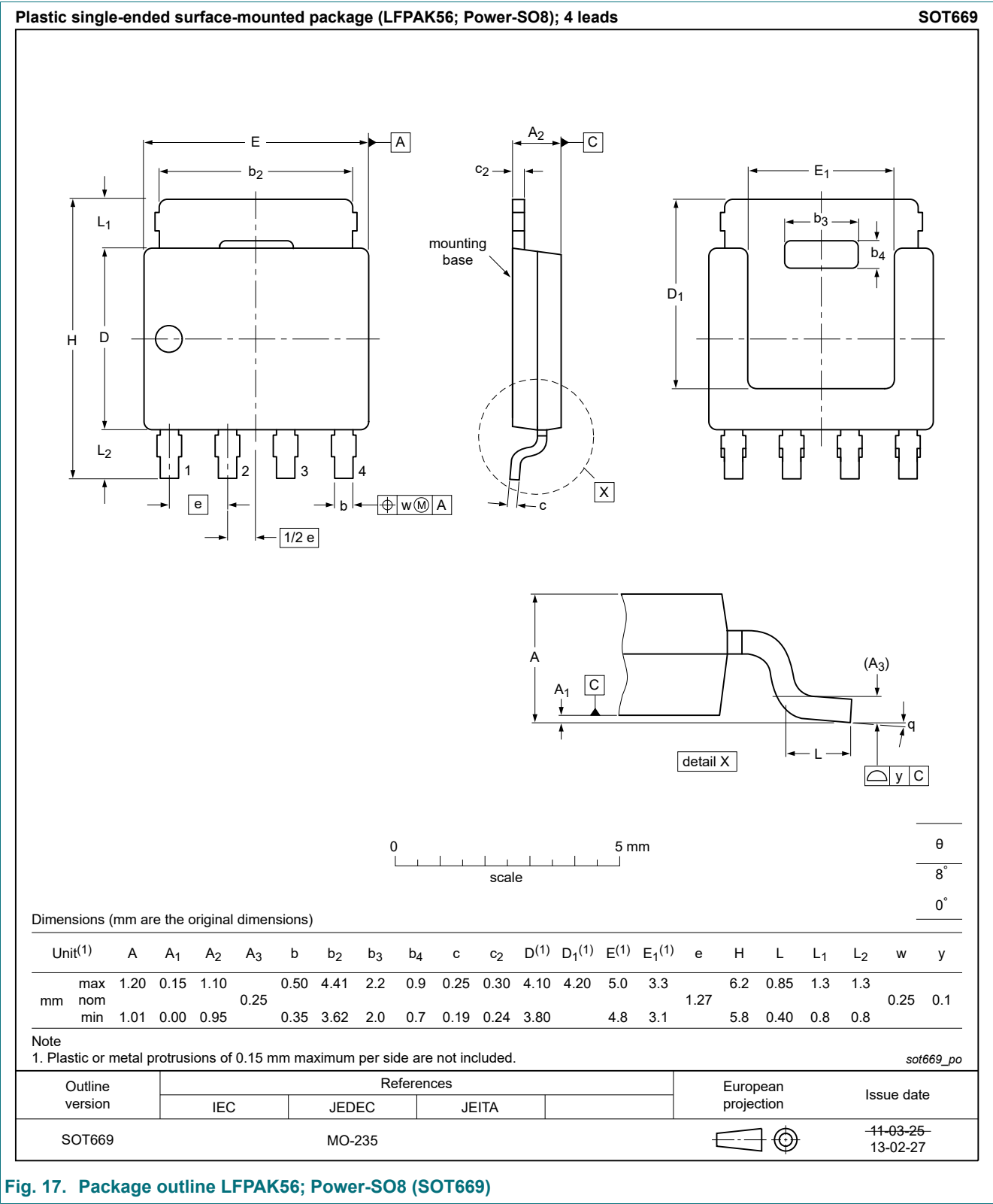


Fig. 17. Package outline LPAK56; Power-SO8 (SOT669)

12. Soldering

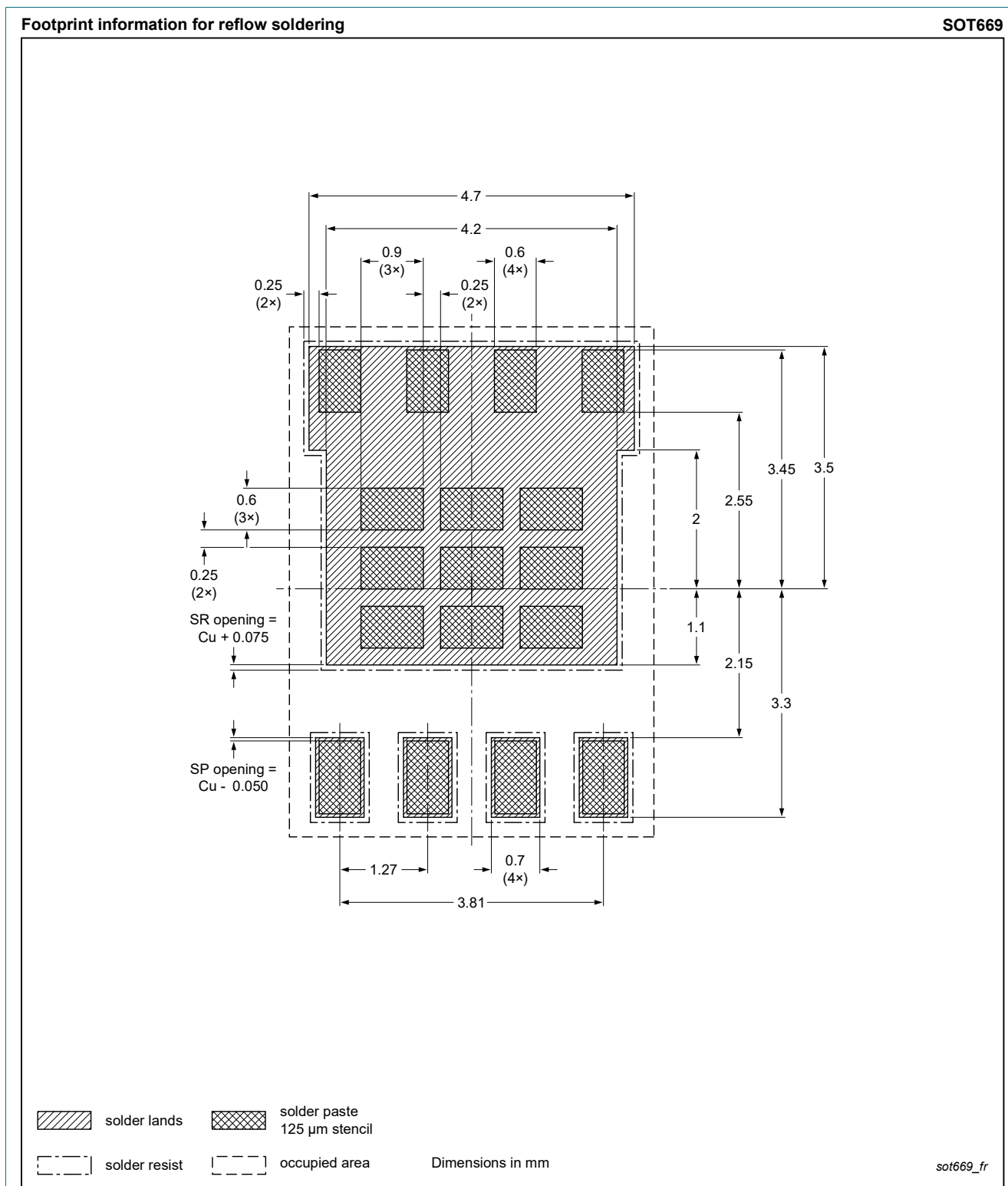


Fig. 18. Reflow soldering footprint for LPAK56; Power-SO8 (SOT669)

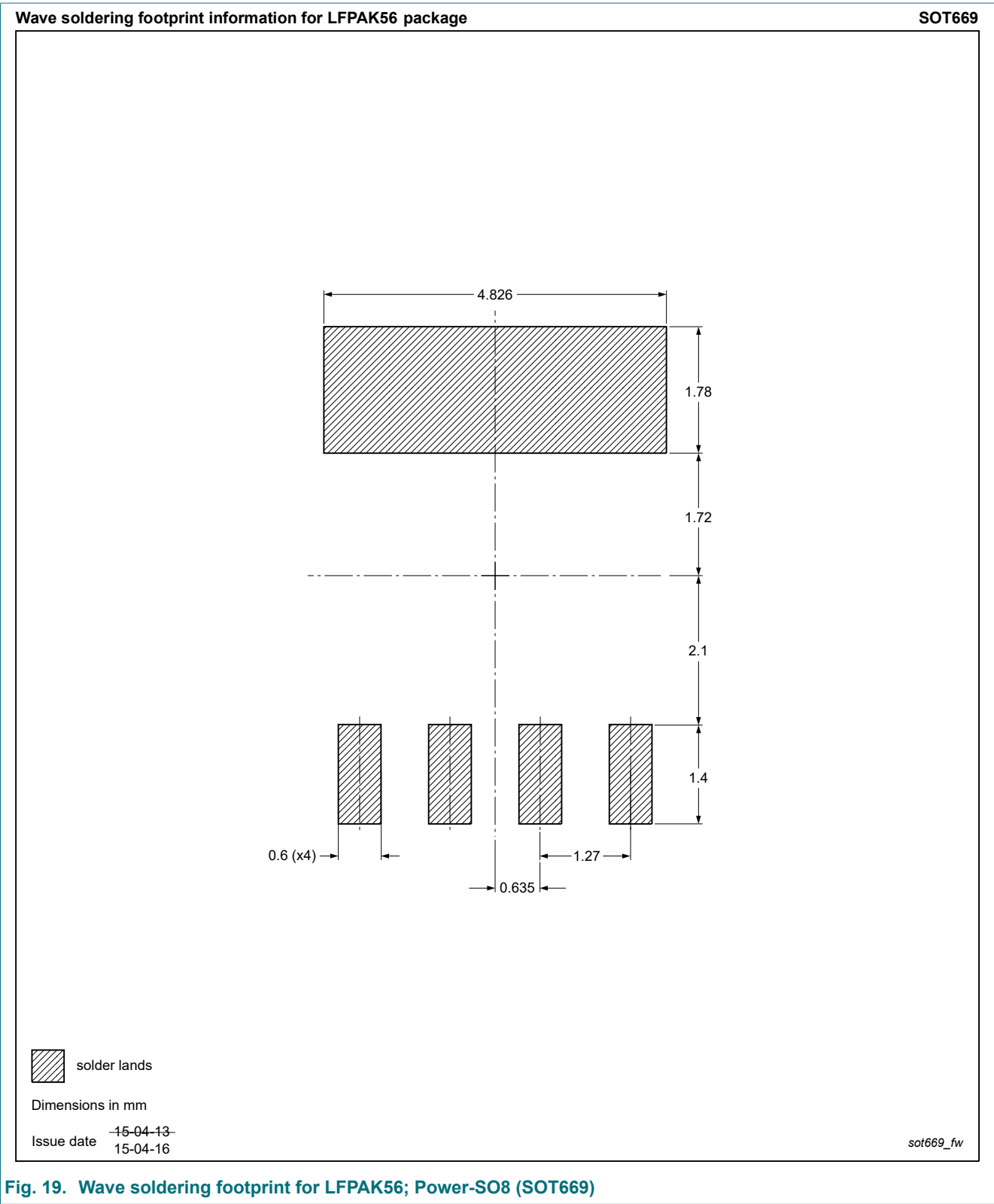


Fig. 19. Wave soldering footprint for LPAK56; Power-SO8 (SOT669)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Date of release: 23 April 2021