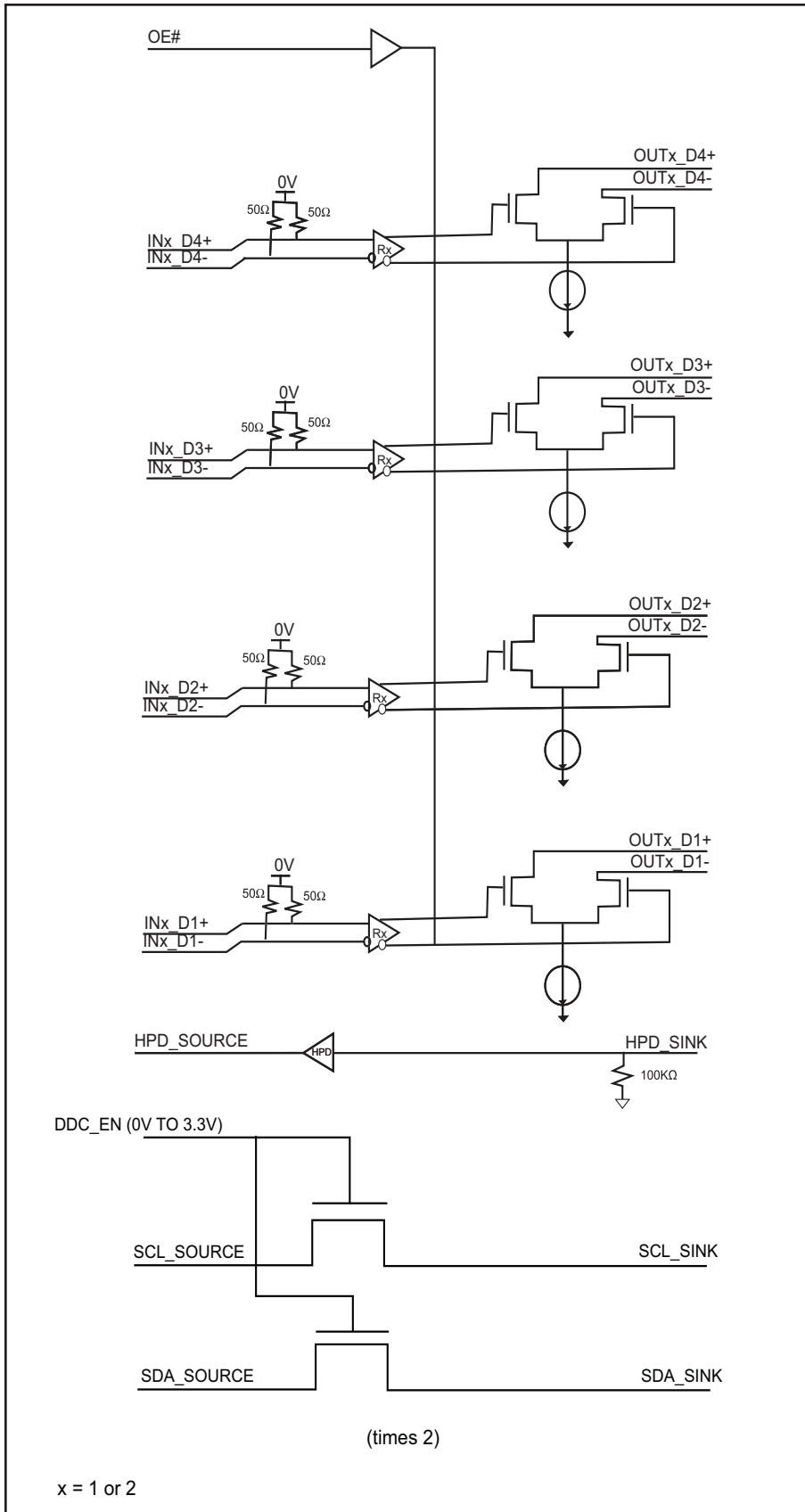


Block Diagram



x = 1 or 2

Maximum Ratings (Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature.....	-65°C to +150°C
Supply Voltage to Ground Potential.....	-0.5V to +5V
DC Input Voltage.....	-0.5V to V _{DD}
DC Output Current	120mA
Power Dissipation	1.0W

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 2: Signal Descriptions

Pin Name	Type	Description									
OE#	5.5V tolerant low-voltage single-ended input	Enable for level shifter path									
		<table border="1"> <thead> <tr> <th>OE#</th> <th>IN_D Termination</th> <th>OUT_D Outputs</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>>100KΩ</td> <td>High-Z</td> </tr> <tr> <td>0</td> <td>50Ω</td> <td>Active</td> </tr> </tbody> </table>	OE#	IN_D Termination	OUT_D Outputs	1	>100KΩ	High-Z	0	50Ω	Active
		OE#	IN_D Termination	OUT_D Outputs							
1	>100KΩ	High-Z									
0	50Ω	Active									
IN_D4+	Differential input	Low-swing diff input from GMCH PCIE outputs. IN_D4+ makes a differential pair with IN_D4-.									
IN_D4-	Differential input	Low-swing diff input from GMCH PCIE outputs. IN_D4- makes a differential pair with IN_D4+.									
IN_D3+	Differential input	Low-swing diff input from GMCH PCIE outputs. IN_D3+ makes a differential pair with IN_D3-.									
IN_D3-	Differential input	Low-swing diff input from GMCH PCIE outputs. IN_D3- makes a differential pair with IN_D3+.									
IN_D2+	Differential input	Low-swing diff input from GMCH PCIE outputs. IN_D2+ makes a differential pair with IN_D2-.									
IN_D2-	Differential input	Low-swing diff input from GMCH PCIE outputs. IN_D2- makes a differential pair with IN_D2+.									
IN_D1+	Differential input	Low-swing diff input from GMCH PCIE outputs. IN_D1+ makes a differential pair with IN_D1-.									
IN_D1-	Differential input	Low-swing diff input from GMCH PCIE outputs. IN_D1- makes a differential pair with IN_D1+.									
OUT_D4+	TMDS Differential output	HDMI 1.3 compliant TMDS output. OUT_D4+ makes a differential output signal with OUT_D4-.									
OUT_D4-	TMDS Differential output	HDMI 1.3 compliant TMDS output. OUT_D4- makes a differential output signal with OUT_D4+.									
OUT_D3+	TMDS Differential output	HDMI 1.3 compliant TMDS output. OUT_D3+ makes a differential output signal with OUT_D3-.									
OUT_D3-	TMDS Differential output	HDMI 1.3 compliant TMDS output. OUT_D3- makes a differential output signal with OUT_D3+.									

(Continued)

Pin Name	Type	Description						
OUT_D2+	TMDS Differential output	HDMI 1.3 compliant TMDS output. OUT_D2+ makes a differential output signal with OUT_D2-.						
OUT_D2-	TMDS Differential output	HDMI 1.3 compliant TMDS output. OUT_D2- makes a differential output signal with OUT_D2+.						
OUT_D1+	TMDS Differential output	HDMI 1.3 compliant TMDS output. OUT_D1+ makes a differential output signal with OUT_D1-.						
OUT_D1-	TMDS Differential output	HDMI 1.3 compliant TMDS output. OUT_D1- makes a differential output signal with OUT_D1+.						
HPD_SINK	5V tolerance single-ended input	Low Frequency, 0V to 5V (nominal) input signal. This signal comes from the HDMI connector. Voltage High indicates "plugged" state; voltage low indicated "unplugged". HPD_SINK is pulled down by an integrated 100K ohm put-down resistor.						
HPD_SOURCE	3.3V single-ended output	HPD_SOURCE: 0V to 3.3V (nominal) output signal. This is level-shifted version of the HPD_SINK signal.						
SCL_SOURCE	Single-ended 3.3V open-drain DDC I/O	3.3V DDC Data I/O. Pulled up by external termination to 3.3V. Connected to SCL_SINK through voltage-limiting integrated NMOS passgate.						
SDA_SOURCE	Single-ended 3.3V open-drain DDC I/O	3.3V DDC Data I/O. Pulled up by external termination to 3.3V. Connected to SDA_SINK through voltage-limiting integrated NMOS passgate.						
SCL_SINK	Single-ended 5V open-drain DDC I/O	5V DDC Clock I/O. Pulled up by external termination to 5V. Connected to SCL_SOURCE through voltage-limiting integrated NMOS passgate.						
SDA_SINK	Single-ended 5V open-drain DDC I/O	5V DDC Data I/O. Pulled up by external termination to 5V. Connected to SDA_SOURCE through voltage-limiting integrated NMOS passgate.						
DDC_EN	5.0V tolerant Single-ended input	Enables bias voltage to the DDC passgate level shifter gates. (May be implemented as a bias voltage connection to the DDC pass gates themselves.) <table border="1" data-bbox="808 1486 1507 1633"> <tr> <td>DDC_EN</td> <td>Passgate</td> </tr> <tr> <td>0V</td> <td>Disabled</td> </tr> <tr> <td>3.3V</td> <td>Enabled</td> </tr> </table>	DDC_EN	Passgate	0V	Disabled	3.3V	Enabled
DDC_EN	Passgate							
0V	Disabled							
3.3V	Enabled							
VDD	3.3V DC Supply	3.3V ± 10%						
OC_2 (REXT)	3.3V single-ended control input	Acceptable connections to OC_1 (REXT) pin are: Resistor to GND; Resistor to 3.3V; NC. (Resistor should be 0-ohm).						

Pin Name	Type	Description
OC_3	Analog connection to external component or supply	Acceptable connections to OC_3 pin are: short to 3.3V or to GND; NC.
OC_0 OC_1 EQ_0 EQ_1	Output and Input jitter elimination control	Control pins are to enable Jitter elimination features. For normal operation these pins are tied GND or to VDD. Please see the truth tables for more information.

Truth Table 1

OC_3 ⁽²⁾	OC_2 ⁽¹⁾	OC_1 ⁽¹⁾	OC_0 ⁽¹⁾	Vswing (mV)	Pre/De-emphasis
0	0	0	0	500	0
0	0	0	1	600	0
0	0	1	0	750	0
0	0	1	1	1000	0
0	1	0	0	500	0
0	1	0	1	500	1.5dB
0	1	1	0	500	3.5dB
0	1	1	1	500	6dB
1	0	0	0	400	0
1	0	0	1	400	3.5dB
1	0	1	0	400	6dB
1	0	1	1	400	9dB
1	1	0	0	1000	0
1	1	0	1	1000	-3.5dB
1	1	1	0	1000	-6dB
1	1	1	1	1000	-9dB

Truth Table 2

EQ_1 ⁽²⁾	EQ_0 ⁽¹⁾	Equalization @ 1.25GHz (dB)
0	0	3
0	1	6
1	0	9
1	1	12

Notes:

- 1) These signals have internal 100kΩ pull-ups.
- 2) For 42-TQFN package, these signals are internally connected to GND directly.
 For 48-TQFN package, these signals have internal 100kΩ pull-ups, with external connection.

Electrical Characteristics
Table 3: Power Supplies and Temperature Range

Symbol	Parameter	Min	Nom	Max	Units	Comments
VDD	3.3V Power Supply	3.0	3.3	3.6	V	
ICC	Max Current			100	mA	Total current from VDD 3.3V supply when de-emphasis/pre-emphasis is set to 0dB.
ICCQ	Standby Current Consumption			2	mA	OE# = HIGH
TCASE	Case temperature range for operation with spec.	-40		85	Celcius	

Table 4: OE# Description

OE#	Device State	Comments
Asserted (low voltage)	Differential input buffers and output buffers enabled. Input impedance = 50Ω	Normal functioning state for IN_D to OUT_D level shifting function.
Unasserted (high voltage)	<p>Low-power state.</p> <p>Differential input buffers and termination are disabled. Differential inputs are in a high-impedance state.</p> <p>OUT_D level-shifting outputs are disabled.</p> <p>OUT_D level-shifting outputs are in high-impedance state.</p> <p>Internal bias currents are turned off.</p>	<p>Intended for lowest power condition when:</p> <ul style="list-style-type: none"> No display is plugged in or The level shifted data path is disabled <p>HPD_SINK input and HPD_SOURCE output are not affected by OE# SCL_SOURCE, SCL_SINK, SDA_SOURCE and SDA_SINK signals and functions are not affected by OE#</p>

Table 5: Differential Input Characteristics for IN_D and RX_IN signals

Symbol	Parameter	Min	Nom	Max	Units	Comments
Tbit	Unit Interval	360			ps	Tbit is determined by the display mode. Nominal bit rate ranges from 250Mbps to 2.5Gbps per lane. Nominal Tbit at 2.5 Gbps=400ps. 360ps=400ps-10%
V _{RX-DIFFp-p}	Differential Input Peak to Peak Voltage	0.175		1.200	V	$V_{RX-DIFFp-p} = 2 V_{RX-D+} \times V_{RX-D-} $ Applies to IN_D and RX_IN signals
T _{RX-EYE}	Minimum Eye Width at IN_D input pair	0.8			Tbit	The level shifter may add a maximum of 0.02UI jitter
V _{CM-AC-pp}	AC Peak Common Mode Input Voltage			100	mV	$V_{CM-AC-pp} = V_{RX-D+} + V_{RX-D-} /2 - V_{RX-CM-DC}$. $V_{RX-CM-DC} = DC(avg) \text{ of } V_{RX-D+} + V_{RX-D-} /2$ VCM-AC-pp includes all frequencies above 30 kHz.
Z _{RX-DC}		40	50	60	Ω	Required IN_D+ as well as IN_D- DC impedance (50Ω ± 20% tolerance).
V _{RX-Bias}		0		2.0	V	Intended to limit power-up stress on chipset's PCIE output buffers.
Z _{RX-HIGH-Z}		100			kΩ	Differential inputs must be in a high impedance state when OE# is HIGH.

TMDS Outputs

The level shifter's TMDS outputs are required to meet HDMI 1.3 specifications.

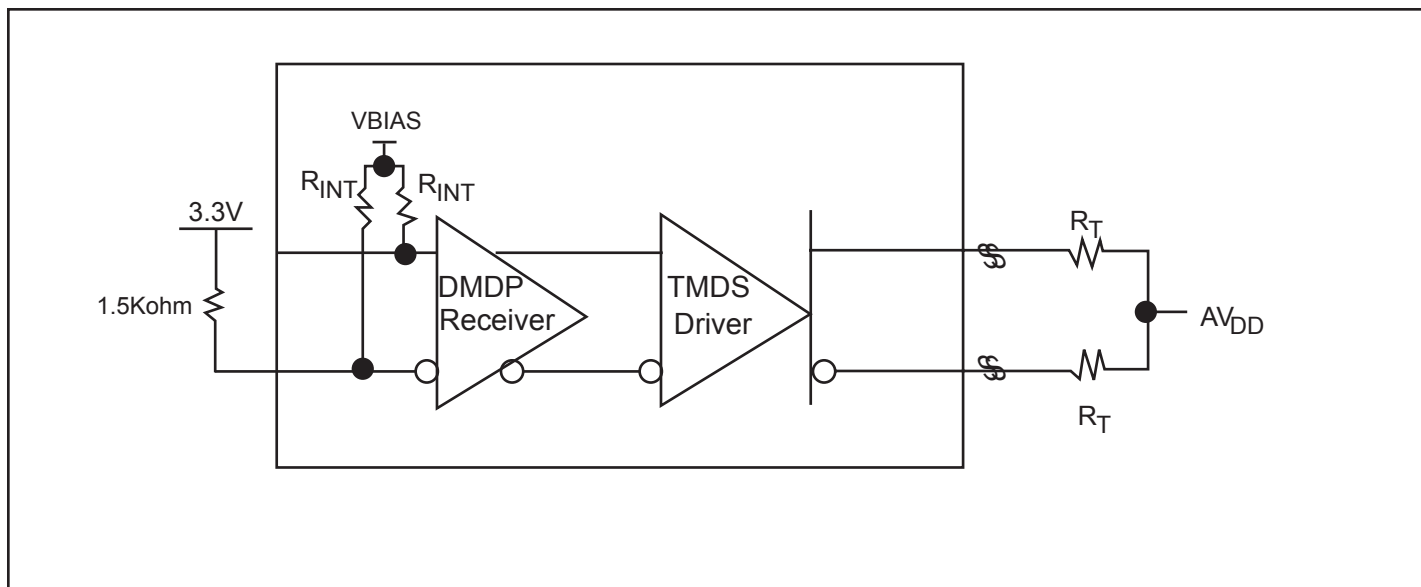
The HDMI 1.3 Specification is assumed to be the correct reference in instances where this document conflicts with the HDMI 1.3 specification.

Table 6: Differential Output Characteristics for TMDS_OUT signals

Symbol	Parameter	Min	Nom	Max	Units	Comments
V _H	Single-ended high level output voltage	VDD-10mV	VDD	VDD+10mV	V	VDD is the DC termination voltage in the HDMI or DVI Sink. VDD is nominally 3.3V
V _L	Single-ended low level output voltage	VDD-600mV	VDD-500mV	VDD-400mV	V	The open-drain output pulls down from VDD.
V _{SWING}	Single-ended output swing voltage	450mV	500mV	600mV	V	Swing down from TMDS termination voltage (3.3V ± 10%)
I _{OFF}	Single-ended current in high-Z state			50	μA	Measured with TMDS outputs pulled up to VDD Max (3.6V) through 50Ω resistors.
T _R	Rise time	125ps		0.4Tbit	ps	Max Rise/Fall time @2.7Gbps = 148ps. 125ps = 148-15%
T _F	Fall time	125ps		0.4Tbit	ps	Max Rise/Fall time @2.7Gbps = 148ps. 125ps = 148-15%
T _{SKEW-INTRA}	Intra-pair differential skew			30	ps	This differential skew budget is in addition to the skew presented between D+ and D- paired input pins. HDMI revision 1.3 source allowable intra-pair skew is 0.15Tbit.
T _{SKEW-INTER}	Inter-pair lane-to-lane output skew			100	ps	This lane-to-lane skew budget is in addition to skew between differential input pairs
T _{JIT}	Jitter added to TMDS signals			25	ps	Jitter budget for TMDS signals as they pass through the level shifter. 25ps = 0.056 Tbit at 2.25 Gb/s

TMDS output oscillation elimination

The inputs do not incorporate a squelch circuit. Therefore, we recommend the input to be externally biased to prevent output oscillation. Pericom recommends to add a 1.5Kohm pull-up to the CLK- input.



TMDS Input Fail-Safe Recommendation

Table 8: HPD Input Characteristics

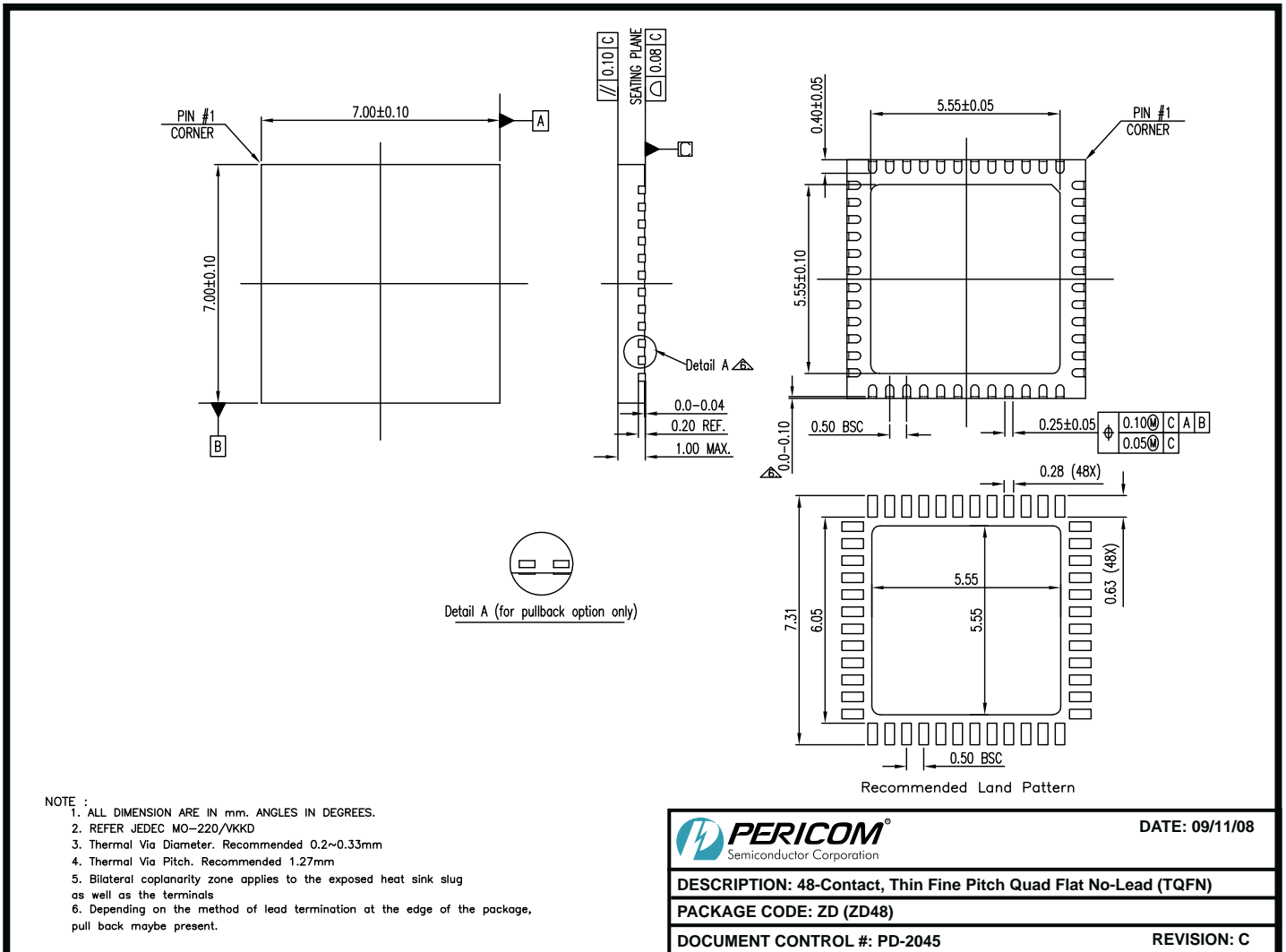
Symbol	Parameter	Min	Nom	Max	Units	Comments
V _{IH-HPD}	Input High Level	2.0	5.0	5.3	V	Low-speed input changes state on cable plug/unplug
V _{IL-HPD}	HPD_sink Input Low Level	0		0.8	V	
I _{IN-HPD}	HPD_sink Input Leakage Current			70	μA	Measured with HPD_sink at V _{IH-HPD} max and V _{IL-HPD} min
V _{OH-HPDB}	HPD_sink Output High-Level	2.5		V _{DD}	V	V _{DD} = 3.3V ± 10%
V _{OL-HPDB}	HPD_sink Output Low-Level	0		0.02	V	
T _{HDP}	HPD_sink to HPD_source propagation delay			200	ns	Time from HPD_sink changing state to HPD_source changing state. Includes HPD_source rise/fall time
T _{RF-HPDB}	HPD_source rise/fall time	1		20	ns	Time required to transition from V _{OH-HPDB} to V _{OL-HPDB} or from V _{OL-HPDB} to V _{OH-HPDB}

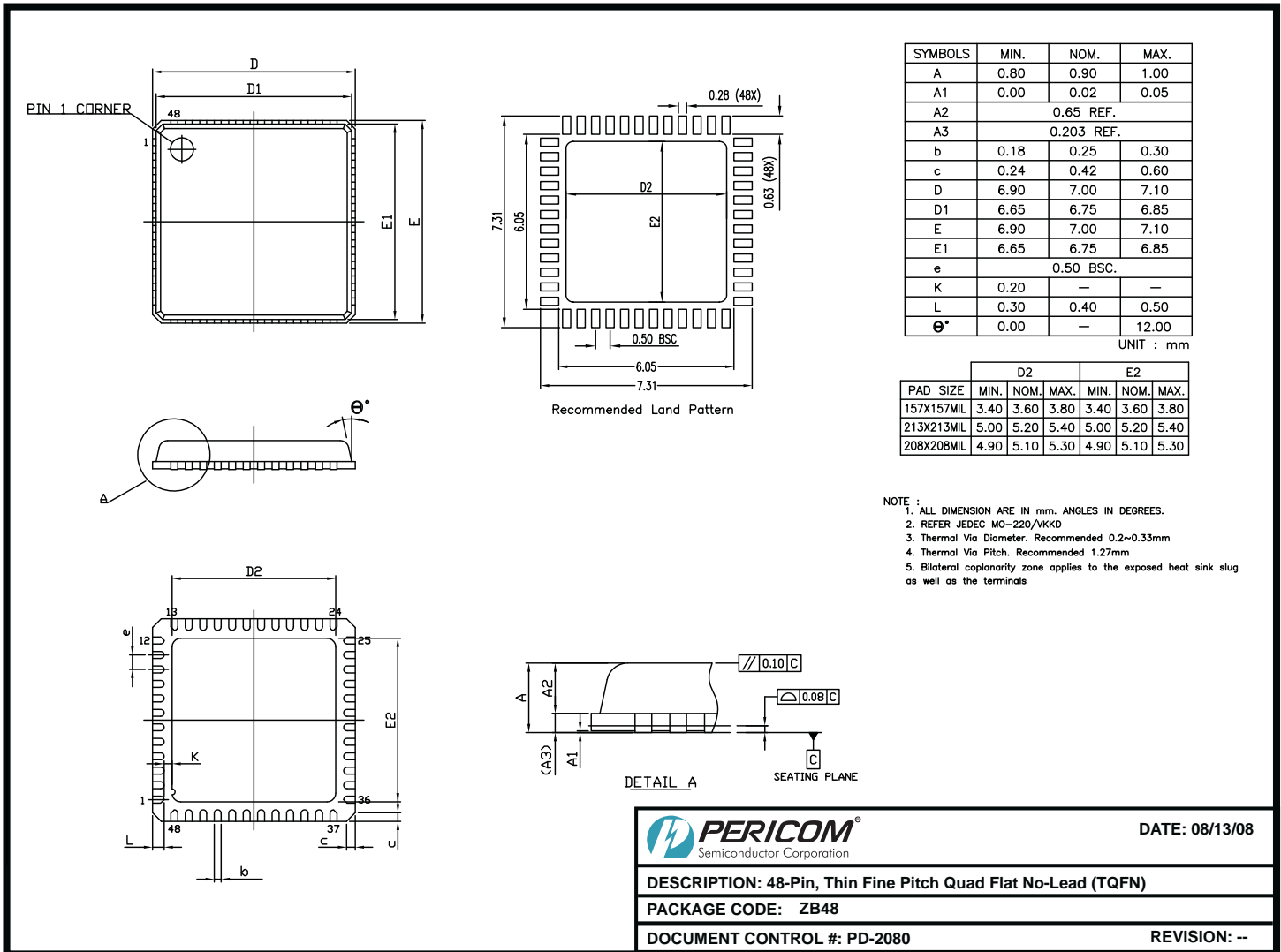
Table 9: OE# Input and DDC_EN

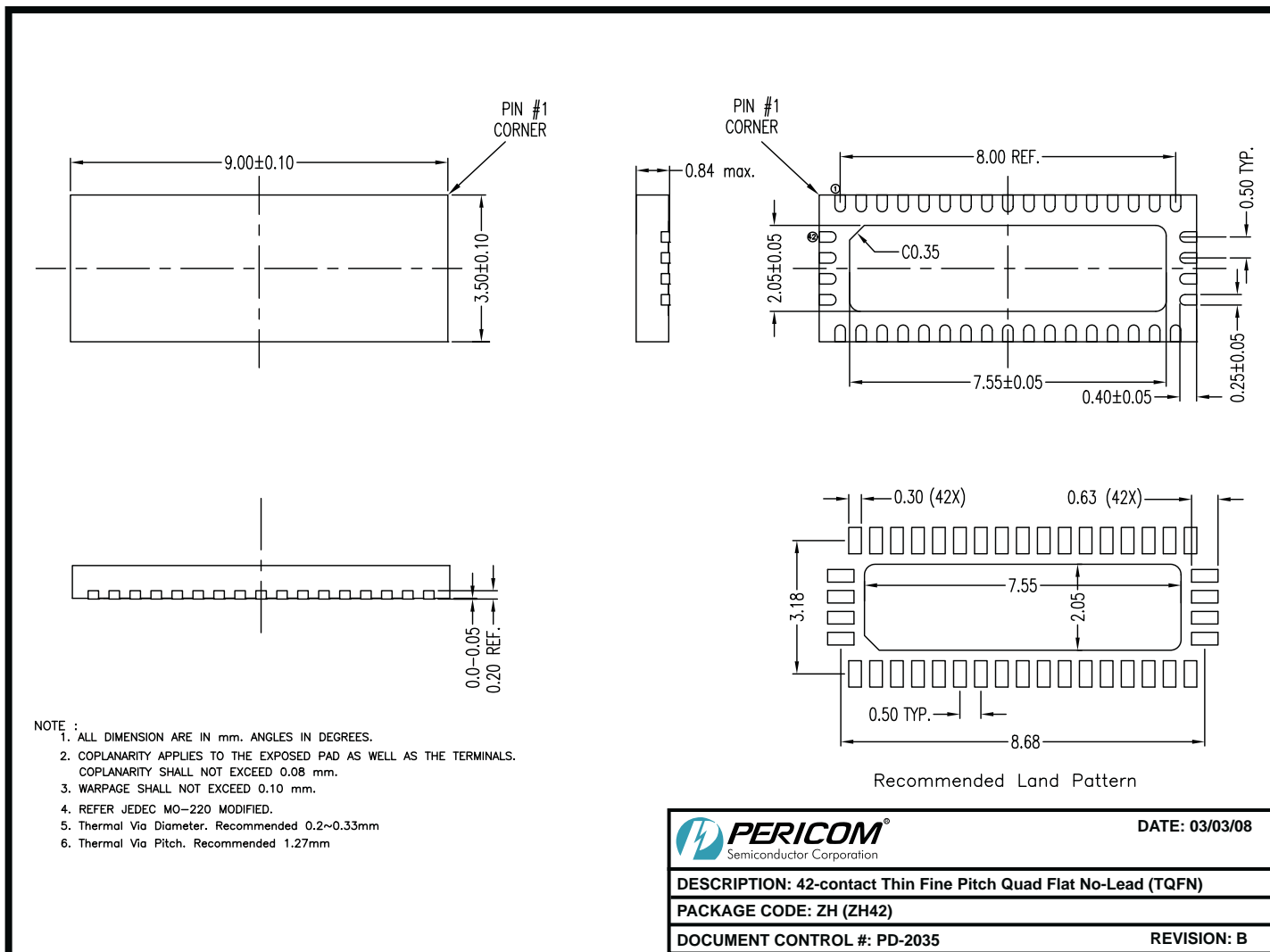
Symbol	Parameter	Min	Nom	Max	Units	Comments
V _{IH}	Input High Level	2.0		V _{DD}	V	TMDS enable input changes state on cable plug/unplug
V _{IL}	Input Low Level	0		0.8	V	
I _{IN}	Input Leakage Current			10	μA	Measured with input at V _{IH-EN} max and V _{IL-EN} min

Table 10: Termination Resistors

Symbol	Parameter	Min	Nom	Max	Units	Comments
R _{HDP}	HPD_sink input pull-down resistor.	80K	100k	120K	Ω	Guarantees HPD_sink is LOW when no display is plugged in.

Packaging Mechanical: 48-Pin, TQFN (ZD)


Packaging Mechanical: 48-Pin, TQFN (ZB)


Packaging Mechanical: 42 pin, TQFN (ZH)


08-0098

Ordering Information

Ordering Code	Package Code	Package Description
PI3VDP411LSZBE	ZBE	48-pin Pb-free & Green, TQFN
PI3VDP411LSZDE	ZDE	48-pin Pb-free & Green, TQFN
PI3VDP411LSZHE	ZHE	42--pin Pb-free & Green, TQFN

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- Adding an X Suffix = Tape/Reel