NTST30120CT, NTSJ30120CTG, NTSB30120CT-1G, NTSB30120CTG, NTSB30120CTT4G

Very Low Forward Voltage Trench-based Schottky Rectifier

Exceptionally Low V_F = 0.50 V at I_F = 5 A

Features

- Fine Lithography Trench−based Schottky Technology for Very Low Forward Voltage and Low Leakage
- Fast Switching with Exceptional Temperature Stability
- Low Power Loss and Lower Operating Temperature
- Higher Efficiency for Achieving Regulatory Compliance
- Low Thermal Resistance
- High Surge Capability
- These are Pb−Free Devices

Typical Applications

- Switching Power Supplies including Notebook / Netbook Adapters, ATX and Flat Panel Display
- High Frequency and DC−DC Converters
- Freewheeling and OR−ing diodes
- Reverse Battery Protection
- Instrumentation

Mechanical Characteristics

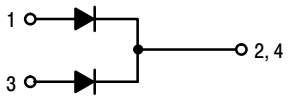
- Case: Epoxy, Molded
- Epoxy Meets Flammability Rating UL 94−0 @ 0.125 in
- Finish: All External Surfaces Corrosion Resistant and Terminal Leads are Readily Solderable
- Lead Temperature for Soldering Purposes: 260°C Maximum for 10 sec

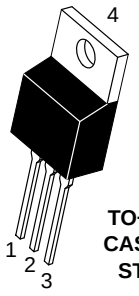
ON Semiconductor®

www.onsemi.com

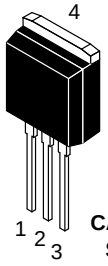
VERY LOW FORWARD VOLTAGE, LOW LEAKAGE SCHOTTKY BARRIER RECTIFIERS 30 AMPERES, 120 VOLTS

PIN CONNECTIONS

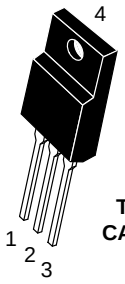




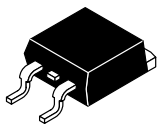
TO−220AB
CASE 221A
STYLE 6



I2PAK
CASE 418D
STYLE 3



TO−220FP
CASE 221AH



D2PAK
CASE 418B

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage		V_{RRM} V_{RWM} V_R	120	V
Average Rectified Forward Current (Rated V_R, T_C = 125°C)	Per device Per diode	$I_{F(AV)}$	 30 15	A
Peak Repetitive Forward Current (Rated V_R, Square Wave, 20 kHz, T_C = 130°C)	Per device Per diode	I_{FRM}	 60 30	A
Nonrepetitive Peak Surge Current (Surge applied at rated load conditions halfwave, single phase, 60 Hz)		I_{FSM}	150	A
Operating Junction Temperature		T_J	−40 to +150	°C
Storage Temperature		T_{stg}	−40 to +150	°C
Voltage Rate of Change (Rated V_R)		dv/dt	10,000	V/μs

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Rating	Symbol	NTST30120CTG NTSB30120CT−1G	NTSB30120CTG	NTSJ30120CTG	Unit
Maximum Thermal Resistance per Diode Junction−to−Case Junction−to−Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 2.5 70	 1.14 46.6	 4.05 105	 °C/W °C/W

ELECTRICAL CHARACTERISTICS (Per Leg unless otherwise noted)

Rating	Symbol	Typ	Max	Unit
Maximum Instantaneous Forward Voltage (Note 1)	v_F			V
(I_F = 5 A, T_J = 25°C)		0.56	−	
(I_F = 7.5 A, T_J = 25°C)		0.71	−	
(I_F = 15 A, T_J = 25°C)		0.90	1.08	
(I_F = 5 A, T_J = 125°C)		0.50	−	
(I_F = 7.5 A, T_J = 125°C)		0.60	−	
(I_F = 15 A, T_J = 125°C)		0.68	0.76	
Maximum Instantaneous Reverse Current (Note 1)	I_R			
(V_R = 90 V, T_J = 25°C)		16	−	μA
(V_R = 90 V, T_J = 125°C)		11	−	mA
(Rated dc Voltage, T_J = 25°C)		−	800	μA
(Rated dc Voltage, T_J = 125°C)		25	100	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%

TYPICAL CHARACTERISITICS

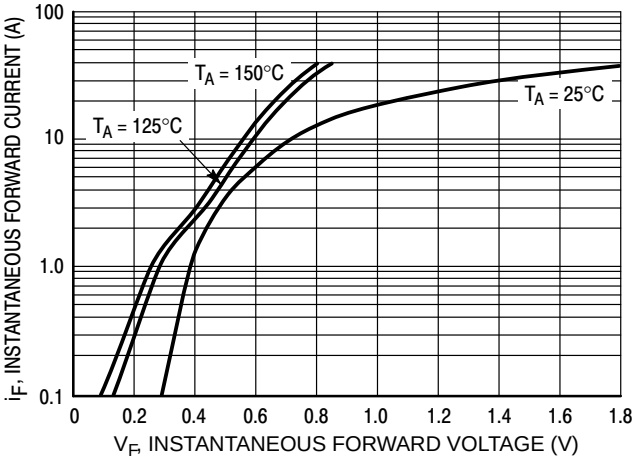


Figure 1. Typical Instantaneous Forward Characteristics

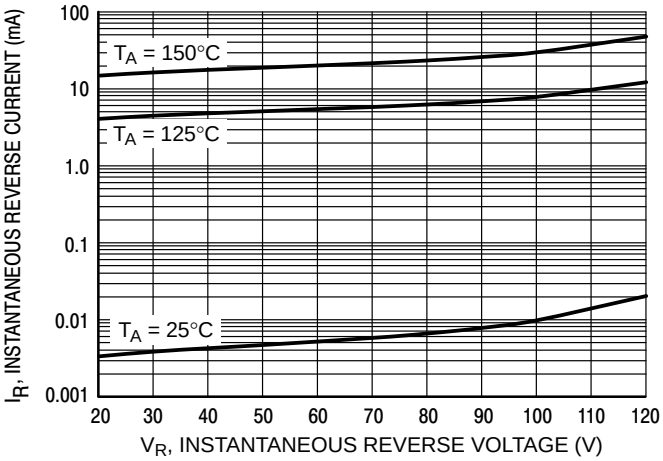


Figure 2. Typical Reverse Current Characteristics

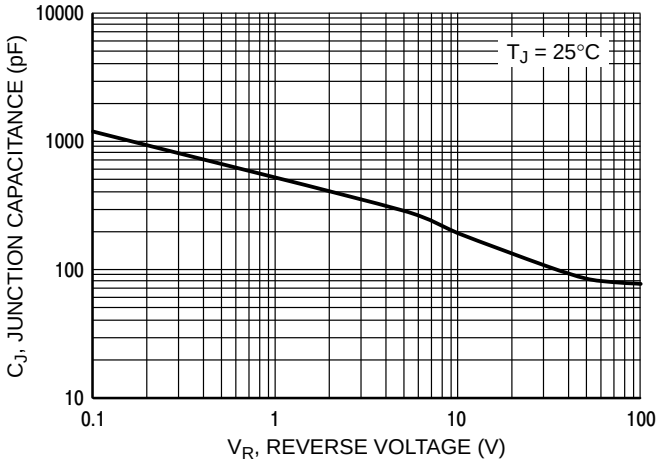


Figure 3. Typical Junction Capacitance

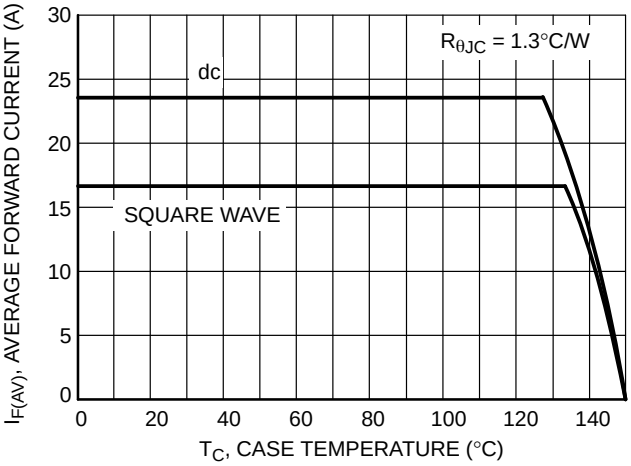


Figure 4. Current Derating per Leg

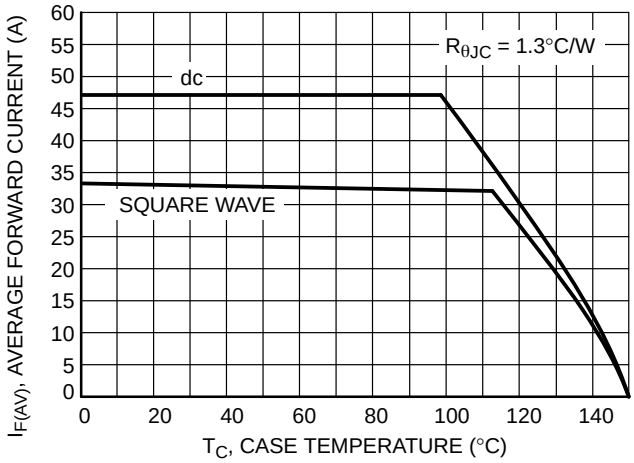


Figure 5. Current Derating

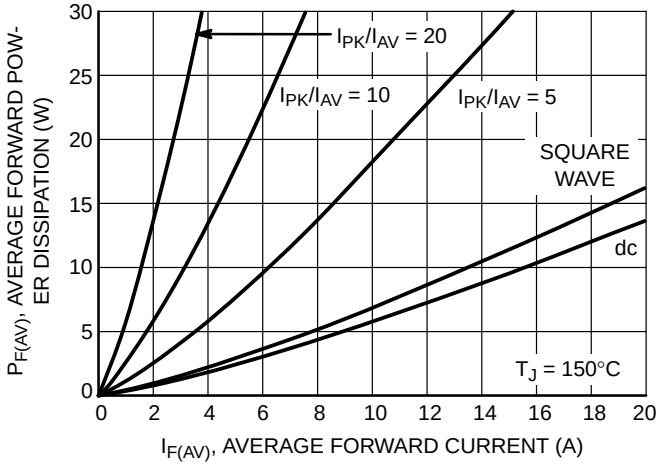


Figure 6. Forward Power Dissipation

TYPICAL CHARACTERISITICS

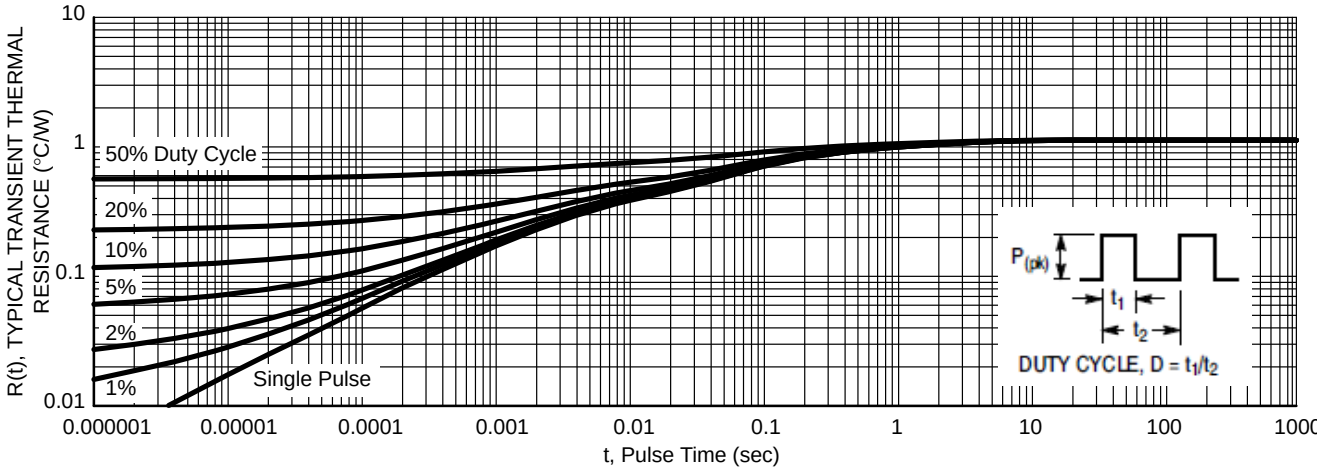


Figure 7. Typical Transient Thermal Response for NTST30120CT and NTSB30120CT−1G

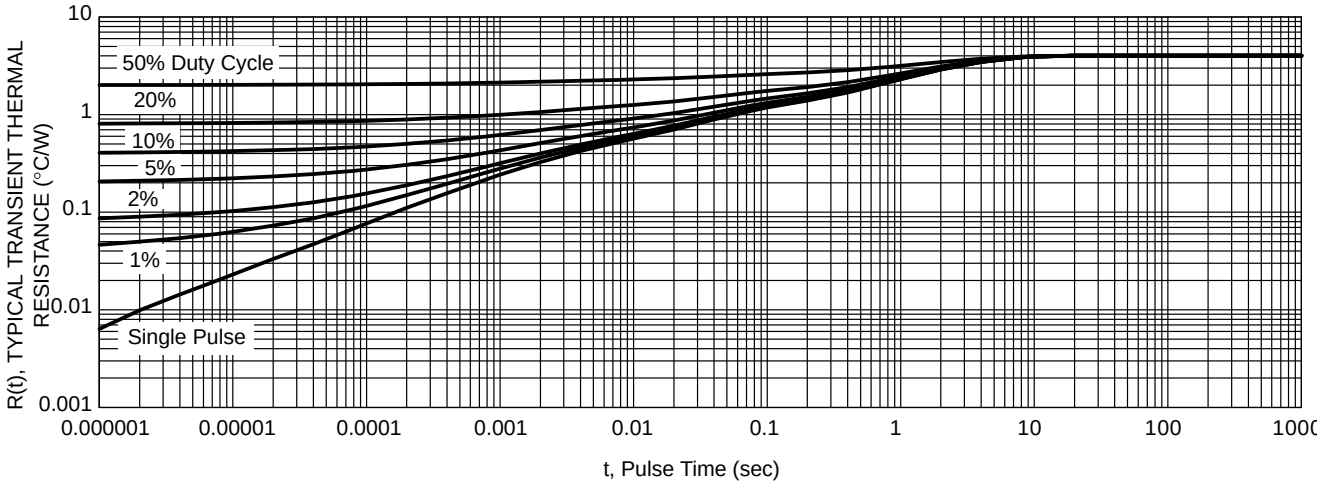


Figure 8. Typical Transient Thermal Response for NTSJ30120CTG

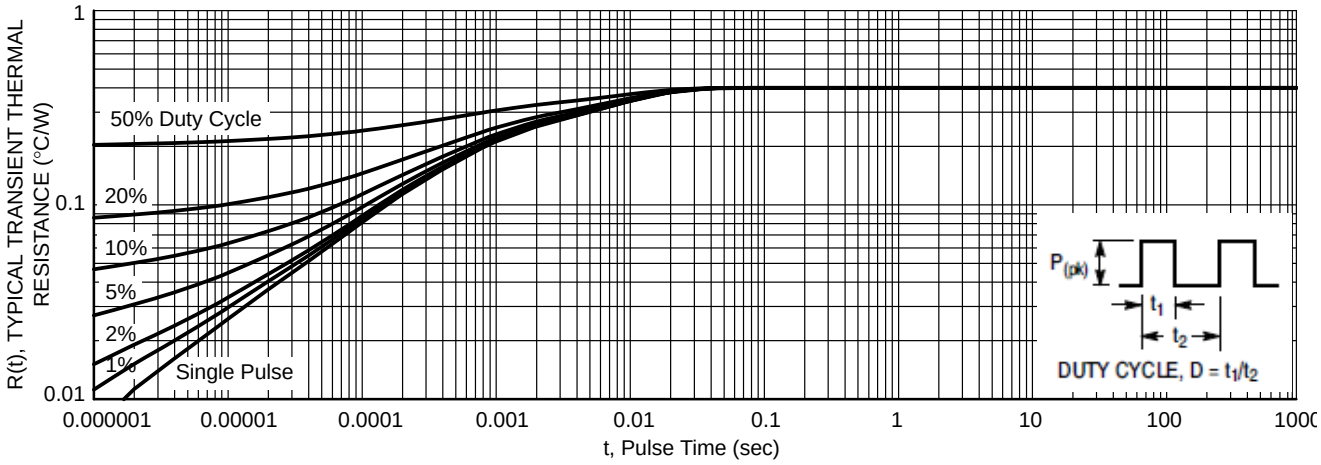


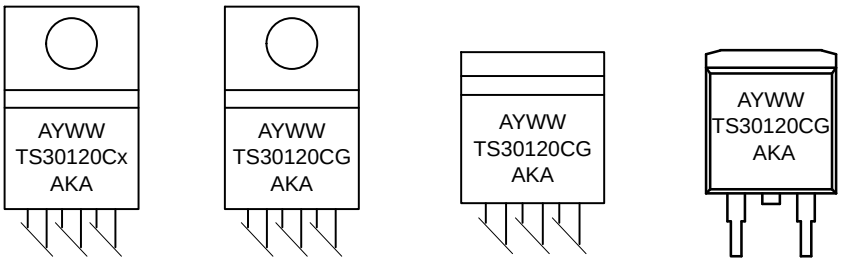
Figure 9. Typical Transient Thermal Response for NTSB30120CTG

ORDERING INFORMATION

Device	Package	Shipping†
NTST30120CTG	TO−220AB (Pb−Free)	50 Units / Rail
NTSJ30120CTG	TO−220FP (Halide−Free)	50 Units / Rail
NTSB30120CT−1G	I^2PAK (Pb−Free)	50 Units / Rail
NTSB30120CTG	D^2PAK (Pb−Free)	50 Units / Rail
NTSB30120CTT4G	D^2PAK (Pb−Free)	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MARKING DIAGRAMS



TO−220AB TO−220FP I^2PAK D^2PAK

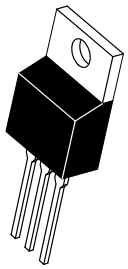
A = Assembly Location
Y = Year
WW = Work Week
AKA = Polarity Designator
x = G or H
G = Pb−Free Package
H = Halide−Free Package

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

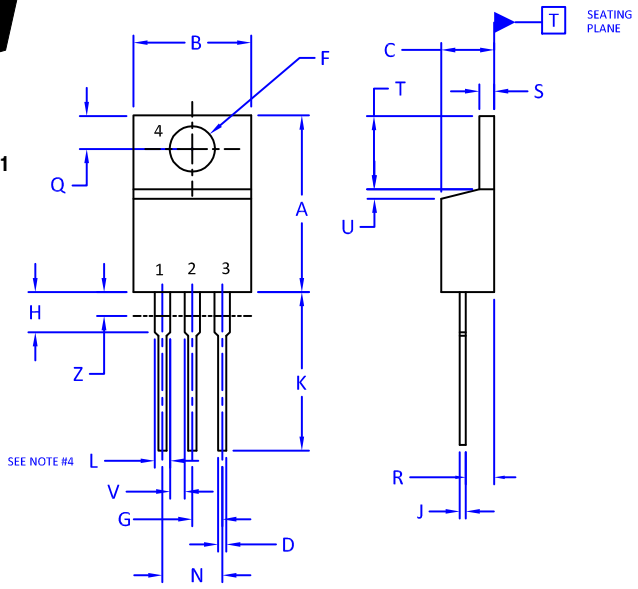
ON Semiconductor®

TO−220
CASE 221A−09
ISSUE AJ

DATE 05 NOV 2019



SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

	INCHES		MILLIMETERS	
DIM	MIN.	MAX.	MIN.	MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	----	1.15	---
Z	----	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

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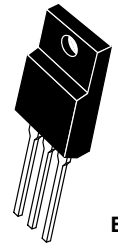
DESCRIPTION:	TO−220	PAGE 1 OF 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

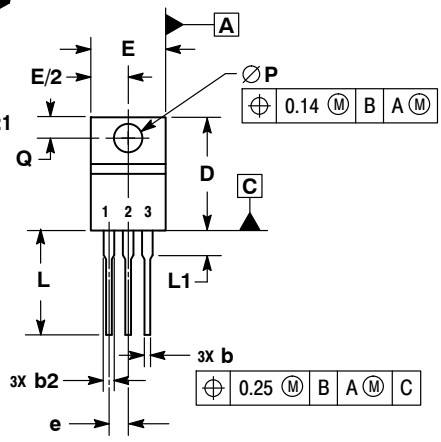
ON Semiconductor®

TO−220 FULLPACK, 3−LEAD
CASE 221AH
ISSUE F

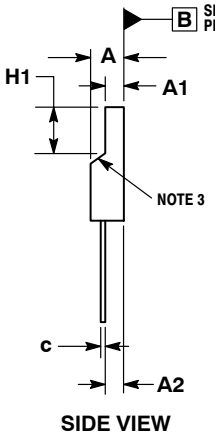
DATE 30 SEP 2014



SCALE 1:1



FRONT VIEW

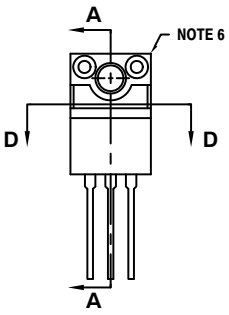


SIDE VIEW

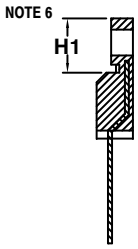
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. CONTOUR UNCONTROLLED IN THIS AREA.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH AND GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.13 PER SIDE. THESE DIMENSIONS ARE TO BE MEASURED AT OUTERMOST EXTREME OF THE PLASTIC BODY.
5. DIMENSION b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 2.00.
6. CONTOURS AND FEATURES OF THE MOLDED PACKAGE BODY MAY VARY WITHIN THE ENVELOP DEFINED BY DIMENSIONS A1 AND H1 FOR MANUFACTURING PURPOSES.

	MILLIMETERS	
DIM	MIN	MAX
A	4.30	4.70
A1	2.50	2.90
A2	2.50	2.90
b	0.54	0.84
b2	1.10	1.40
c	0.49	0.79
D	14.70	15.30
E	9.70	10.30
e	2.54 BSC	
H1	6.60	7.10
L	12.50	14.73
L1	---	2.80
P	3.00	3.40
Q	2.80	3.20

SECTION D−D

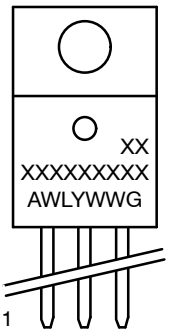


ALTERNATE CONSTRUCTION



SECTION A−A

GENERIC MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLE 1:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. GATE

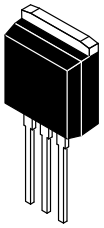
DOCUMENT NUMBER:	**98AON52577E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**TO−220 FULLPACK, 3−LEAD**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

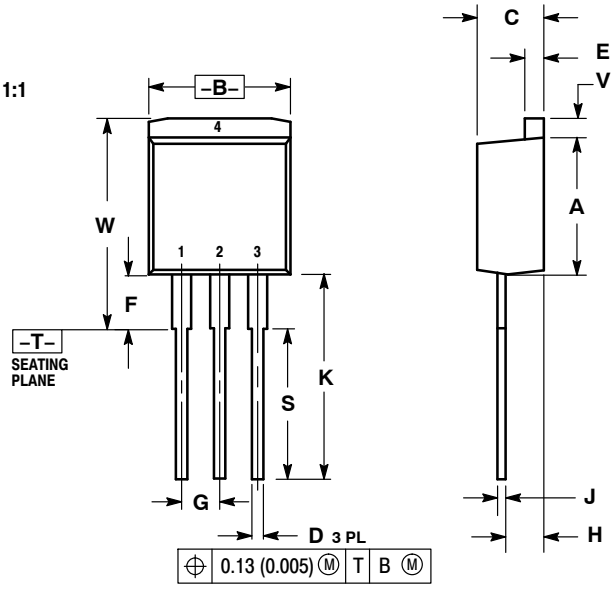
ON Semiconductor®

I²PAK (TO−262)
CASE 418D−01
ISSUE D

DATE 16 OCT 2007



SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.335	0.380	8.51	9.65
B	0.380	0.406	9.65	10.31
C	0.160	0.185	4.06	4.70
D	0.026	0.035	0.66	0.89
E	0.045	0.055	1.14	1.40
F	0.122 REF		3.10 REF	
G	0.100 BSC		2.54 BSC	
H	0.094	0.110	2.39	2.79
J	0.013	0.025	0.33	0.64
K	0.500	0.562	12.70	14.27
S	0.390 REF		9.90 REF	
V	0.045	0.070	1.14	1.78
W	0.522	0.551	13.25	14.00

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

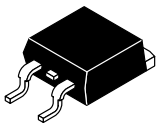
STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DOCUMENT NUMBER:	**98ASB16716C**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**I²PAK (TO−262)**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

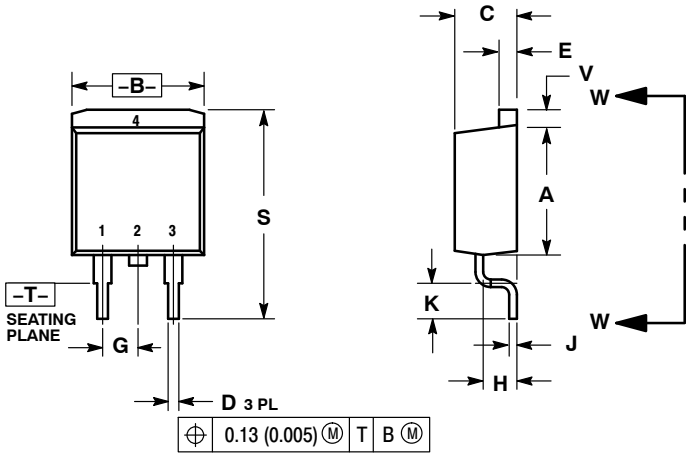
ON Semiconductor®



D²PAK 3
CASE 418B–04
ISSUE L

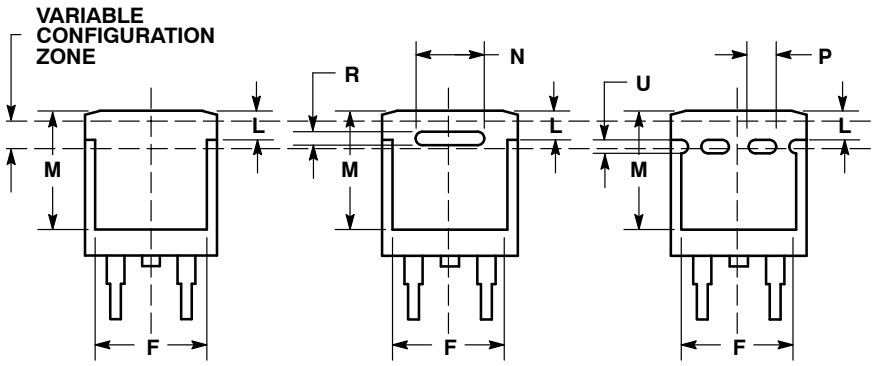
DATE 17 FEB 2015

SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B–01 THRU 418B–03 OBSOLETE, NEW STANDARD 418B–04.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197 REF		5.00 REF	
P	0.079 REF		2.00 REF	
R	0.039 REF		0.99 REF	
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40



VIEW W–W 1 | VIEW W–W 2 | VIEW W–W 3

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. NO CONNECT
2. CATHODE
3. ANODE
4. CATHODE

MARKING INFORMATION AND FOOTPRINT ON PAGE 2

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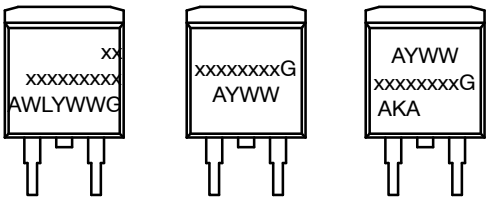
DESCRIPTION:	**D²PAK 3**		**PAGE 1 OF 2**

D²PAK 3
CASE 418B−04
ISSUE L

DATE 17 FEB 2015

GENERIC
MARKING DIAGRAM*

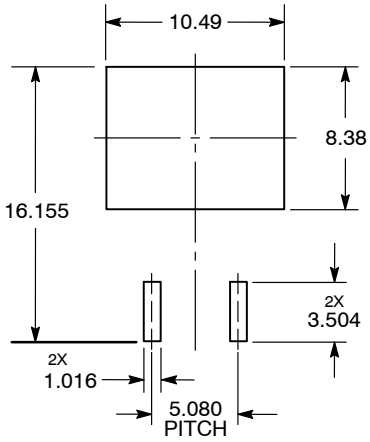


IC **Standard** **Rectifier**

xx	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package
AKA	= Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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