

Orderable parts

Table 1. Orderable part variations ⁽¹⁾

| Part number | Temperature (T _A) | Package |
|--------------------------------|-------------------------------|------------------------|
| MPC17531ATEP | -20 °C to 65 °C | 24 QFN |
| MPC17531ATEV/EL ⁽²⁾ | | 20 VMFP |
| MPC17531ATEJ | | 20 TSSOP (exposed pad) |

Notes

- 1. To order parts in Tape & Reel, add the R2 suffix to the part number.
- 2. Not recommended for new designs.

Internal block diagram

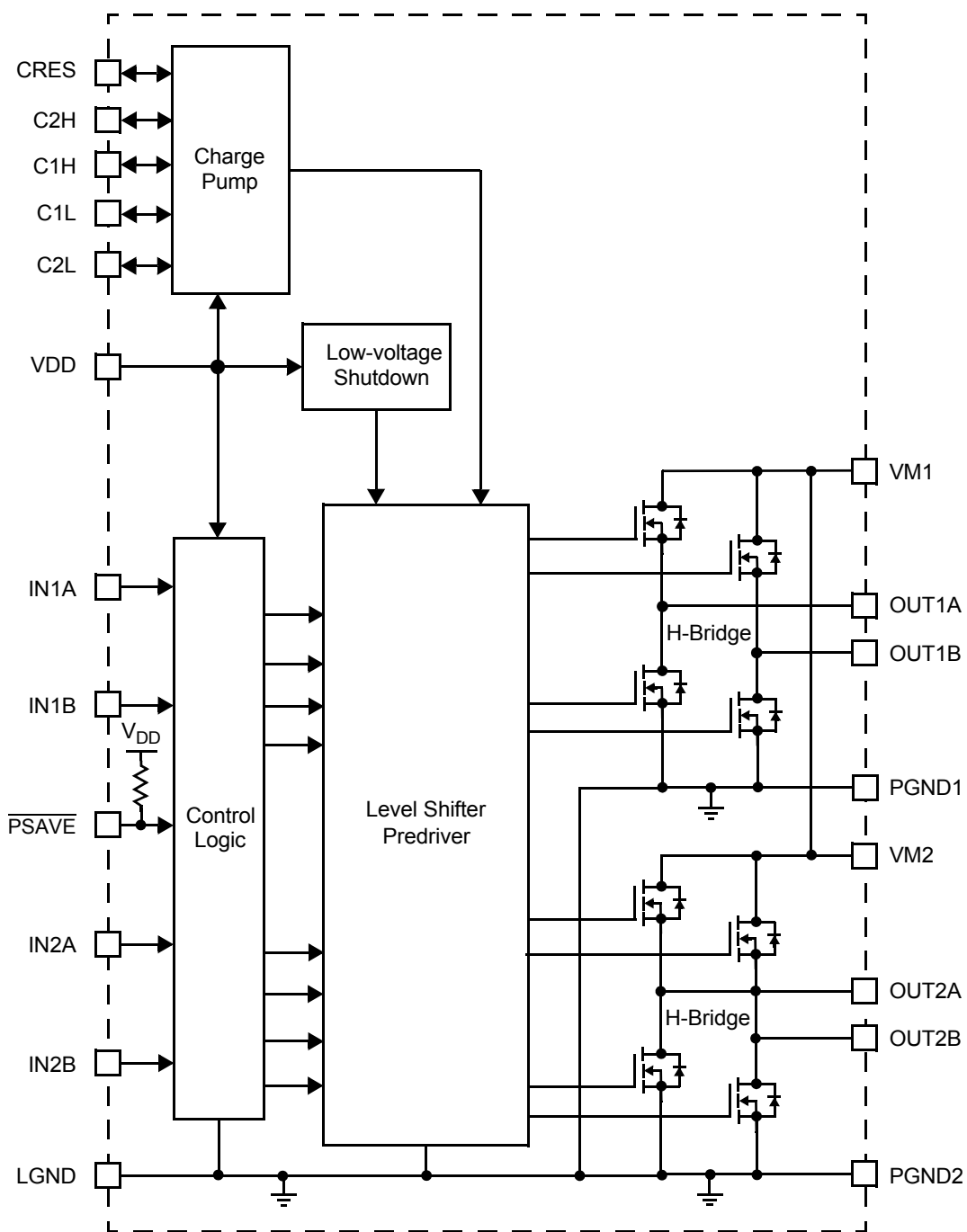


Figure 2. 17531A Simplified internal block diagram

Pin connections

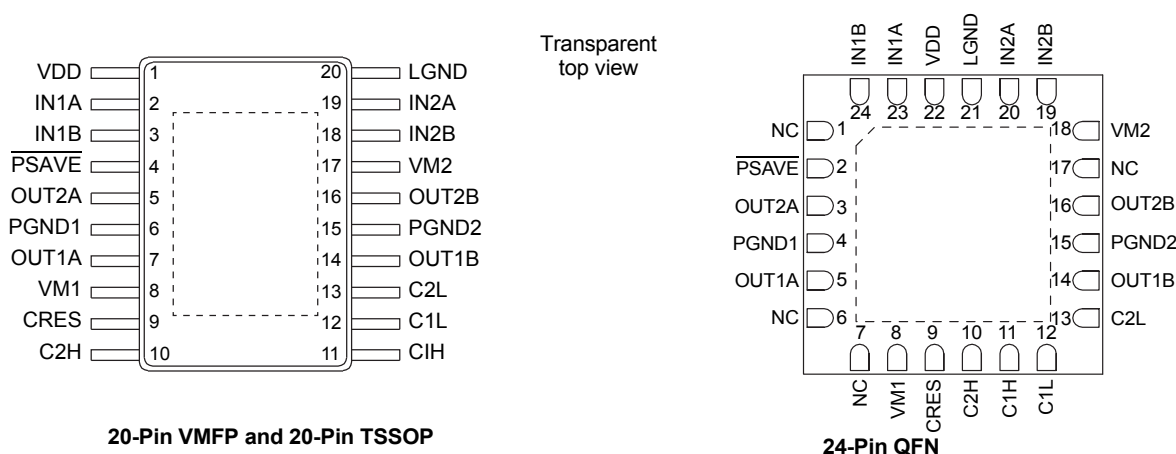


Figure 3. Pin connections

A functional description of each pin can be found in the Functional Pin Description section beginning on [page 9](#).

Table 2. 17531A, pin definitions

| Pin number 20-Pin VMFP, 20-Pin TSSOP | Pin number 24-Pin QFN | Pin name | Formal name | Definition |
|--|--------------------------|----------|----------------------------|--|
| 1 | 22 | VDD | Logic Supply | Control circuit power supply pin. |
| 2 | 23 | IN1A | Logic Input Control 1A | Logic input control of OUT1A (refer to Table 6, Truth table , page 8). |
| 3 | 24 | IN1B | Logic Input Control 1B | Logic input control of OUT1B (refer to Table 6, Truth table , page 8). |
| 4 | 2 | PSAVE | Power Save | Logic input controlling power save mode. |
| 5 | 3 | OUT2A | H-Bridge Output 2A | Output A of H-Bridge channel 2. |
| 6 | 4 | PGND1 | Power Ground 1 | High-current power ground 1. |
| 7 | 5 | OUT1A | H-Bridge Output 1A | Output A of H-Bridge channel 1. |
| 8 | 8 | VM1 | Motor Drive Power Supply 1 | Positive power source connection for H-Bridge 1 (Motor Drive Power Supply). |
| 9 | 9 | CRES | Predriver Power Supply | Internal triple charge pump output as predriver power supply. |
| 10 | 10 | C2H | Charge Pump 2H | Charge pump bucket capacitor 2 (positive pole). |
| 11 | 11 | C1H | Charge Pump 1H | Charge pump bucket capacitor 1 (positive pole). |
| 12 | 12 | C1L | Charge Pump 1L | Charge pump bucket capacitor 1 (negative pole). |
| 13 | 13 | C2L | Charge Pump 2L | Charge pump bucket capacitor 2 (negative pole). |
| 14 | 14 | OUT1B | H-Bridge Output 1B | Output B of H-Bridge channel 1. |
| 15 | 15 | PGND2 | Power Ground 2 | High-current power ground 2. |
| 16 | 16 | OUT2B | H-Bridge Output 2B | Output B of H-Bridge channel 2. |
| 17 | 17 | VM2 | Motor Drive Power Supply 2 | Positive power source connection for H-Bridge 2 (Motor Drive Power Supply). |
| 18 | 19 | IN2B | Logic Input Control 2B | Logic input control of OUT2B (refer to Table 6, Truth table , page 8). |
| 19 | 20 | IN2A | Logic Input Control 2A | Logic input control of OUT2A (refer to Table 6, Truth table , page 8). |
| 20 | 21 | LGND | Logic Ground | Low-current logic signal ground. |
| N/A | 1, 6, 7, 17 | NC | — | No Connect |
| - | N/A | - | - | Exposed pad on 20-Pin TSSOP |

Electrical characteristics

Maximum ratings

Table 3. Maximum ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

| Symbol | Ratings | Value | Unit | Notes |
|--------------------------|--|-------------------------|------|----------|
| V_M | Motor Supply Voltage | -0.5 to 11.0 | V | |
| V_{CRES} | Charge Pump Output Voltage | -0.5 to 14.0 | V | |
| V_{DD} | Logic Supply Voltage | -0.5 to 5.0 | V | |
| V_{IN} | Signal Input Voltage | -0.5 to $V_{DD} + 0.5$ | V | |
| I_O I_{OPK} | Driver Output Current • Continuous • Peak | 0.7 1.4 | A | (3) |
| V_{ESD1} V_{ESD2} | ESD Voltage • Human Body Model • Machine Model | ± 1200 ± 150 | V | (4) |
| T_J | Operating Junction Temperature | -20 to 150 | °C | |
| T_A | Operating Ambient Temperature | -20 to 65 | °C | |
| T_{STG} | Storage Temperature Range | -65 to 150 | °C | |
| $R_{\theta JA}$ | Thermal Resistance | 50 | °C/W | (5) |
| P_D | Power Dissipation • WMFP • QFN | 1.0 2.5 | W | (6) |
| T_{SOLDER} | Pin Soldering Temperature | 260 | °C | (7) |
| T_{PPRT} | Peak Package Reflow Temperature During Reflow | Note 8 | °C | (7), (8) |

Notes

- $T_A = 25^\circ\text{C}$, 10 ms pulse width at 200 ms intervals.
- ESD1 testing is performed in accordance with the Human Body Model ($C_{ZAP} = 100\text{ pF}$, $R_{ZAP} = 1500\ \Omega$), ESD2 testing is performed in accordance with the Machine Model ($C_{ZAP} = 200\text{ pF}$, $R_{ZAP} = 0\ \Omega$).
- QFN24: 45 x 30 x 1 [mm] glass EPOXY board mount. (See: recommended heat pattern) VMFP16: 37 x 50 x 1.6 [mm] glass EPOXY board mount. When the exposed pad is bonded, Rsj is not performed.
- Maximum at $T_A = 25^\circ\text{C}$. When the exposed pad is bonded, Rsj is not performed.
- Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
- NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.NXP.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxx enter 33xxx), and review parametrics.

Static electrical characteristics

Table 4. Static electrical characteristics

Characteristics noted under conditions $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 3.0\text{ V}$, $V_M = 5.0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min. | Typ. | Max. | Unit | Notes |
|--------------------------------|--|--------|--------|------------|------------------------------|--------------|
| Power input | | | | | | |
| V_{M-CP} | Motor Supply Voltage (Using Internal Charge Pump) | 2.0 | 5.0 | 8.6 | V | (9) |
| V_{M-NCP} | Motor Supply Voltage (V_{CRES} Applied Externally) | – | – | 10 | V | (10) |
| $V_{CRES-VM}$ | Gate Drive Voltage - Motor Supply Voltage (V_{CRES} Applied Externally) | 5.0 | 6.0 | – | V | (11) |
| V_{DD} | Logic Supply Voltage | 2.7 | 3.0 | 3.6 | V | |
| I_{QM} $I_{QM-PSAVE}$ | Driver Quiescent Supply Current • No Signal Input • Power Save Mode | – – | – – | 100 1.0 | μA | |
| I_{QVDD} $I_{QVDD-PSAVE}$ | Logic Quiescent Supply Current • No Signal Input • Power Save Mode | – – | – – | 1.0 1.0 | mA μA | (12) |
| I_{VDD} I_{CRES} | Operating Power Supply Current • Logic Supply Current • Charge Pump Circuit Supply Current | – – | – – | 3.0 0.7 | mA | (13) (14) |
| V_{DDEDET} | Low V_{DD} Detection Voltage | 1.0 | 1.6 | 2.5 | V | (15) |
| $R_{DS(ON)}$ | Driver Output ON Resistance | – | 0.8 | 1.2 | Ω | (16) |

Gate drive

| | | | | | | |
|----------------|--|------|-----|------|---------------|------|
| V_{CRES} | Gate Drive Voltage • No Current Load | 12 | 13 | 13.5 | V | (14) |
| $V_{CRESLOAD}$ | Gate Drive Ability (Internally Supplied) • $I_{CRES} = -1.0\text{ mA}$ | 8.5 | 9.2 | – | V | |
| C_{CP} | Recommended External Capacitance ($C1L-C1H$, $C2L-C2H$, $C_{RES}-GND$) | 0.01 | 0.1 | 1.0 | μF | |

Control logic

| | | | | | | |
|--|--|--|------------------------|---|---|--|
| V_{IN} | Logic Input Voltage | 0 | – | V_{DD} | V | |
| V_{IH} V_{IL} I_{IH} I_{IL} $I_{IL-PSAVE}$ | Logic Inputs ($2.7\text{ V} < V_{DD} < 3.3\text{ V}$) • High Level Input Voltage • Low Level Input Voltage • High Level Input Current • Low Level Input Current • PSAVE Pin Input Current Low | $V_{DD} \times 0.7$ – – –1.0 – | – – – – 50 | – $V_{DD} \times 0.3$ 1.0 – 100 | V V μA μA μA | |

Notes

9. Gate drive voltage V_{CRES} is generated internally. $2 \times V_{DD} + V_M$ must be $< V_{CRES\text{ MAX}}$ (13.5 V).
10. No internal charge pump used. V_{CRES} is applied from an external source.
11. $R_{DS(ON)}$ is not guaranteed if $V_{CRES-VM} < 5.0\text{ V}$. Also, function is not guaranteed if $V_{CRES-VM} < 3.0\text{ V}$.
12. I_{QVDD} includes the current to pre-driver circuit.
13. I_{VDD} includes the current to predriver circuit at $f_{IN} = 100\text{ kHz}$.
14. At $f_{IN} = 20\text{ kHz}$.
15. Detection voltage is defined as when the output becomes high-impedance after V_{DD} drops below the detection threshold. V_{CRES} is applied from an external source. $2 \times V_{DD} + V_M$ must be $< V_{CRES\text{ MAX}}$ (13.5 V).
16. $I_O = 0.7\text{ A}$ source + sink.

Dynamic electrical characteristics

Table 5. Dynamic electrical characteristics

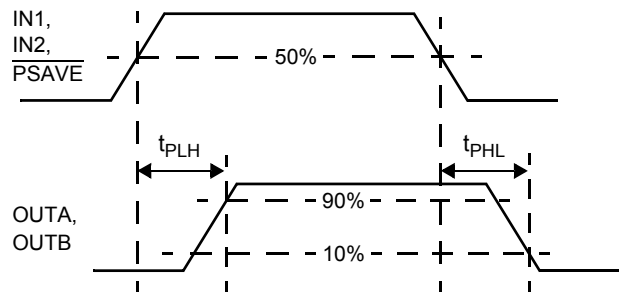
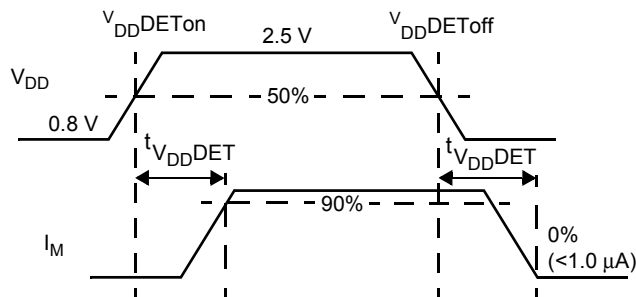
Characteristics noted under conditions $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 3.0\text{ V}$, $V_M = 5.0\text{ V}$, $\text{GND} = 0\text{ V}$, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min. | Typ. | Max. | Unit | Notes |
|------------------------|---|--------|------------|---------------------|---------------|-----------------|
| Input | | | | | | |
| f_{IN} | Pulse Input Frequency | – | – | 200 | kHz | |
| t_R | Input Pulse Rise Time | – | – | 1.0 ⁽¹⁸⁾ | μs | ⁽¹⁷⁾ |
| t_F | Input Pulse Fall Time | – | – | 1.0 ⁽¹⁸⁾ | μs | ⁽¹⁹⁾ |
| Output | | | | | | |
| t_{PLH} t_{PHL} | Propagation Delay Time • Turn-ON Time • Turn-OFF Time | – – | 0.1 0.1 | 0.5 0.5 | μs | ⁽²⁰⁾ |
| t_{VGON} | Charge Pump Wake-up Time | – | 1.0 | 3.0 | ms | ⁽²¹⁾ |
| t_{VDDDET} | Low Voltage Detection Time | – | – | 10 | ms | |

Notes

17. Time is defined between 10% and 90%.
18. That is, the input waveform slope must be steeper than this.
19. Time is defined between 90% and 10%.
20. Output load is $8.0\text{ }\Omega$ DC.
21. $C_{CP} = 0.1\text{ }\mu\text{F}$.

Timing diagrams

**Figure 4. t_{PLH} , t_{PHL} , and t_{PZH} timing****Figure 5. Low voltage detection timing**

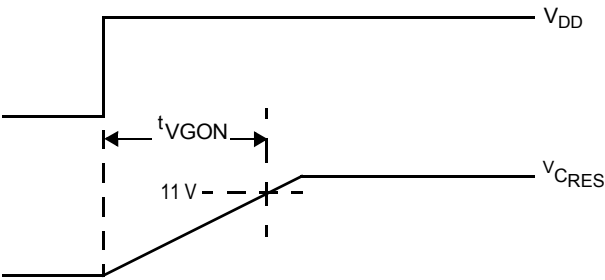


Figure 6. Charge pump timing

Table 6. Truth table

| INPUT | | | OUTPUT | | Charge pump and low voltage detector |
|---------------------------|--------------|--------------|----------------|----------------|--------------------------------------|
| $\overline{\text{PSAVE}}$ | IN1A IN2A | IN1B IN2B | OUT1A OUT2A | OUT1B OUT2B | |
| L | L | L | L | L | RUN |
| L | H | L | H | L | RUN |
| L | L | H | L | H | RUN |
| L | H | H | Z | Z | RUN |
| H | X | X | Z | Z | STOP |

H = High.
L = Low.
Z = High-impedance.
X = Don't care.
PSAVE pin is pulled up to V_{DD} with internal resistance.

Functional description

Introduction

The 17531A is a monolithic dual H-Bridge ideal for portable electronic applications to control bipolar step motors and brush DC motors, such as those found in camera lens assemblies, camera shutters, and optical disk drives. The device features an on-board charge pump, as well as built-in shoot-through current protection and under-voltage shutdown.

The 17531A has four operating modes: Forward, Reverse, Brake, and Tri-state (high-impedance). The MOSFETs comprising the output bridge have a total source + sink $R_{DS(ON)} \leq 1.2 \, \Omega$. The 17531A can simultaneously drive two brush DC motors or one bipolar step motor. The drivers are designed to be PWMed at frequencies up to 200 kHz.

Functional pin description

Logic supply (VDD)

The VDD pin carries the logic supply voltage and current into the logic sections of the IC. VDD has an undervoltage threshold. If the supply voltage drops below the undervoltage threshold, the output power stage switches to a tri-state condition. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input pins.

Logic input control (IN1A, IN1B, IN2A, and IN2B)

These logic input pins control each H-Bridge output. IN1A logic HIGH = OUT1A HIGH. However, if all inputs are taken HIGH, the outputs bridges are both tri-stated (refer to [Table 6, Truth table](#), page 8).

Power save ($\overline{\text{PSAVE}}$)

The $\overline{\text{PSAVE}}$ pin is a HIGH = TRUE power save mode input. When $\overline{\text{PSAVE}} = \text{HIGH}$, all H-Bridge outputs (OUT1A, OUT1B, OUT2A, and OUT2B) are tri-stated (High-Z), regardless of logic inputs (IN1A, IN1B, IN2A, and IN2B) states, and the internal charge pump and low voltage detection current are shut off to save power.

H-Bridge output (OUT1A, OUT1B, OUT2A, and OUT2B)

These pins provide connection to the outputs of each of the internal H-Bridges (see [Figure 2, 17531A Simplified internal block diagram](#), page 3).

Motor drive power supply (VM1 and VM2)

The VM pins carry the main supply voltage and current into the power sections of the IC. This supply then becomes controlled and/or modulated by the IC as it delivers the power to the loads attached between the OUTput pins. All VM pins must be connected together on the printed circuit board.

Charge pump (C1L and C1H, C2L and C2H)

These two pairs of pins, the C1L and C1H, and the C2L and C2H, connect to the external bucket capacitors required by the internal charge pump. The typical value for the bucket capacitors is 0.1 μF .

Predriver power supply (CRES)

The CRES pin is the output of the internal charge pump. Its output voltage is approximately three times of V_{DD} voltage. The V_{CRES} voltage is power supply for the internal predriver circuit of H-Bridges.

Power ground (PGND)

Power ground pins. They must be tied together on the PCB.

Logic ground (LGND)

Logic ground pin.

Typical applications

Figure 7 shows a typical application for the 17531A. When applying the gate voltage to the CRES pin from an external source, be sure to connect it via a resistor equal to or greater than $R_G = V_{CRES}/0.02 \Omega$.

The internal charge pump of this device is generated from the V_{DD} supply; therefore, care must be taken to provide sufficient gate-source voltage for the high side MOSFETs when $V_M \gg V_{DD}$ (e.g., $V_M = 5.0 \text{ V}$, $V_{DD} = 3.3 \text{ V}$), in order to ensure full enhancement of the high side MOSFET channels.

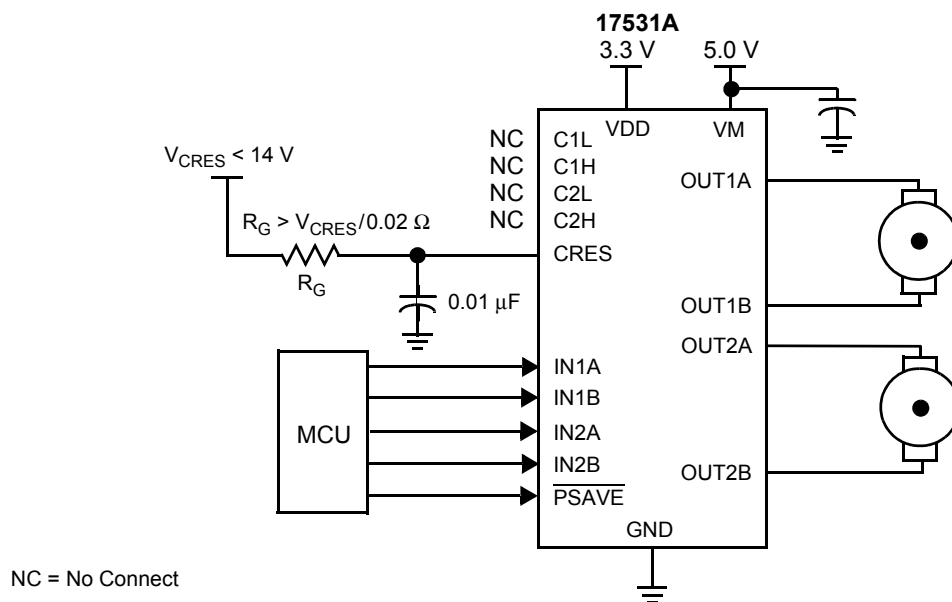


Figure 7. 17531A typical application diagram

CEMF snubbing techniques

Care must be taken to protect the IC from potentially damaging CEMF spikes induced when commutating currents in inductive loads. Typical practice is to provide snubbing of voltage transients via placing a capacitor or zener at the supply pin (VM) (see Figure 8).

PCB layout

When designing the printed circuit board (PCB), connect sufficient capacitance between power supply and ground pins to ensure proper filtering from transients. For all high current paths, use wide copper traces and the shortest possible distances.

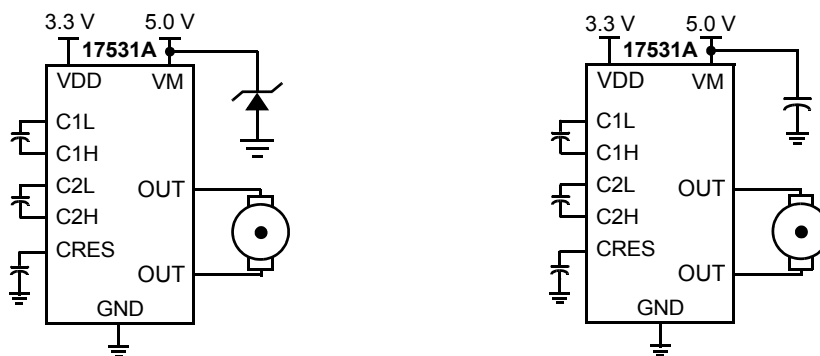
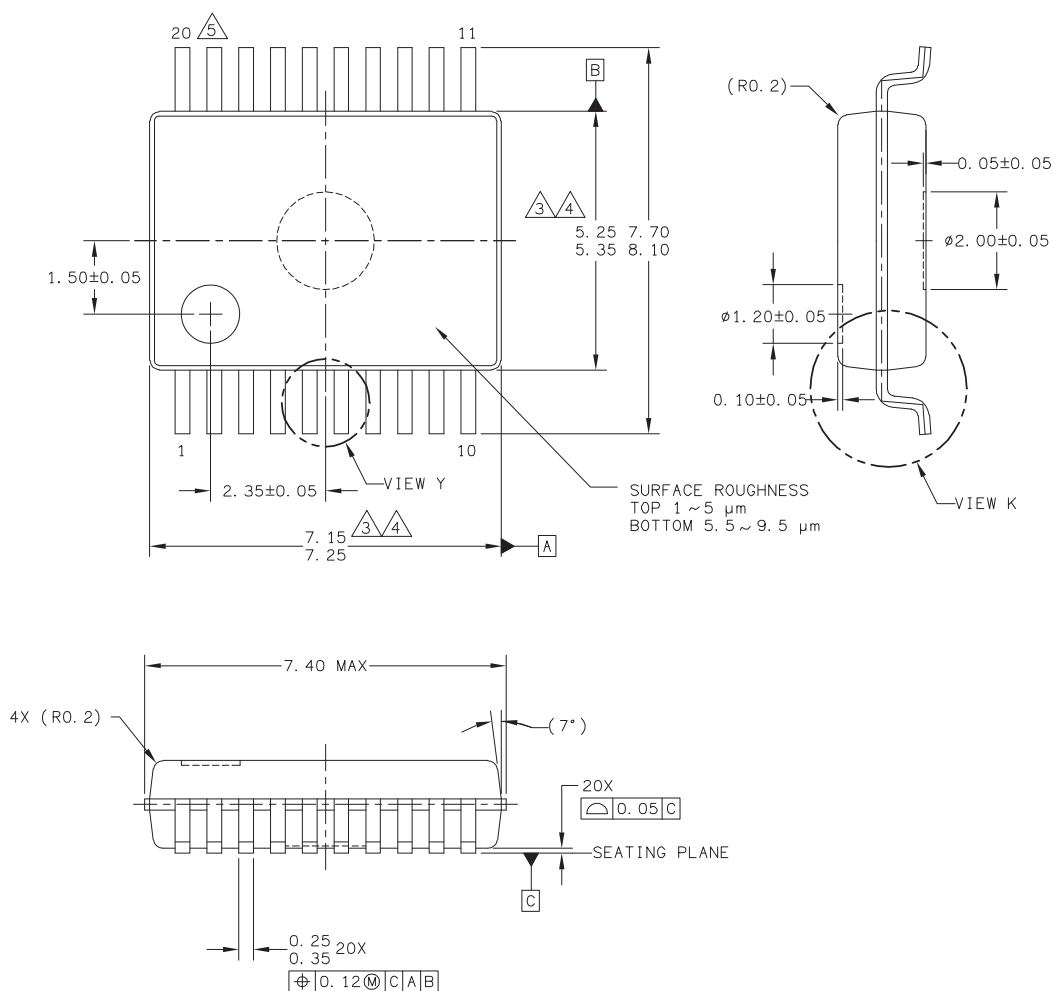


Figure 8. CEMF snubbing techniques

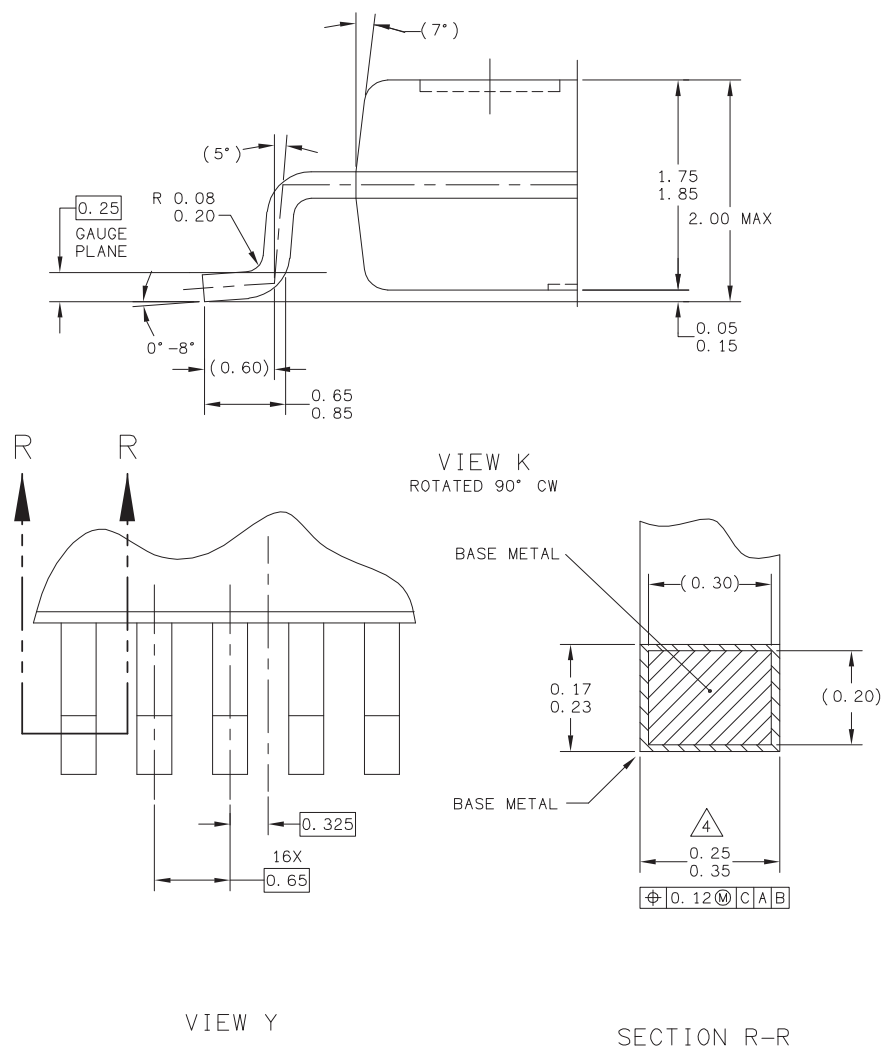
Packaging

Package dimensions

For the most current package revision, visit www.NXP.com and perform a keyword search using the “98A” drawing number listed.



| | | |
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NOTES:

1 DIMENSIONING AND TOLERANCING PER ASME Y14.5M – 1994.

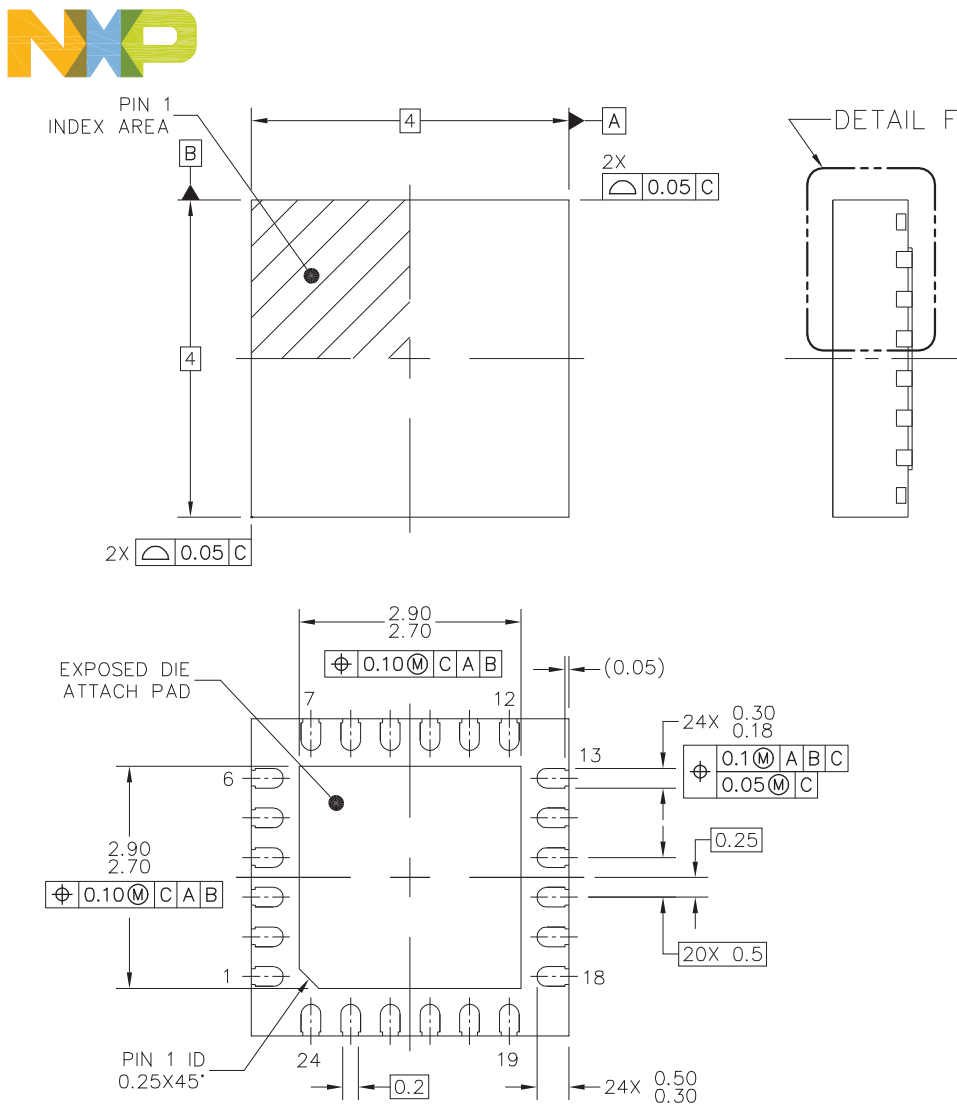
2 ALL DIMENSIONS ARE IN MILLIMETERS.

3 DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.10 ANY SIDE.
DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 PER SIDE.

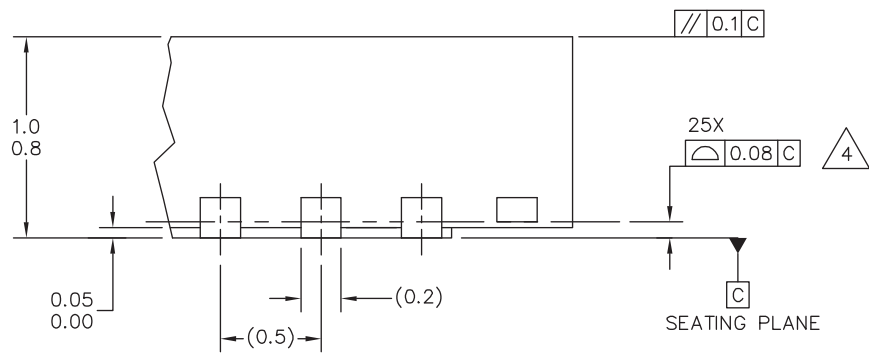
4 DIMENSIONS ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY
EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS, AND INTERLEAD FLASH,
BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

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DETAIL F
VIEW ROTATED 90°CW

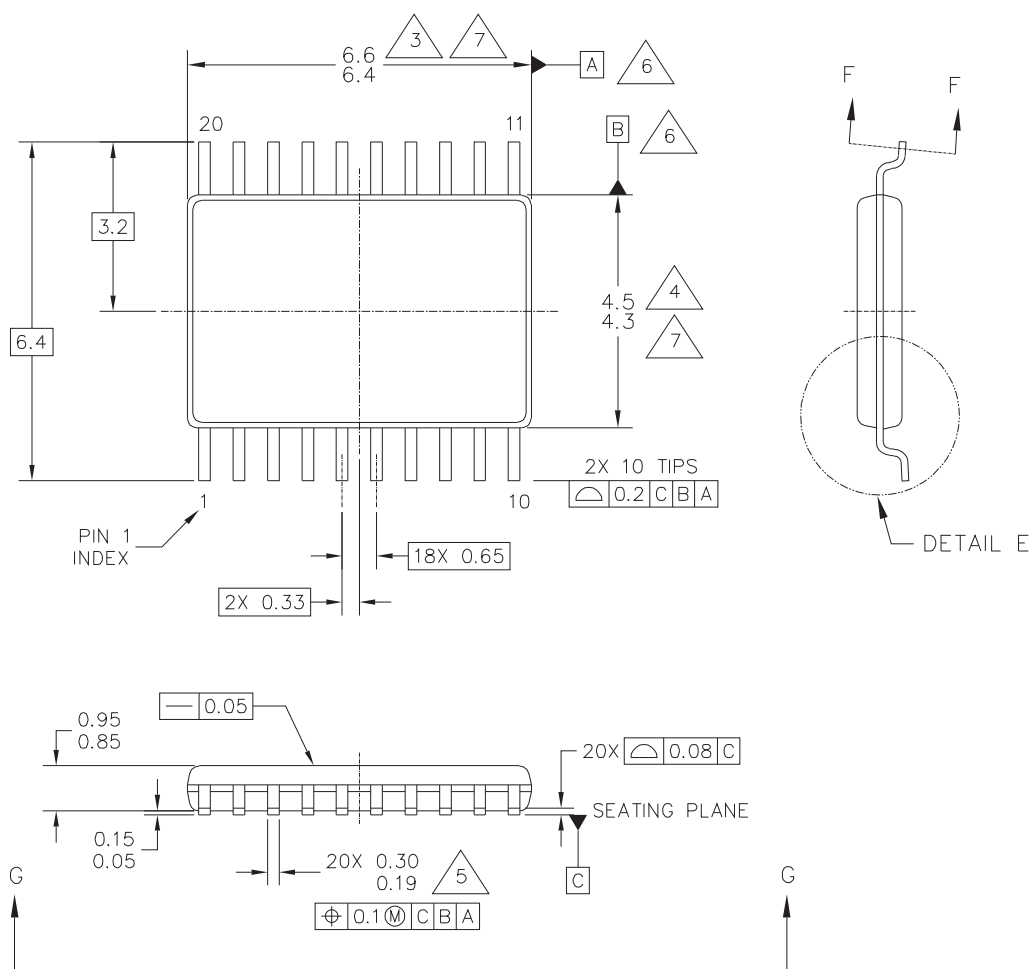
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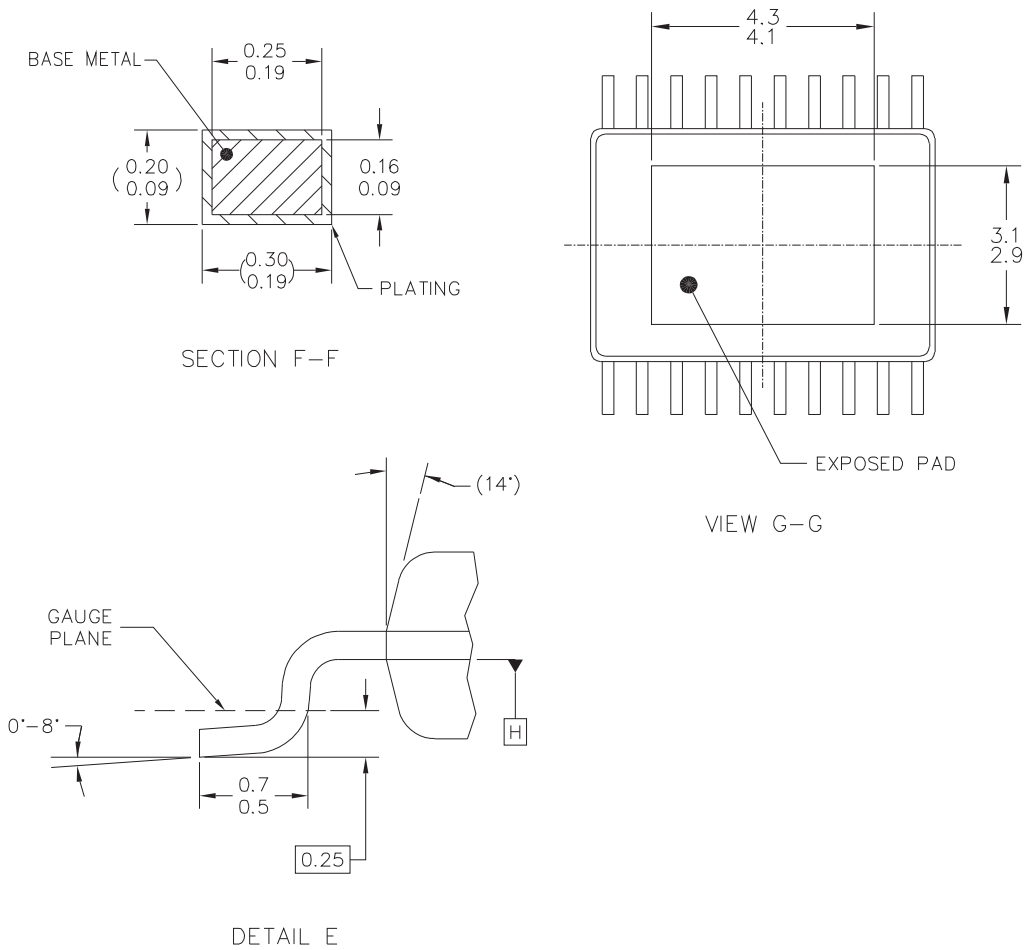
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- 4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.
- 5. MIN. METAL GAP SHOULD BE 0.2 MM.

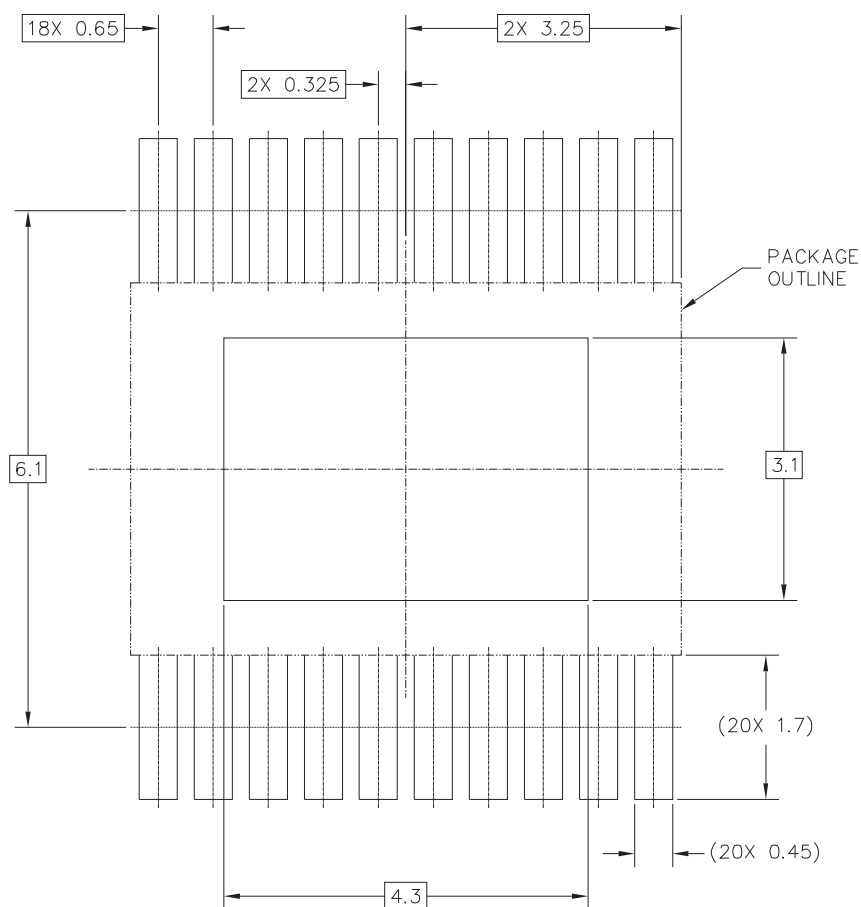
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2. DIMENSIONS ARE IN MILLIMETERS.

3. DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.15 PER SIDE.

4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR MOLD PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.

5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 MM.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.

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Revision history

| Revision | Date | Description of changes |
|----------|---------|--|
| 2.0 | 9/2005 | <ul style="list-style-type: none"> Implemented Revision History page Converted to Freescale format |
| 3.0 | 2/2008 | <ul style="list-style-type: none"> Corrected Table 2, Pin Definitions on page 4 |
| 4.0 | 5/2009 | <ul style="list-style-type: none"> Corrected Note 7, in Static Electrical Characteristics table |
| 5.0 | 10/2013 | <ul style="list-style-type: none"> Updated package drawings Corrected ordering information table to MPC17531ATEP and MPC17531ATEV/EL Added new back page and document properties |
| 6.0 | 10/2013 | <ul style="list-style-type: none"> Corrected packaging information on page 1 |
| 7.0 | 11/2014 | <ul style="list-style-type: none"> Changed the QFN 98A to 98ASA00474D per PCN 16331 Corrected errors in ordering information |
| 8.0 | 3/2015 | <ul style="list-style-type: none"> Corrected unit typo for Logic Quiescent Supply Current |
| 9.0 | 7/2015 | <ul style="list-style-type: none"> Added 98ASA00887D package information and updated tables where applicable Added MPC17531ATEJ to the ordering information Updated as per PCN # 16724 |
| | 8/2015 | <ul style="list-style-type: none"> Corrected the 98A package information for 20-pin TSSOP |
| 10.0 | 10/2015 | <ul style="list-style-type: none"> Added EP notation for TSSOP package. Fixed notations for TSSOP in Orderable parts and Pin connections. Updated Packaging 98A drawing for TSSOP |
| | 7/2016 | <ul style="list-style-type: none"> Updated to NXP document form and style |

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