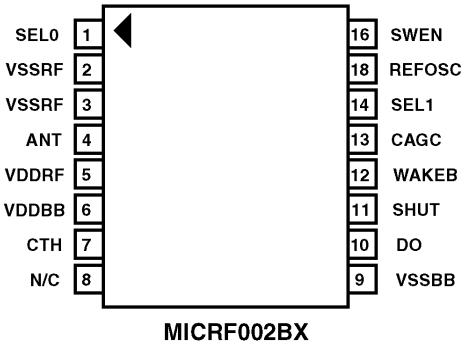
Ordering Information

Part Number	Temperature Range	Package
MICRF002BN	-40°C to +85°C	16-Pin DIP
MICRF002BM	-40°C to +85°C	16-Pin SOIC
MICRF022BN	-40°C to +85°C	8-Pin DIP
MICRF022BM	-40°C to +85°C	8-Pin SOIC

The standard 16-pin package provides the user with complete control of MICRF002 mode and filter selection. An 8-pin standard part is also available for very low cost applications. The 8-pin version comes pre-programmed in SWP mode, with Demodulator Filter bandwidth set to 5000Hz, and SHUT pin externally available. Other 8-pin configurations are available. Contact the factory for details.

Pin Configuration (DIP and SOIC)



MICRF002BX

MICRF0022BX

Pin Description (Pin numbers for the 8-pin version are identified in parentheses)

Pin Number	Pin Name	Pin Function
1	SEL0	This pin, in conjunction with SEL1, programs the desired Demodulator Filter Bandwidth. This pin is internally pulled-up to VDD. See Table 1.
2/3	VSSRF	This pin is the ground return for the RF section of the IC. The bypass capacitor connected from VDDRF to VSSRF should have the shortest possible lead length. For best performance, connect VSSRF to VSSBB at the power supply only (i.e., keep VSSBB currents from flowing through VSSRF return path).
(1)	VSS	This pin is the ground return for the IC. The bypass capacitor connected from VDD to VSS should have the shortest possible lead length.
4 (2)	ANT	This is the receive RF input, internally ac-coupled. Connect this pin to the receive antenna. Input impedance is high (FET gate) with approximately 2pF of shunt (parasitic) capacitance. For applications located in high ambient noise environments, a fixed value band-pass network may be connected between the ANT pin and VSSRF to provide additional receive selectivity and input overload protection. (See *"Application Note TBD"*.)
5	VDDRF	This pin is the positive supply input for the RF section of the IC. VDDBB and VDDRF should be connected directly at the IC pins. Connect a low ESL, low ESR decoupling capacitor from this pin to VSSRF, as short as possible.
6	VDDBB	This pin is the positive supply input for the baseband section of the IC. VDDBB and VDDRF should be connected directly at the IC pins.
(3)	VDD	This pin is the positive supply input for the IC. Connect a low ESL, low ESR decoupling capacitor from this pin to VSSRF, as short as possible.
7 (4)	CTH	This capacitor extracts the (DC) average value from the demodulated waveform, which becomes the reference for the internal data slicing comparator. Treat this as a low-pass RC filter with source impedance of 118kΩ (for REFOSC frequency ft = 4.90MHz, see Note 5). A standard ± 20% X7R ceramic capacitor is generally sufficient.
8	N/C	Unused Pin
9	VSSBB	This is the ground return for the baseband section of the IC. The bypass and output capacitors connected to VSSBB should have the shortest possible lead lengths. For best performance, connect VSSRF to VSSBB at the power supply only (i.e., keep VSSBB currents from flowing through VSSRF return path).
10 (5)	DO	The output data signal. CMOS level compatible.
11 (6)	SHUT	A logic input for Shutdown Mode control. Pull this pin low to place the IC into operation. This pin in internally pulled-up to VDD.
12	WAKEB	An output signal, active low when the IC detects an incoming RF signal, determined by monitoring for data preamble. CMOS level compatible.
13 (7)	CAGC	Integrating capacitor for on-chip AGC (Automatic Gain Control). The Decay/Attack time-constant (TC) ratio is nominally set as 10:1. Use of 0.47uF or greater is strongly recommended for best range performance. Use low-leakage type capacitors for duty-cycle operation (Dip Tantalum, Ceramic, Polyester). (See *"Application Note* TBD.)
14	SEL1	This pin, in conjunction with SEL0, programs the desired Demodulator Filter Bandwidth. This pin in internally pulled-up to VDD. See Table 1.
15 (8)	REFOSC	This is the timing reference for on-chip tuning and alignment. Connect either a ceramic resonator or crystal (mode dependent) between this pin and VSSBB, or drive the input with an AC coupled 0.5Vpp input clock. Use ceramic resonators without integral capacitors. Note that if operating in FIXED mode, a crystal must be used; however in SWP mode, one may use either a crystal or ceramic resonator. See *"Application Note TBD"* for details on frequency selection and accuracy.
16	SWEN	This logic pin controls the operating mode of the MICRF002. When SWEN = HIGH, the MICRF002 is in SWP mode. When SWEN = LOW, the device operates as a conventional single-conversion superheterodyne receiver. (See *"Application Note TBD"* for details.) This pin is internally pulled-up to VDD.

SEL0	SEL1	Demodulator Bandwidth (Hz)	
		SWP Mode	FIXED Mode
1	1	5000	10000
0	1	2500	5000
1	0	1250	2500
0	0	625	1250

Table 1
Nominal Demodulator (Baseband) Filter Bandwidth
vs. SEL0, SEL1 and Mode

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VDDRF, VDDBB).....+7V
Voltage on any I/O Pin.....VSS-0.3 to VDD+0.3
Junction Temperature.....+150°C
Storage Temperature Range.....-65°C to + 150°C
Lead Temperature (soldering, 10 seconds).....+ 260°C

Operating Ratings

Supply Voltage (VDDRF, VDDBB).....4.75V to 5.5V
Ambient Operating Temperature (T_A).....-40°C to +85°C
Package Thermal Resistance θ_{JA} (16 Pin DIP).....90°C/W
Package Thermal Resistance θ_{JA} (16 Pin SOIC)....120°C/W

This device is ESD sensitive: Meets Class 1ESD test requirements (Human body Model, HBM), in accordance with MIL-STD-883C, Method 3015. Do not operate or store near strong electrostatic fields. Use appropriate ESD precautions.

Electrical Characteristics

Unless otherwise stated, these specifications apply for Ta = -40°C to 85°C, 4.75<VDD<5.5V. All voltages are with respect to Ground; Positive currents flow into device pins. CAGC = 4.7µF, CTH = .047µF, VDDRF= VDDBB = VDD. REFOSC frequency = 4.90MHz.

Parameter	Test Conditions	MIN	TYP	MAX	UNITS
Power Supply					
Operating Current	Continuous Operation		2.4		mA
Operating Current	10:1 Duty Cycle		240		µA
Standby Current	SHUT = VDD		0.5		µA
RF/IF Section					
Receiver Sensitivity	Note 1, 3		-103		dBm
IF Center Frequency	Note 4		0.86		MHz
IF 3dB Bandwidth	Note 3, 4		0.43		MHz
RF Input Range		300		440	MHz
Receive Modulation Duty-Cycle		20		80	%
Maximum Receiver Input	Rsc = 50Ω		-20		dBm
Spurious Reverse Isolation	ANT pin, Rsc = 50Ω Note 2		30		µVrms
AGC Attack / Decay ratio	T(Attack) / T(Decay)		0.1		
AGC Leakage Current	Ta = 85°C		±100		nA
Local Oscillator Stabilization Time	To 1% of Final Value		2.5		msec
Demod Section					
CTH Source Impedance	Note 5		118k		Ω
CTH Source Impedance Variation		-15		+15	%
CTH Leakage Current	Ta = 85°C		±100		nA
Demod Filter Bandwidth	SEL0 = SEL1 = SWEN = VDD, Note 4, 6		4160		Hz
Demod Filter Bandwidth	SEL0 = SEL1 = VDD, SWEN = VSS Note 4, 6		8320		Hz
Digital/Control Section					
REFOSC Input Impedance			200k		Ω
Input Pull up Current	SEL0, SEL1, SWEN, SHUT=VSS		8		µA
Input High Voltage	SEL0, SEL1, SWEN			0.8VDD	V
Input Low Voltage	SEL0, SEL1, SWEN	0.2VDD			V
Output Current	DO, WAKEUP pins, Push-Pull		10		µA
Output High Voltage	DO, WAKEUP pins, Iout = -1µA	0.9VDD			V
Output Low Voltage	DO. WAKEUP pins, Iout = +1µA			0.1VDD	V
Output Tr, Tf	DO, WAKEUP pins, Cload=15pF			10	µsec

Note 1: Sensitivity is defined as the average signal level measured at the input necessary to achieve 10e-2 Bit Error Rate (BER). The input signal is defined as a return-to-zero (RZ) waveform with 50% average duty cycle (e.g., Manchester Encoded Data) at a data rate of 300bps. The RF input is assumed to be matched into 50Ω.

Note 2: Spurious reverse isolation represents the spurious components which appear on the RF input (ANT) pin measured into 50Ω with an input RF matching network.

Note 3: Sensitivity, a commonly specified Receiver parameter, provides an indication of the Receiver's input referred noise, generally input thermal noise. However, it is possible for a more sensitive receiver to exhibit range performance no better than that of a less sensitive receiver, if the "ether" noise is appreciably higher than the thermal noise. "Ether" noise refers to other interfering "noise" sources, such as FM radio stations, pagers, etc.

A better indicator of achievable receiver range performance is usually given by its Selectivity, often stated as Intermediate Frequency (IF) or Radio Frequency (RF) bandwidth, depending on receiver topology. Selectivity is a measure of the rejection by the receiver of "ether" noise. More selective receivers will almost invariably provide better range. Only when the receiver selectivity is so high that most of the noise on the receiver input is actually thermal will the receiver demonstrate sensitivity-limited performance.

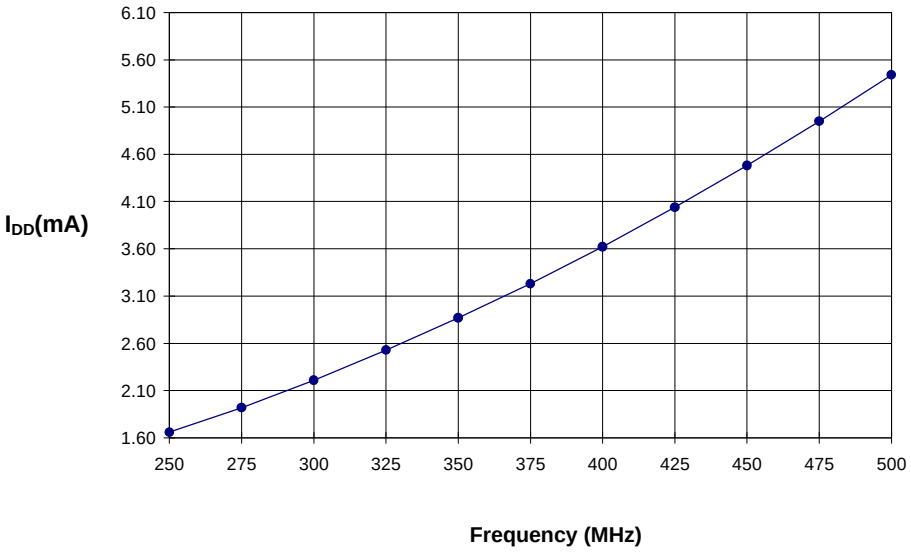
Note 4: Parameter scales linearly with REFOSC frequency ft. For any REFOSC frequency other than 4.90MHz, compute new parameter value as the ratio [(REFOSC FREQ (in MHz) / 4.90] * [Parameter Value @ 4.90MHz]. Example: For REFOSC Freq. ft = 6.00MHz, [Parameter Value @ 6.00MHz] = (6.00 / 4.90) * [Parameter Value @ 4.90MHz].

Note 5: Parameter scales inversely with REFOSC frequency ft. For any REFOSC frequency other than 4.90MHz, compute new parameter value as the ratio [4.90 / (REFOSC FREQ (in MHz)] * [Parameter Value @ 4.90MHz]. Example: For REFOSC Freq. ft = 6.00MHz, [Parameter Value @ 6.00MHz] = (4.90 / 6.00) * [Parameter Value @ 4.90MHz].

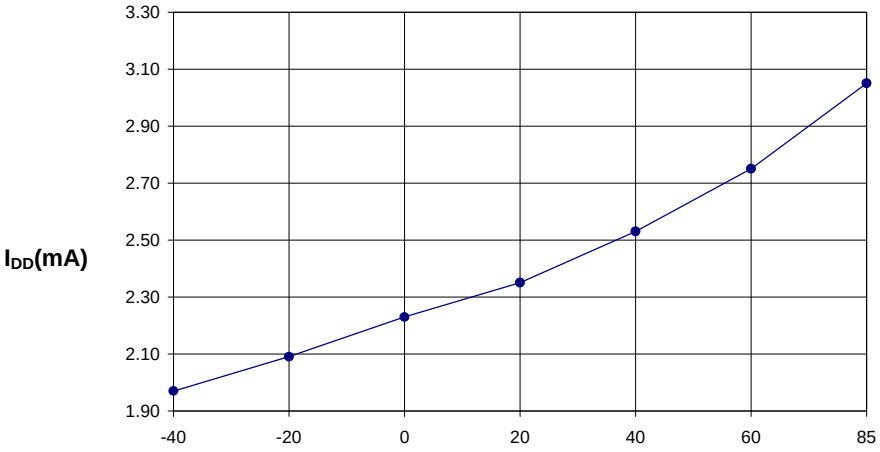
Note 6: Demod filter bandwidths are related in a binary manner, so any of the (lower) nominal filter values may be derived simply by dividing this parameter value by 2, 4, or 8 as desired.

Typical Performance Characteristics

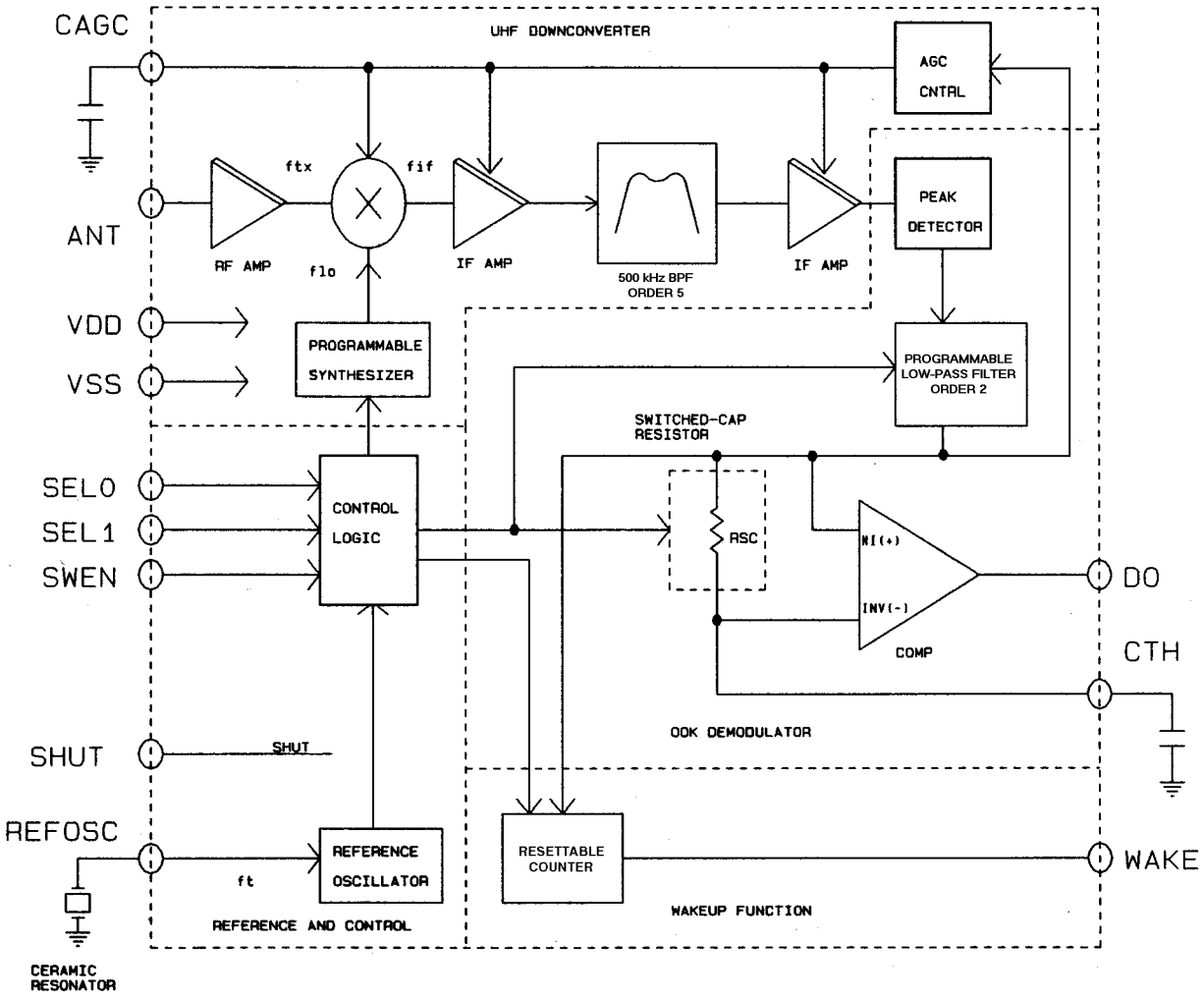
MICRF002 I_{DD} vs Frequency
(Temperature=25°C, V_{DD}=5.0V, SWP Mode, Continuous Operation)



MICRF002 I_{DD} vs Temperature
(Frequency=315MHz, V_{DD}=5.0V, SWP Mode, Continuous Operation)



MICRF002 Block Diagram



Functional Description

Please refer to "MICRF002 Block Diagram". Identified in the block diagram are the four principal functional blocks of the IC, namely (1) UHF Downconverter, (2) OOK Demodulator, (3) Reference and Control, and (4) Wakeup. Also shown in the figure are two capacitors (CTH, CAGC) and one timing component (CR), usually a ceramic resonator. With the exception of a supply decoupling capacitor, these are all the external components needed with the MICRF002 to construct a complete UHF receiver. Four control inputs are shown in the block diagram, SEL0, SEL1, SWEN, and SHUT. Through these logic inputs the user can control the operating mode and selectable features of the IC. These inputs are CMOS compatible, and are pulled-up on the IC.

Input SWEN selects the operating mode of the IC (FIXED mode or SWP mode). When low, the IC is in FIXED mode, and functions as a conventional superheterodyne receiver. When SWEN is high, the IC is in SWP mode. In this mode, while the topology is still superheterodyne, the local oscillator (LO) is deterministically swept over a range of frequencies at rates greater than the data rate. When coupled with a peak-detecting demodulator, this technique effectively increases the RF bandwidth of the MICRF002, so the device can operate in applications where significant Transmitter/Receiver frequency misalignment may exist.

[Note: The swept LO technique does not affect the IF bandwidth, so noise performance is not impacted relative to FIXED mode. In other words, the IF bandwidth is the same (500kHz) whether the device is in FIXED or SWP mode.]

Due to limitations imposed by the LO sweeping process, the upper limit on data rate in SWP mode is approximately 2.5kbps. Data rates beyond 10kbps are possible in FIXED mode however.

Examples of SWP mode operation include applications which utilize low-cost LC-based transmitters, whose transmit frequency may vary up to ± 0.5% over initial tolerance, aging, and temperature. In this (patent-pending) mode, the LO frequency is varied in a prescribed fashion which results in downconversion of all signals in a band approximately 1.5% around the transmit frequency. So the Transmitter may drift up to ± 0.5% without the need to retune the Receiver, and without impacting system performance. Such performance is not achieved with currently available crystal-based superheterodyne receivers, which can operate only with SAW or crystal based transmitters.

[Note: In SWP mode only, a range penalty will occur in installations where there exists a competing signal of sufficient strength in this small frequency band of 1.5% around the transmit frequency. This results from the fact that sweeping the LO indiscriminately "sweeps" all signals within the sweep range down into the IF band. This same penalty also exists with super-regenerative type receivers, as their RF bandwidth is also generally 1.5%. So any application for a super-regenerative receiver is also an application for the MICRF002 in SWP mode.]

For applications where the transmit frequency is accurately set for other reasons (e.g., applications where a SAW transmitter is used for its mechanical stability), the user may choose to configure the MICRF002 as a standard superheterodyne receiver (FIXED mode), mitigating the aforementioned problem of a competing close-in signal. This can be accomplished by tying SWEN to ground. Doing so forces the on-chip LO frequency to a fixed value. In FIXED mode, the ceramic resonator would be replaced with a crystal. Generally, however, the MICRF002 can be operated in SWP mode, using a ceramic resonator , with either LC or CRYSTAL/SAW based transmitters, without any significant range difference.

The inputs SEL0 and SEL1 control the Demodulator filter bandwidth in four binary steps (625Hz—5000Hz in SWP, 1250Hz—10000Hz in FIXED mode), and the user must select the bandwidth appropriate to his needs.

Rolloff response of the IF Filter is 5^{th} order, while the demodulator data filter exhibits a 2^{nd} order response. Multiplication factor between the REFOSC frequency ft and the internal Local Oscillator (LO) is 64.5X for FIXED mode, and 64.25X for SWP mode (i.e., for ft = 6.00MHz in FIXED mode, LO frequency = 6.00MHz * 64.5 = 387MHz).

Slicing Level and the CTH Capacitor

Extraction of the DC value of the demodulated signal for purposes of logic-level data slicing is accomplished by external capacitor CTH and the on-chip switched-cap "resistor" RSC, indicated in the block diagram. The effective resistance of RSC is 118kohms. The value of capacitor CTH is easily calculated, once the slicing level time-constant is chosen. Slicing Level time constant values vary somewhat with decoder type, data pattern, and data rate, but typical values range 5-50msec. Optimization of the CTH value is required to maximize range, as discussed in *"Application Note TBD"*.

During quiet periods (i.e., no signal transmissions) the Data Output (DO pin) transitions randomly based on noise. This may present problems for some decoders. The most common solution is to introduce a small offset ("Squelch") on the CTH pin so that noise does not trigger the internal comparator. Usually 20-30mV is sufficient, and may be introduced by connecting a several-Megohm resistor from the CTH pin to either VSS or VDD, depending on the desired offset polarity. Since the MICRF002 is an AGC'd receiver, noise at the internal comparator input is always the same, set by the AGC. So the squelch offset requirement does not change as the local "ether" noise changes from installation to installation. Note that introducing squelch will reduce range modestly, so only introduce an amount sufficient to "quiet" the output.

AGC Function and the CAGC Capacitor

The signal path has automatic gain control (AGC) to increase input dynamic range. An external capacitor, CAGC, must be connected to the CAGC pin of the device. The *ratio* of decay-to-attack time-constant is fixed at 10:1 (i.e., the attack time constant is 1/10th the decay time constant), and this ratio cannot be changed by the user. However, the attack time constant is selectable by the user through the value of capacitor CAGC.

[By adding resistance from the CAGC pin to VDDBB or VSSBB in parallel with the CAGC capacitor, the *ratio* of decay-to-attack time-constant may be varied, although the value of such adjustments must be studied on a per-application basis. Generally the design value of 10:1 is adequate for the vast majority of applications.] See *"Application Note TBD"*.

To maximize system range, it is important to keep the AGC control voltage ripple low, preferably under 10mVpp once the control voltage has attained its quiescent value. For this reason capacitor values ≥ 0.47uF are recommended.

The AGC control voltage is carefully managed on-chip to allow duty-cycle operation of the MICRF002 in excess of 100:1. When the device is placed into SHUT mode (i.e., SHUT pin pulled high), the AGC capacitor is "floated", to retain the voltage. When operation is resumed, only the voltage droop on the capacitor associated with leakage must be replenished. Thus a relatively low-leakage capacitor is recommended for duty cycle operation. The actual tolerable leakage will be application dependent. Clearly, leakage performance is less critical when the device off-time is low (milliseconds), and more critical when the off-time is high (seconds).

To further enhance Duty-cycle operation of the IC, the AGC push and pull currents are increased for a fixed time immediately after the device is taken out of Shutdown mode (i.e., turned-on). This compensates for AGC capacitor voltage "droop" while the IC is in Shutdown, reduces the time to reacquire the correct AGC voltage, and thus extends maximum achievable duty ratios. Push/Pull currents are increased by 45X their nominal values. The fixed time period is based on the REFOSC frequency ft, 10.9msec for ft = 6.00MHz, and varies inversely as ft varies.

Reference Oscillator (REFOSC) and External Timing Element

All timing and tuning operations on the MICRF002 are derived from the REFOSC function. This function is a single-pin Colpitts-type oscillator. The user may handle this pin in one of three possible ways:

(1) connect a ceramic resonator, or
(2) connect a crystal, or
(3) drive this pin with an external timing signal.

The third approach is attractive for further lowering system cost if an accurate reference signal exists elsewhere in the system (e.g., a reference clock from a crystal or ceramic resonator-based microprocessor). An externally applied signal should be AC-coupled, and resistively-divided down (or otherwise limited) to approximately 0.5Vpp. The specific reference frequency required is related to the system transmit frequency, and to the operating mode of the device as set by the SWEN control pin. See *"Application Note TBD"* for a discussion of frequency selection and accuracy requirements.

Wakeup Function

The Wakeup function is made available for the purposes of further reducing power consumption of the overall wireless system. WAKEB is an output logic signal, which goes active when the IC detects a constant tone "header" in the demodulated output signal. Sense of the signal is active-low. This output may be used to "wakeup" other external circuits, like a data decoder or microprocessor, only at times when there is a reasonable expectation of an incoming RF signal. The Wakeup function is unavailable when the IC is in SHUT mode.

The Wakeup function is composed of a resettable counter, based on an internal 25kHz clock (based on a 6.4MHz reference frequency). To utilize this function, a constant tone in excess of about 4msec must be placed at the start of each data code word, or a single 4msec tone at the start of the data pattern (clearly the former is preferred to improve communication reliability). When this constant tone is detected, without interruption, for 128 clock cycles of 25kHz, WAKEB will transition low, and stay low until data begins. This particular approach is utilized over others (1) since constant tones in excess of 4msec are very rare, leading to few false-positive indications, and (2) this technique does not require the introduction of a signal path offset, which impacts achievable range.

[Note: For designers who wish to use the Wakeup function while "squelching" the output, a positive squelching offset voltage must be used. This simply requires the squelch resistor be taken to a voltage more *positive* than the quiescent voltage on pin CTH, so that the data output is low in absence of a transmission.]

Shutdown Function

The Shutdown function is controlled by the logic state of SHUT. When SHUT is high, the device goes into low-power standby mode, consuming less than 1μA. This pin is pulled high internally, and so must be pulled low to engage the device.

MICRF002 Frequency and Capacitor Selection

Selection of the REFOSC frequency ft, Slicing Level (CTH) capacitor, and AGC capacitor are briefly summarized in this section. Please see Application Note TBD for complete details.

1. Selecting REFOSC Frequency ft (FIXED Mode)

As with any superheterodyne receiver, the difference between the (internal) Local Oscillator (LO) frequency flo and the incoming Transmit frequency ftx must ideally equal the IF Center frequency. Equation (1) may be used to compute the appropriate flo for a given ftx:

$$flo = ftx \pm 1.064 * (ftx / 390) \quad (1)$$

where ftx and flo are in MHz. Note that two values of flo exist for any given ftx, distinguished as "high-side mixing" and "low-side mixing", and there is generally no preference of one over the other.

After choosing one of the two acceptable values of flo, use equation (2) to compute the REFOSC frequency ft:

$$ft = flo / 64.5. \quad (2)$$

Here ft is in MHz. Connect a crystal of frequency ft to the REFOSC pin of the MICRF002. 4 decimal-place accuracy on the frequency is generally adequate. The following table identifies ft for some common Transmit frequencies when the MICRF002 is operated in FIXED mode.

Transmit Freq. ftx (MHz)	REFOSC Freq. ft (MHz)
315	4.8970
418	6.4983
433.92	6.7458

2. Selecting REFOSC Frequency ft (SWP Mode)

Selection of REFOSC frequency ft in SWP mode is much simpler than in FIXED mode, due to the LO sweeping process. Further, accuracy requirements of the frequency reference component are significantly relaxed.

In SWP mode, ft is given by equation (3):

$$ft = ftx / 64.25. \quad (3)$$

Connect a ceramic resonator of frequency ft to the REFOSC pin of the MICRF002. 2-decimal place accuracy is generally adequate. (A crystal may also be used if desired, but may be necessary to reduce the Rx frequency ambiguity if the Tx frequency ambiguity is excessive. See Application Note TBD for further details.)

3. Selecting Capacitor CTH

First step in the process is selection of a Data Slicing Level timeconstant. This selection is strongly dependent on system issues, like system decode response time and data code structure (e.g., existence of data preamble, etc.). This issue is too broad to discuss here, and the interested reader should consult the Application Note 22.

Source impedance of the CTH pin is given by equation (4), where ft is in MHz:

$$Rsc = 118k\Omega * (4.90 / ft). \quad (4)$$

Assuming that a Slicing Level Timeconstant TC has been established, capacitor CTH may be computed using equation (5):

$$CTH = TC / Rsc. \quad (5)$$

4. Selecting CAGC Capacitor in Continuous Mode

Selection of CAGC is dictated by minimizing the ripple on the AGC control voltage, by using a sufficiently large capacitor. It is Micrel's experience that CAGC should be in the vicinity of 0.47µF to 4.7µF. Large capacitor values should be carefully considered, as this determines the time required for the AGC control voltage to settle from a completely discharged condition. AGC settling time from a completely discharged (0-volt) state is given approximately by equation (6):

$$\Delta T = (1.333 * CAGC) - 0.44 \quad (6)$$

where CAGC is in microfarads, and ΔT is in seconds.

5. Selecting CAGC Capacitor in Duty-Cycle Mode

Generally, droop of the AGC control voltage during shutdown should be replenished as quickly as possible after the IC is "turned-on". Recall from the section **"AGC Function and the CAGC Capacitor"** that for about 10msec after the IC is turned-on, the AGC push-pull currents are increased to 45X their normal values. So consideration should be given to selecting a value for CAGC and a shutdown time period such that the droop can be replenished within this 10msec period.

Polarity of the droop is unknown, meaning the AGC voltage could droop up or down. Worst-case from a recovery standpoint is downward droop, since the AGC pullup current is $1/10^{th}$ magnitude of the pulldown current. The downward droop is replenished according to the well-known equation (7):

$$I / CAGC = \Delta V / \Delta T \quad (7)$$

where I = AGC Pullup current for initial 10msec (67.5µA), CAGC is the AGC capacitor value, ΔT = Droop recovery time (<10msec), and ΔV is the droop voltage.

For example, if user desires ΔT = 10msec, and chooses a 4.7µF CAGC, then the allowable droop is about 144mV. Using the same equation with 200nA worst case pin leakage and assuming 1uA of capacitor leakage in the same direction, the maximum allowable ΔT (Shutdown time) is about 0.56 seconds, for droop recovery in 10msec.

I/O Pin Interface Circuitry

Interface circuitry for the various I/O pins of the MICRF002 is shown in Figures 1 through 6. Specific information regarding each of these circuits is discussed in the following sub-paragraphs. Not shown are ESD protection diodes which are applied to all input and output pins.

1. ANT Pin

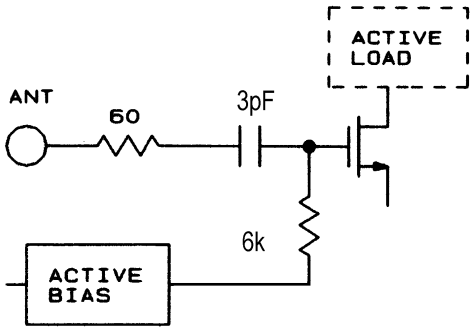


Figure 1 ANT Pin

The ANT pin is internally AC-coupled via a 3pF capacitor, to an RF N-channel MOSFET, as shown in Figure 1. Impedance on this pin to VSS is quite high at low frequencies, and decreases as frequency increases. In the UHF frequency range, the device input can be modeled as 6.3kΩ in parallel with 2pF (pin capacitance) shunt to VSSRF.

2. CTH Pin

Figure 2 illustrates the CTH pin interface circuit. CTH pin is driven from a P-channel MOSFET source-follower biased with approximately 10µA of bias current. Transmission gates TG1 and TG2 isolate the 6.9pF capacitor. Internal control signals PHI1/PHI2 are related in a manner such that the impedance across the transmission gates looks like a "resistance" of approximately 100kΩ. The DC potential on the CTH pin is approximately 1.6V

3. CAGC Pin

Figure 3 illustrates the CAGC pin interface circuit. The AGC control voltage is developed as an integrated current into a capacitor CAGC. The attack current is nominally 15µA, while the decay current is a 1/10th scaling of this, nominally 1.5µA, so the attack/decay timeconstant ratio is fixed at 10:1. Signal gain of the RF/IF strip inside the IC diminishes as the voltage on CAGC decreases. Further discussion on setting the attack time constant is found in *"Application Note TBD*. Modification of the attack/decay ratio is possible by adding resistance from CAGC pin either to VDDBB or VSSBB, as desired.

Both the Push and Pull current sources are disabled during SHUT, which holds the voltage across CAGC, and improves recovery time in duty-cycled applications. To further improve duty cycle recovery, both Push and Pull currents are increased by 45X for approximately 10msec after release of SHUT. This allows rapid recovery of any voltage droop on CAGC while in SHUT.

4. DO and WAKEB Output Pins

The output stage for the signals DO and WAKEB is shown in Figure 4. The output is a 10µA push-10µA pull, switched current stage. Such an output stage is capable of driving CMOS-type loads. An external buffer-driver is recommended for driving high capacitance loads.

5. REFOSC Pin

The REFOSC input circuit is shown in Figure 5. Input impedance is quite high (200kΩ). This is a Colpitts oscillator, with internal 30pF capacitors. This input is intended to work with standard ceramic resonators, connected from this pin to VSSBB, although a crystal may be used instead, where greater frequency accuracy is required. The resonators should not contain integral capacitors, since these capacitors are contained inside the IC. Externally applied signals should be AC-coupled, amplitude limited to approximately 0.5Vpp. The nominal DC bias voltage on this pin is 1.4V.

6. Control Inputs (SEL0, SEL1, SWEN, SHUT)

Control input circuitry is shown in Figures 6a and 6b. The standard input is a logic inverter constructed with minimum geometry MOSFETs (Q2, Q3). P-channel MOSFET Q1 is a large channel length device which functions essentially as a "weak" pullup to VDDBB. Typical pullup current is 5µA, leading to an impedance to the VDDBB supply of typically 1MΩ.

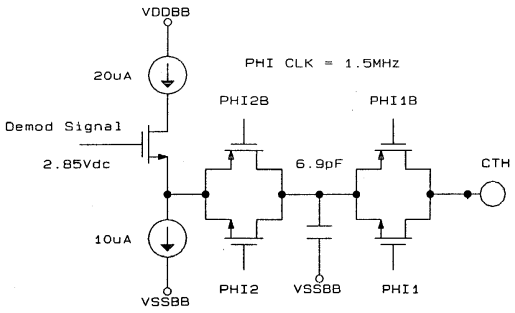


Figure 2 CTH Pin

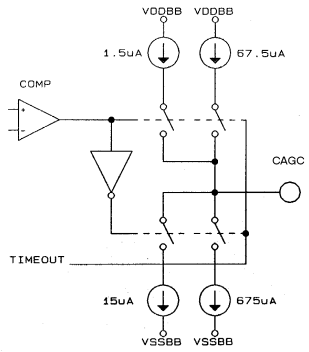


Figure 3 CAGC Pin

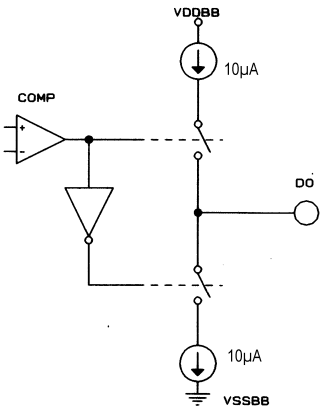


Figure 4 DO and WAKEB Pins

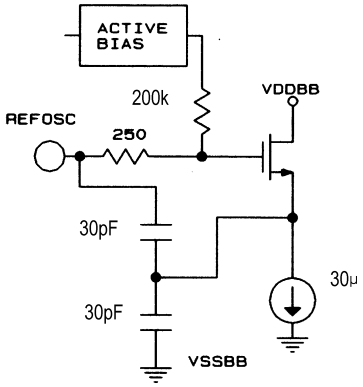


Figure 5 REFOSC Pin

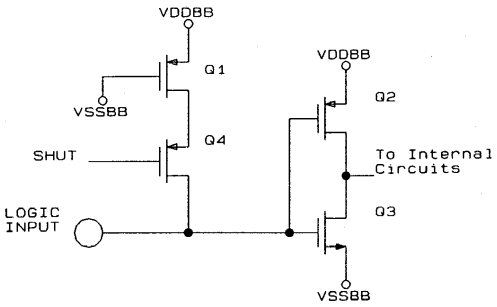


Figure 6a SEL0, SEL1, SWEN

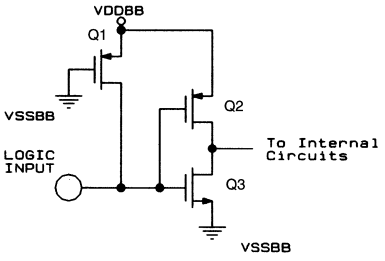


Figure 6b SHUT

Typical Application

Figure 7 below illustrates a typical application for the MICRF002 UHF Receiver IC. Operation in this example is at 385.5MHz, and may be customized by selection of the appropriate reference frequency (CR1), and adjustment of the antenna length. The value of C4 would also change, if the optional input filter is used. Changes from the 1kbps data rate may require a change in the value of R1. The Bill of Materials is shown in the accompanying chart.

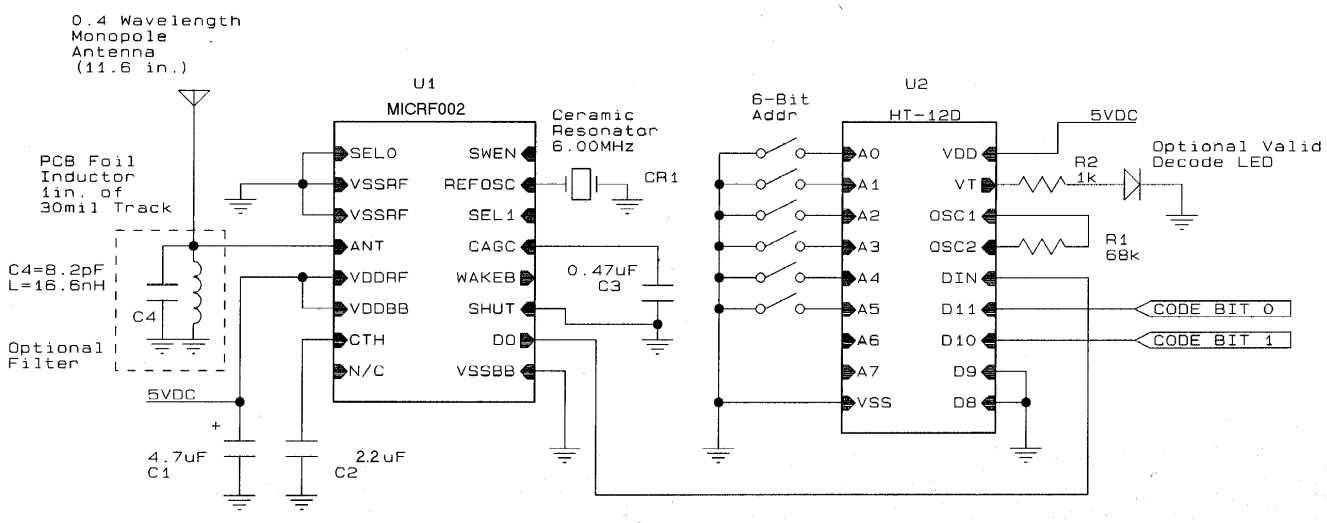


Figure 7

385.5MHz, 1kbps OOK Receiver/Decoder
SWP Mode, Continuous Operation
6-Bit Address Decode/2 OP Codes

Bill of Materials

Item	Part Number	Manufacturer	Description
U1	MICRF002	Micrel	UHF Receiver
U2	HT-12D	Holtek	Logic decoder
CR1	CSA6.00MG	Murata	6.00MHz Cer. Res.
D1	SSF-LX100LID	Lumex	Red LED
R1		Bourns	68k, 1/4W ,5%
R2		Bourns	1k,1/4W, 5%
C1		Panasonic	4.7µF, Dip Tant. Cap
C3		Panasonic	0.47µF, Dip Tant. Cap
C2		Panasonic	2.2µF, Dip Tant. Cap
C4		Panasonic	8.2pF, COG Cer. Cap

Vendor	Telephone	Fax
Bourns	(909) 781-5500	(909) 781-5273
Holtek	(408) 894-9046	(408) 894-0838
Lumex	(800) 278-5666	(847) 359-8904
Murata	(800) 241-6574	(770) 436-3030
Panasonic	(201) 348-7000	(201) 348-8164

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