**NOTES:**

## 1.0 DEVICE OVERVIEW

The MCP2122 is a stand-alone IrDA standard encoder/decoder device that is pinout-compatible with the Agilent® HSDL-7000 encoder/decoder.

The MCP2122 has two interfaces: the host UART interface and the IR interface (see Figure 1-1). The host UART interfaces to the UART of the Host Controller. The Host Controller is the device in the embedded system that transmits and receives the data. The IR interface connects to an infrared (IR) optical transceiver circuit that converts electrical pulses into IR light (encode) and converts IR light into electrical pulses (decode). This IR optical transceiver circuit could be either a standard infrared optical transceiver (such as a Vishay® TFDU 4300) or it could be implemented with discrete components. For additional information, please refer to AN243, “Fundamentals of the Infrared Physical Layer” (DS00243).

When the Host Controller transmits the UART format data, the MCP2122 receives this UART data and encodes (modulates) it bit by bit. This encoded data is then output as electrical pulses to the IR transceiver. The IR transceiver will then convert these electrical pulses to IR light pulses.

The IR transceiver also receives IR light pulses (data), which are outputted as electrical pulses. The MCP2122 decodes (demodulates) these electrical pulses, with the data then being transmitted by the MCP2122 UART. This modulation/demodulation method is performed in accordance with the IrDA standard.

Table 1-1 shows an overview of some of the device features. Figure 1-1 shows a typical application block diagram. Table 1-2 shows the pin definitions of the MCP2122 during normal operation.

**TABLE 1-1: MCP2122 FEATURES OVERVIEW**

| Features | MCP2122 |
|---|---|
| Serial Communications: | UART, IR |
| Baud Rate Selection: | 16XCLK |
| Low-power Mode: | Yes |
| Packages: | 8-pin PDIP<br>8-pin SOIC |

Infrared Technology Features:

- Universal standard for connecting portable computing devices
- Effortless implementation
- Economical alternative to other connectivity solutions
- Reliable, high-speed connection
- Safe to use in any environment; can even be used during air travel
- Eliminates the hassle of cables
- Allows PCs and non-PCs to communicate with each other
- Enhances mobility by allowing users to easily connect

### 1.1 Applications

Some applications where an IR interface (**MCP2122**) could be used include:

- Data-Logging/Data Exchange
- System Setup
- System Diagnostic Read Out
- Manufacturing Configuration
- Host Controller Firmware Updates
- System Control

**FIGURE 1-1: SYSTEM BLOCK DIAGRAM**

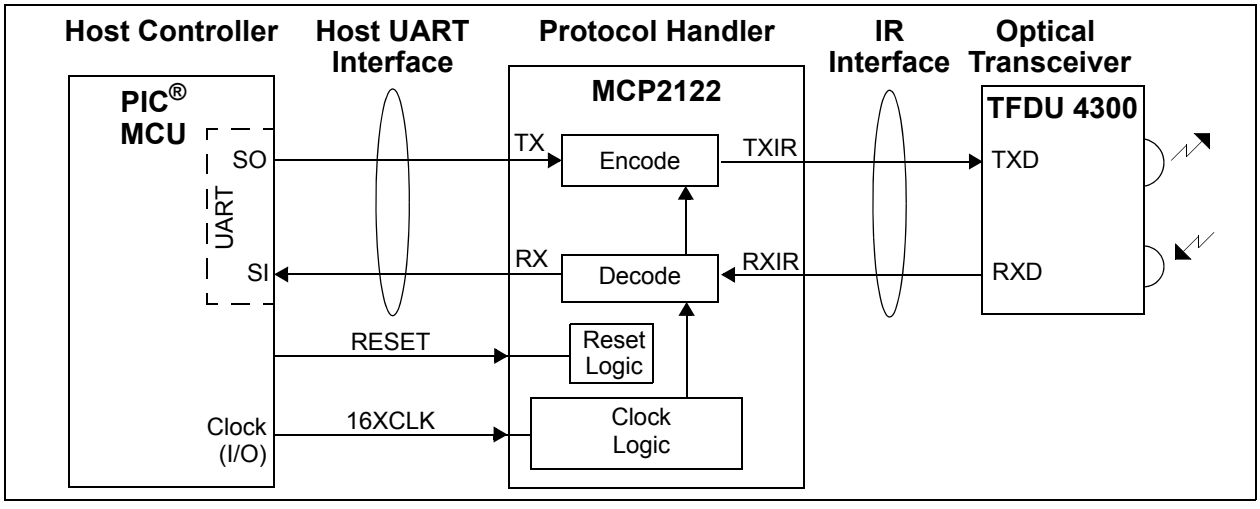


**TABLE 1-2: PIN DESCRIPTION**

| Pin Name | Pin Number | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|
| | PDIP | SOIC | | | |
| 16XCLK | 1 | 1 | I | ST | 16x external clock source input |
| TX | 2 | 2 | I | ST | Asynchronous receive from Host Controller UART |
| RX | 3 | 3 | O | — | Asynchronous transmit to Host Controller UART |
| VSS | 4 | 4 | — | P | Ground reference for logic and I/O pins |
| RESET | 5 | 5 | I | ST | Resets the Device<br>H = Normal Operation<br>L = Device in Reset |
| RXIR | 6 | 6 | I | ST | Asynchronous receive from infrared transceiver |
| TXIR | 7 | 7 | O | — | Asynchronous transmit to infrared transceiver |
| VDD | 8 | 8 | — | P | Positive supply for logic and I/O pins |

**Legend:** ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
O = Output

## 2.0 DEVICE OPERATION

The MCP2122 is a low-cost infrared encoder/decoder. The baud rate is the same for the host UART and IR interfaces and is determined by the frequency of the 16XCLK signal, with a maximum baud rate of 115.2 Kbaud.

The MCP2122 is made up of these functional modules:

- Clock Driver (16XCLK)
- Reset
- IR Encoder/Decoder
  - IrDA Standard Encoder
  - IrDA Standard Decoder

The **16XCLK** circuit allows a clock input to provide the device clock.

The **Reset** circuit supports an external reset signal.

The **IR Encoder** logic takes a data bit and converts it to the IrDA standard signal according to the IrDA standard Physical Layer specification, while the **IR Decoder** logic takes the IrDA standard signal and converts it to 8-bit data bytes.

### 2.1 Power-up

As the device is powered up, there will be a voltage range in which the device will not operate properly. The device should be reset once it has entered the normal operating range (from an out-of-voltage condition). The RESET pin may then be forced high.

Other device operating parameters (such as frequency, temperature, etc.) must also be within their operating ranges when the device exits reset. Otherwise, the device may not function as desired.

### 2.2 Device Reset

The MCP2122 is forced into the known state (RESET) when the $\overline{\text{RESET}}$ pin is in the low state. Once the $\overline{\text{RESET}}$ pin is brought to a high state, the device begins normal operation (if the device operating parameters are met). Table 2-1 shows the states of the output pins while the device is in reset (RESET = Low). Table 2-2 shows the state of the output pins once the device exits reset, RESET = L→H (device in Normal Operation mode).

The MCP2122 has a $\overline{\text{RESET}}$ noise filter in the $\overline{\text{RESET}}$ input signal path. The filter will detect and ignore small pulses.

Using the RESET pin to enter a low-power state is discussed in **Section 2.9 "Minimizing Power"**.

**TABLE 2-1: DEFAULT OUTPUT PIN STATES IN DEVICE RESET**

| Input Pin | | Output Pin State | | Comments |
|---|---|---|---|---|
| Name | State | RX | TXIR | |
| RESET | L | H | L | Device in Reset mode |

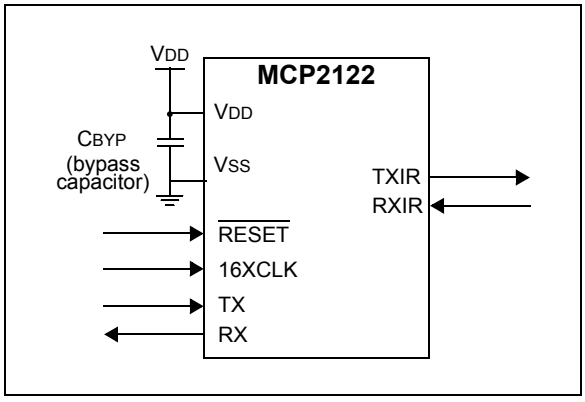
**TABLE 2-2: DEFAULT OUTPUT PIN STATES AFTER DEVICE RESET (RESET = L→H)**

| Input Pin | | Output Pin State | | Comments |
|---|---|---|---|---|
| Name | State | RX | TXIR | |
| TX | L | — | L→H →L | After 7 - 8 16XCLK pulses, the TXIR pin will pulse high. |
| | H | — | L | |
| RXIR | L | H→L | — | After 4 16XCLK pulses, RX = L. |
| | H | H | — | |

### 2.3 Decoupling

It is highly recommended that the MCP2122 have a decoupling capacitor (CBYP). A 0.01 µF capacitor is recommended as a starting value, but an evaluation of the best value for your circuit/layout should be performed. Place this decoupling capacitor (CBYP) as close to the MCP2122 as possible (see Figure 2-1).

**FIGURE 2-1: DEVICE DECOUPLING**



### 2.3.1 BROWN-OUTS

Some applications may subject the MCP2122 to a brown-out condition. Good design practice requires that when a system is in brown-out, the system should be in reset to ensure that the system is in a known state when the system exits the brown-out. This brown-out circuitry is external to the MCP2122.

#### 2.3.1.1 External Brown-Out Reset Circuits

Figure 2-2 shows a circuit for external brown-out protection using the TCM809 device.

Figure 2-3 and Figure 2-4 illustrate two examples of external circuitry that may be implemented. Each option needs to be evaluated to determine if they satisfy the requirements of the application.

**FIGURE 2-2: EXTERNAL BROWN-OUT PROTECTION USING THE TCM809**

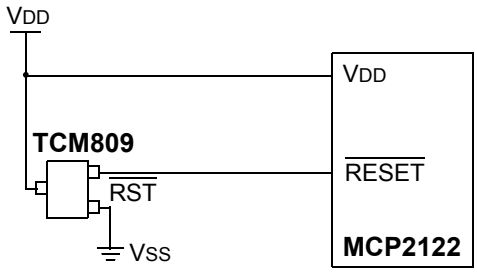
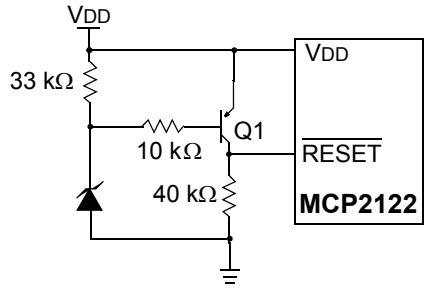


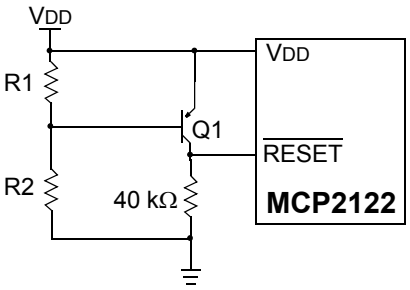

**FIGURE 2-3: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1**




**Note 1:** Resistors should be adjusted for the characteristics of the transistor.

**2:** This circuit will activate reset when VDD goes below (Vz + 0.7V), where Vz = Zener voltage.

**FIGURE 2-4: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2**




**Note 1:** This circuit is less expensive, but less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \bullet \frac{R1}{R1 + R2} = 0.7V$$

**2:** Resistors should be adjusted for the characteristics of the transistor.

## 2.4 16XCLK (Bit Clock)

The MCP2122 requires an external clock source to operate. The 16XCLK pin is the device clock input (see Figure 2-5) and is independent of the host UART interface or the IR interface. The 16XCLK determines all timing during device operation. It is the edge of the 16XCLK pin that causes activity to occur.

The 16XCLK signal can also be referred to as a bit clock (BITCLK). There are 16 BITCLKs for each bit time. The BITCLKs are used for the generation of the Start bit, the eight data bits and the Stop bit.

When the embedded system could be receiving IR communication, the MCP2122 is required to have the 16XCLK signal clocking at the expected frequency, with minimal variation in that frequency. Between data bytes (Stop bit to Start bit), the 16XCLK frequency can be changed. This may occur in systems where the Host Controller is implementing one of the IrDA standard application layer protocols (such as IrObex).

When the embedded system does not want to receive IR communications, the 16XCLK clock can be disabled (static). This will reduce the power consumption of the system.

Figure 2-6 shows the relationship of the 16XCLK signal to the RXIR input, which then determines the RX output signal. Figure 2-7 shows the relationship of the 16XCLK signal to the TX input, which then determines the TXIR output signal. For device timing information, refer to **Section 4.0 "Electrical Characteristics"**.

**FIGURE 2-5: DEVICE CLOCK SOURCE**

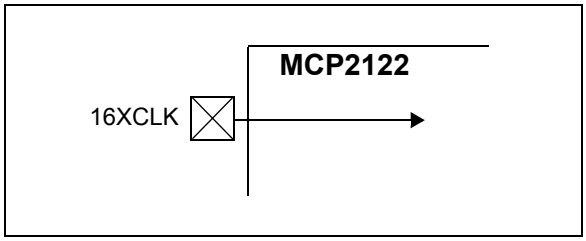



**FIGURE 2-6: 16XCLK AND RX/RXIR**

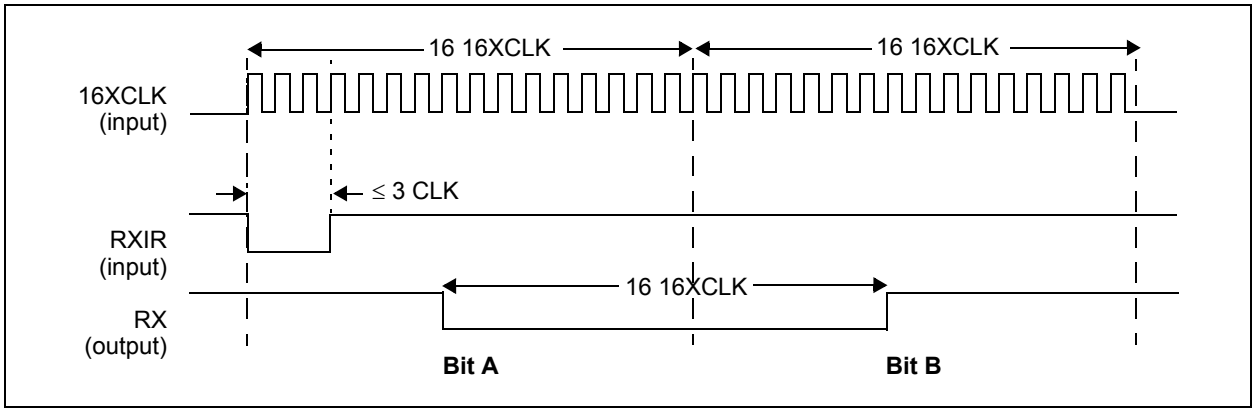
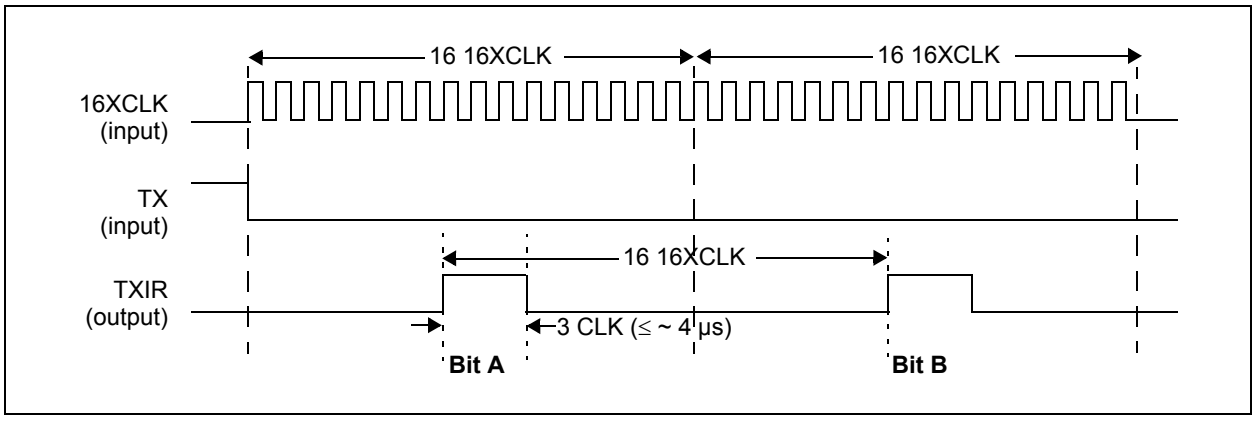



**FIGURE 2-7: 16XCLK AND TX/TXIR**



### 2.4.1 BAUD RATE

The baud rate for the MCP2122 is determined by the frequency of the 16XCLK signal. Equation 2-1 demonstrates how to calculate the 16XCLK frequency based on the desired baud rate. Table 2-3 shows some common baud rates and the corresponding 16XCLK frequency.

**EQUATION 2-1: 16XCLK FREQUENCY**

$$F_{16XCLK} = 16 \bullet (Desired\ Baud\ Rate)$$

**TABLE 2-3: COMMON BAUD RATE/ 16XCLK FREQUENCY**

| Baud Rate | 16XCLK Frequency ($F_{16XCLK}$) | Comment |
|---|---|---|
| 9600 | 153,600 | |
| 19,200 | 307,200 | |
| 38,400 | 614,400 | |
| 57,600 | 921,600 | |
| 115,200 | 1,843,200 | |

## 2.5 Encoder/Decoder

The IR encoder/decoder is made up of two major components. They are:

- IR Decoder
- IR Encoder

The encoder receives UART data (bit by bit) and outputs a data bit in the IrDA standard bit format. Figure 2-8 shows a functional block diagram of the encoder.

The decoder receives IrDA standard data (bit by bit) and outputs data in UART data bit format. Figure 2-8 shows a functional block diagram of the decoder.

The encoder/decoder has two interfaces. They are:

- Host UART interface
- IR interface

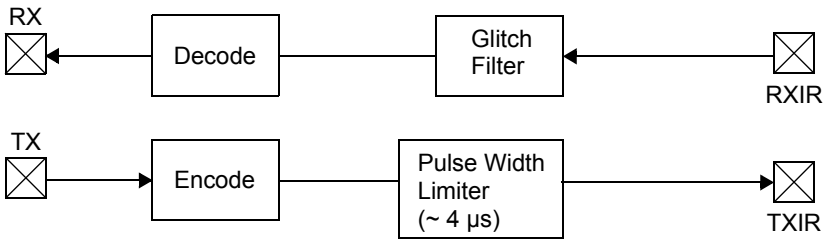
### 2.5.1 ENCODING (MODULATION)

Each bit time is comprised of 16 bit clocks. If the value to be transmitted (as determined by the TX pin) is a logic-low, the TXIR pin will output a low level for 7-bit clock cycles, a logic-high level for 3-bit clock (with a maximum high-time of about 4 µs) cycles, with the remaining time (6-bit clock cycles or more) being low. If the value to transmit is a logic-high, the TXIR pin will output a low level for the entire 16 bit clock cycle.

### 2.5.2 DECODING (DEMODULATION)

Each bit time is comprised of 16 bit clocks. If the value to be received is a logic-low, the RXIR pin will be a low level for the first 3-bit clock cycle (or a minimum of 1.6 µs), with the remaining time (13-bit clock cycles) being high. If the value to be received is a logic-high, the RXIR pin will be a high level for the entire 16-bit clock cycle. The level on the RX pin will be in the appropriate state for an entire 16-bit clock cycle.

**FIGURE 2-8: MCP2122 RECEIVE DETECT TO ENCODER/DECODER BLOCK DIAGRAM**




The following table shows the state on the $\overline{\text{RESET}}$ pin and how this effects the operation of the TXIR pin.

| $\overline{\text{RESET}}$ State | Comment |
|---|---|
| VIH | TXIR output encoded value of TX pin |
| VIL | TXIR is forced low |

### 2.5.3 ENCODING AND SCREEN CAPTURES

Table 2-4 shows the TXIR pin high-time at different common baud rates. The internal TXIR pulse-width high-time limiter is a feature that minimizes the system current consumption at lower baud rates. The IrDA standard specification requires that optical receiver circuitry detect pulses as narrow as 1.41 µs (1.63 µs is the typical time at 115200 baud). Therefore, the time that the TXIR pin is high after this valid detection is additional current that is driven by the emitter LED. The MCP2122 will force the TXIR pin low once the pulse-width limiter has timed out. Figure 2-9 shows the MCP2122 16XCLK, TX and TXIR waveforms at 115200 baud for a single TX low bit. In this case, the TXIR is high for three 16XCLK pulses. In Figure 2-10, the MCP2122 is at 9600 baud for a single TX low bit. In this case, the TXIR is high for 3.55 µs (determined by pulse-width limiter circuit).

**TABLE 2-4: TXIR HIGH PULSE WIDTH**

| Baud Rate | TXIR Pulse Width | | |
|---|---|---|---|
| | 3xT16XCLK Circuit | Pulse-width Limiter (2) Circuit | Actual Pulse Width |
| 9600 | 19.53 µs (1) | 4.00 µs | 4.00 µs (3) |
| 19200 | 9.77 µs (1) | 4.00 µs | 4.00 µs (3) |
| 38400 | 4.88 µs (1) | 4.00 µs | 4.00 µs (3) |
| 57600 | 3.26 µs | 4.00 µs | 3.26 µs |
| 115200 | 1.63 µs | 4.00 µs | 1.63 µs |

**Note 1:** The pulse-width limiter on the TXIR pin saves system current for this baud rate.

**2:** This TXIR pulse width time is a design target and is not tested. Actual times may be greater than, or less than, this value.

**3:** This time (determined by the pulse-width limiter circuit) is device dependent.

**FIGURE 2-9: MCP2122 AT 115200 BAUD WAVEFORM**

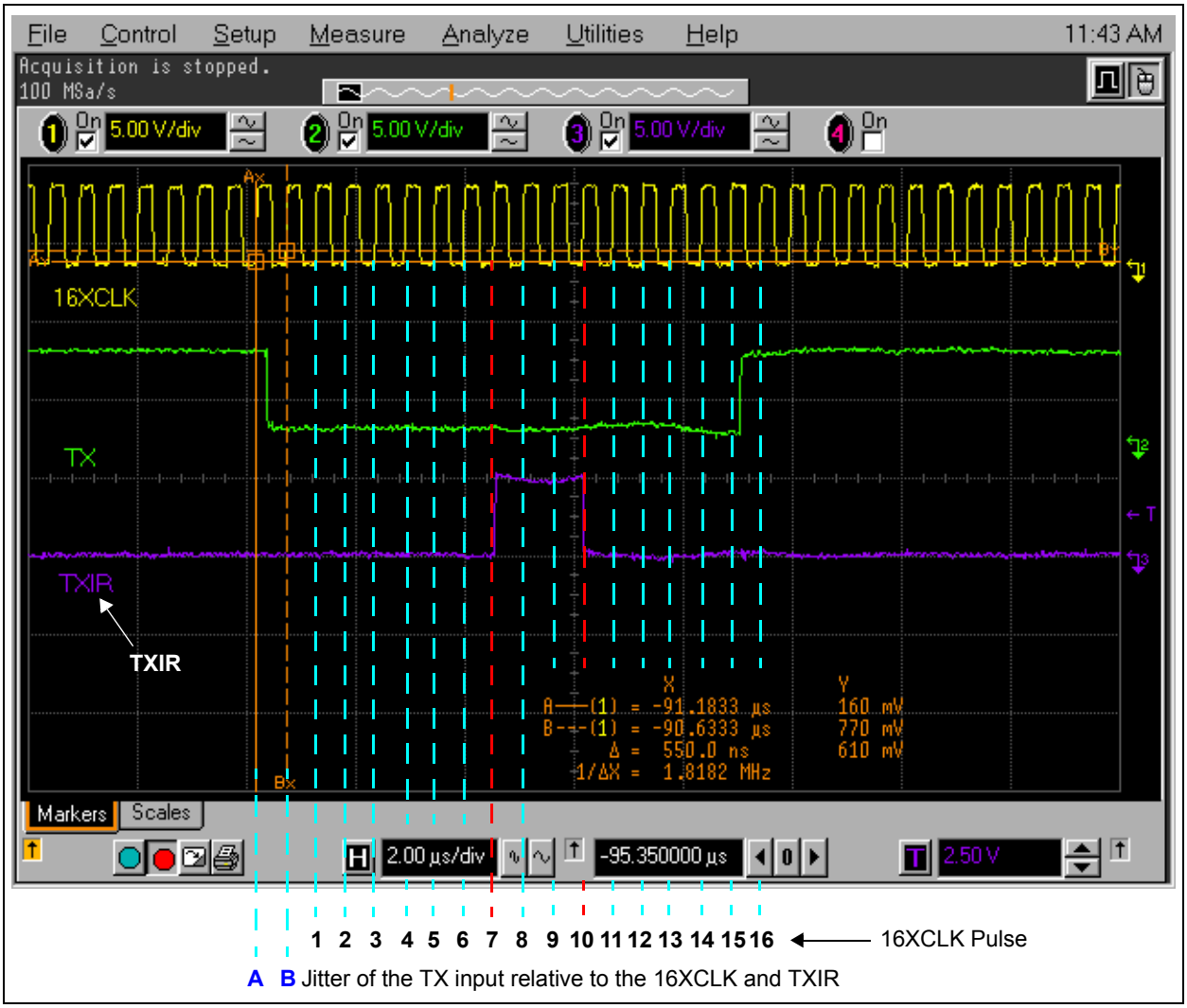
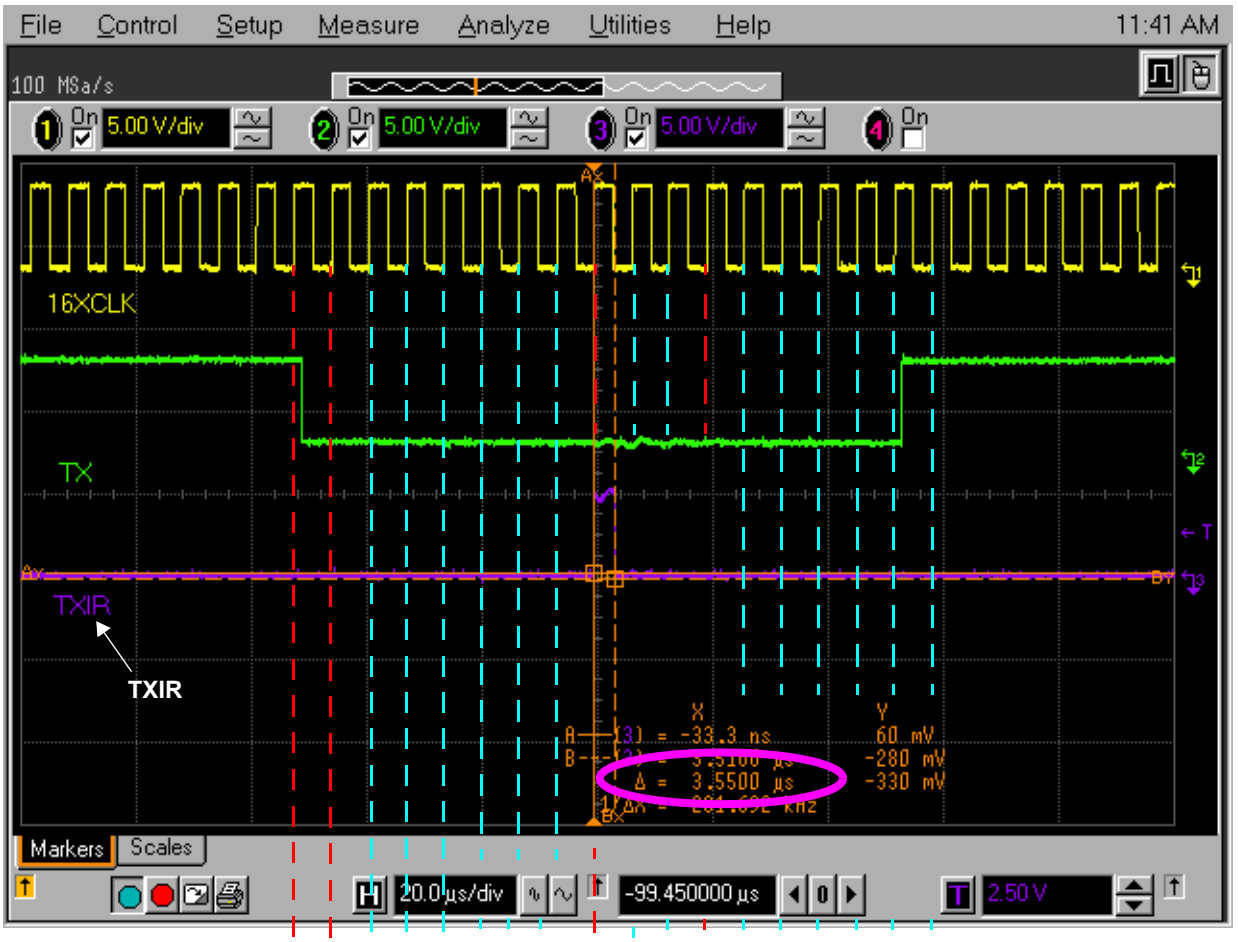


**FIGURE 2-10: MCP2122 AT 9600 BAUD WAVEFORM**



## 2.6 Host UART Interface

The UART interface is used to communicate with the Host Controller. Though a UART is capable of a full-duplex interface, the direct coupling to the IR encoder/decoder allows only half-duplex operation (since the IR side is either receiving or transmitting and not both at the same time). This means that the system can't transmit and receive at the same time.

### 2.6.1 TRANSMITTING

When the controller sends serial data to the MCP2122, the baud rates are required to match.

There will be some jitter on the detection of the high-to-low edge of the start bit. This jitter will affect the placement of the encoded start bit. All subsequent bits will be 16 BITCLK times later.

While RXIR is receiving data (low pulse), the TXIR pin is disabled from transmitting.

### 2.6.2 RECEIVING

When the controller receives serial data from the MCP2122, the baud rates are required to match.

There will be some jitter on the detection of the high-to-low edge of the Start bit. This jitter will affect the placement of the decoded Start bit. All subsequent bits will be 16 BITCLK times later.

The TXIR pin is disabled when data is being received (low pulse) on the RXIR pin.

## 2.7 IR Interface

The IR interface is used to communicate with the optical receiver circuitry. The IR interface is either transmitting data or receiving data (half-duplex).

## 2.8 Encoding/Decoding Jitter and Offset

Figure 2-11 shows the jitter on the RXIR and TX pins, along with the offset on the RX pin and the TXIR pin.

Jitter is the possible variation of the desired edge. Figure 2-9 and Figure 2-10 show the jitter of the TX pin (range is indicated by red dashed lines).

Offset is the propagation delay of the input signal (RXIR or TX) to the output signal (RX or TXIR). Figure 2-9 and Figure 2-10 show the offset of the TXIR pin from the 16XCLK signal that starts the bit time.

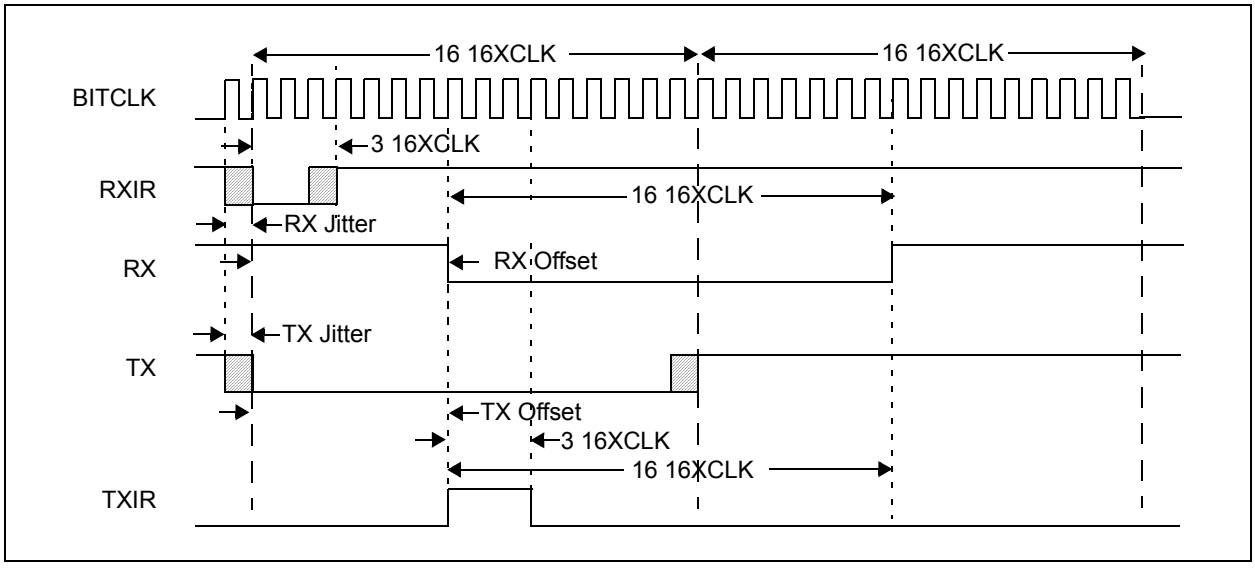
## 2.9 Minimizing Power

The device can be placed in a low-power mode by forcing the RESET pin low. This disables the internal state machine. To ensure that the lowest power consumption is obtained, ensure that the 16XCLK pin is not active and that the other input pins (TX and RXIR) are at a logic-high or logic-low level.

### 2.9.1 RETURNING TO OPERATION

When returning to normal operation, the RESET pin must be forced high and the 16XCLK signal should be operating. Time should be given to ensure that the 16XCLK is stabilized at the desired frequency before data is allowed to be transmitted or received.

**FIGURE 2-11: EFFECTS OF JITTER AND OFFSET**



**NOTES:**

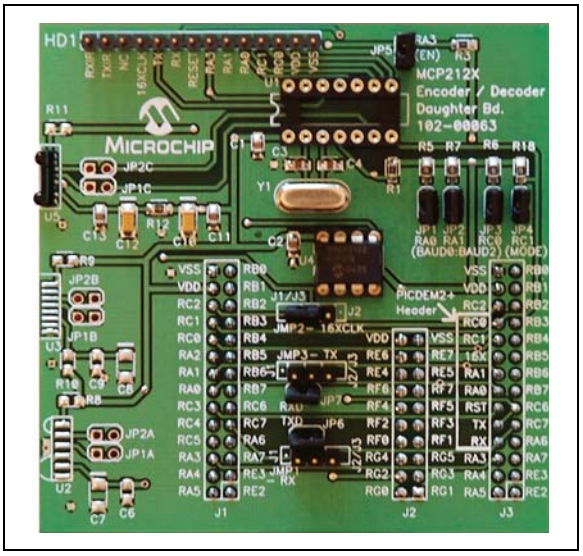
## 3.0 DEVELOPMENT TOOLS

The MCP212X Developer's Daughter Board is used to evaluate and demonstrate the MCP2122 or the MCP2120 IrDA® Standard Encoder/Decoder devices.

A header allows the MCP212X Developer's Daughter Board to be jumpered easily into systems for development purposes.

The MCP212X Developer's Daughter Board is designed to interface to several of the "new" low cost PIC® Demo Boards. These include the PICDEM HPC Explorer Demo board, the PICDEM FS USB Demo board, and the PICDEM LCD Demo board.

When the MCP212X Developer's Daughter Board is used in conjunction with the PICDEM HPC Explorer Demo board, the MCP212x can be connected to either of the PIC18F8772's two UARTs or the RX and TX signals can be "crossed" so the MCP212x device can communicate directly out the PICDEM HPC Explorer Demo Board's UART (DB-9).




### Features:

- 8-pin socket for installation of MCP2122 (installed) and 14-pin socket for installation of MCP2120
- Three Optical Transceiver circuits (1 installed)
- Headers to interface to low cost PICDEM Demo Boards, including:
  - • PICDEM™ HPC Explorer Demo Board
  - • PICDEM™ LCD Demo Board
  - • PICDEM™ FS USB Demo Board
  - • PICDEM™ 2 Plus Demo Board
- Headers to easily connect to the user's embedded system
- Jumpers to select routing of MCP212X signals to the PICDEM™ Demo Board Headers
- Jumpers to configure the operating mode of the board

**NOTES:**

## 4.0 ELECTRICAL CHARACTERISTICS

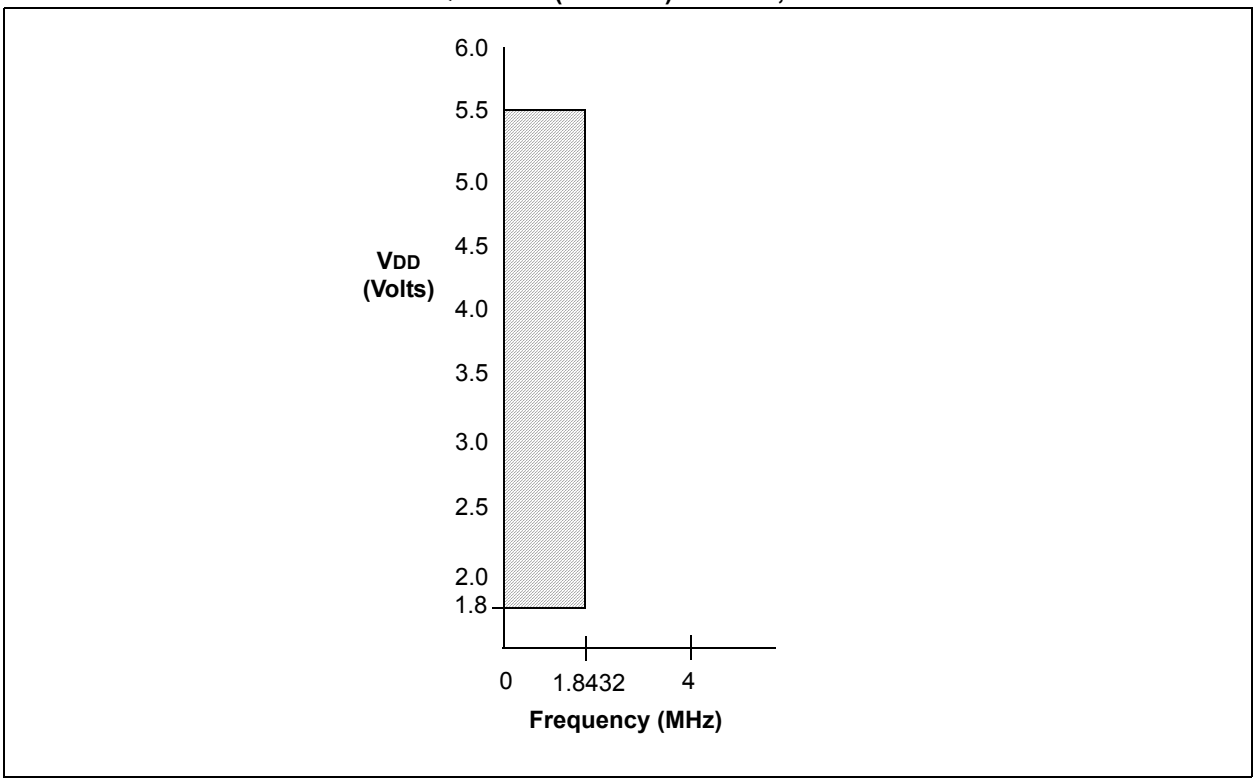
### Absolute Maximum Ratings†

Ambient Temperature under bias ..... –40°C to +125°C
Storage Temperature ..... –65°C to +150°C
Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... –0.3V to +6.5V
Voltage on $\overline{RESET}$ with respect to $V_{SS}$ ..... –0.3V to +14V
Voltage on all other pins with respect to $V_{SS}$ ..... –0.3V to ($V_{DD}$ + 0.3V)
Total Power Dissipation (1) ..... 800 mW
Max. Current out of $V_{SS}$ pin ..... 500 mA
Max. Current into $V_{DD}$ pin ..... 500 mA
Input Clamp Current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{DD}$) ..... ±20 mA
Output Clamp Current, $I_{OK}$ ($V_0$ < 0 or $V_0$ > $V_{DD}$) ..... ±20 mA
Max. Output Current sunk by any Output pin ..... 25 mA
Max. Output Current sourced by any Output pin ..... 25 mA

**Note 1:** Power Dissipation is calculated as follows:
$P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

**†NOTICE:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**FIGURE 4-1: VOLTAGE-FREQUENCY (16XCLK) GRAPH, -40°C ≤ TA ≤ +125°C**



## 4.1 DC Characteristics

| DC Characteristics | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature: –40°C ≤ TA ≤ +125°C (Extended) | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Sym** | **Characteristic** | **Min** | **Typ (1)** | **Max** | **Units** | **Conditions** |
| D001 | VDD | Supply Voltage | 1.8 | — | 5.5 | V | See Figure 4-1 |
| D010 | IDD | Supply Current (2) | — | 0.1 | 1 | mA | FOSC = 1.8432 MHz, VDD = 5.5V (TX = H, RXIR = H) |
| | | | | | | | Transmitter (TX = L, RXIR = H) |
| | | | — | — | 300 | µA | FOSC = 1.8432 MHz, VDD = 1.8V (4) |
| | | | — | — | 1 | mA | FOSC = 1.8432 MHz, VDD = 5.5V |
| | | | | | | | Receiver (RXIR = L, TX = H) |
| | | | — | — | 500 | µA | FOSC = 1.8432 MHz, VDD = 1.8V (4) |
| | | | — | — | 2 | mA | FOSC = 1.8432 MHz, VDD = 5.5V |
| D020 | IPD | Device Disabled Current (3) | — | — | 2 | µA | VDD = 1.8V (4) |
| | | | — | — | 4 | µA | VDD = 5.5V |

**Note 1:** Data in the Typical (“Typ”) column is based on characterization results at +25°C. This data is for design guidance only and is not tested.

**2:** The supply current is mainly a function of the operating voltage and frequency. Pin loading, pin rate and temperature have an impact on the current consumption.

a)The test conditions for all IDD measurements are:
16XCLK = external square wave, from rail-to-rail; TX = VSS, RXIR = VSS, $\overline{\text{RESET}}$ = VDD.

**3:** The device disable current is mainly a function of the operating voltage. Temperature also has an impact on the current consumption. When the device is disabled (RESET = VSS). The test conditions for all IDD measurements are:
16XCLK = external square wave, from rail-to-rail; TX = VSS, RXIR = VDD, $\overline{\text{RESET}}$ = VSS; The output pins are driving a high or low level into infinite impedance.

**4:** These parameters (shaded) are characterized but are not tested. These values should be used for design guidance only.

## DC Characteristics (Continued)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating temperature –40°C ≤ TA ≤ +125°C (extended)<br>Operating voltage VDD range as described in DC spec, **Section 4.1 "DC Characteristics"**. | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym** | **Characteristic** | **Min** | **Typ (1)** | **Max** | **Units** | **Conditions** |
| | VIL | **Input Low-Voltage** | | | | | |
| | | Input pins | | | | | |
| D031 | | TX, RXIR | Vss | — | 0.2 VDD | V | |
| D032 | | $\overline{\text{RESET}}$ | Vss | — | 0.2 VDD | V | |
| D033 | | 16XCLK | Vss | — | 0.2 VDD | V | |
| | VIH | **Input High-Voltage** | | | | | |
| | | Input pins | | — | | | |
| D041 | | TX, RXIR | 0.8 VDD | — | VDD | V | |
| D042 | | $\overline{\text{RESET}}$ | 0.8 VDD | — | VDD | V | |
| D043 | | 16XCLK | 0.8 VDD | — | VDD | V | |
| | IIL | **Input Leakage Current (2, 3)** | | | | | |
| D060A | | TX and 16XCLK | — | — | ±1 | µA | VSS ≤ VPIN ≤ VDD, Pin at high-impedance |
| D061 | | $\overline{\text{RESET}}$ | — | — | ±1 | µA | VSS ≤ VPIN ≤ VDD |
| D060B | IIH | RXIR | — | — | ±1 | µA | VDD = 5.5V, VRXIR = VDD |

**Note 1:** Data in the Typical ("Typ") column is based on characterization results at +25°C. This data is for design guidance only and is not tested.

**2:** The leakage current on the $\overline{\text{RESET}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**3:** Negative current is defined as coming out of the pin.

## DC Characteristics (Continued)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating temperature: –40°C ≤ TA ≤ +125°C (Extended)<br>Operating voltage VDD range as described in DC spec, **Section 4.1 "DC Characteristics"**. | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym** | **Characteristic** | **Min** | **Typ (1)** | **Max** | **Units** | **Conditions** |
| | VOL | **Output Low-Voltage** | | | | | |
| D080B | | RX | — | — | 0.6 | V | IOL = 2 mA, VDD = 1.8V |
| D081 | | TXIR | — | — | 0.6 | V | IOL = 2 mA, VDD = 1.8V |
| | VOH | **Output High-Voltage** | | | | | |
| D090B | | RX (2) | VDD – 0.7 | — | — | V | IOH = -0.8 mA, VDD = 1.8V |
| D091 | | TXIR (2) | VDD – 0.7 | — | — | V | IOH = -0.8 mA, VDD = 1.8V |
| | | **Capacitive Loading Specs on Output Pins** | | | | | |
| D101A | COUT | All Output pins | — | — | 50 | pF | |
| D101B | CIN | All Input pins | — | 7 | — | pF | TA = +25°C, FC = 1.0 MHz |

**Note 1:** Data in the Typical ("Typ") column is based on characterization results at +25°C. This data is for design guidance only and is not tested.

**2:** Negative current is defined as coming out of the pin.

## 4.2 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created following one of the following formats:

### 4.2.1 TIMING CONDITIONS

The temperature and voltages specified in Table 4-2 apply to all timing specifications, unless otherwise noted. Figure 4-2 specifies the load conditions for the timing specifications.

**TABLE 4-1: SYMBOLOGY**

1. TppS2ppS

2. TppS

| | | | |
|---|---|---|---|
| **T** | | | |
| F | Frequency | T | Time |
| E | Error | | |

Lowercase letters (pp) and their meanings:

| | | | |
|---|---|---|---|
| **pp** | | | |
| io | Input or Output pin | xclk | Oscillator |
| rx | Receive | tx | Transmit |
| bitclk | RX/TX BITCLK | RST | Reset |

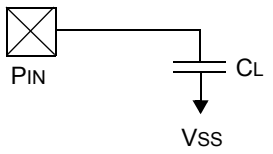
Uppercase letters and their meanings:

| | | | |
|---|---|---|---|
| **S** | | | |
| F | Fall | P | Period |
| H | High | R | Rise |
| I | Invalid (Hi-impedance) | V | Valid |
| L | Low | Z | High-impedance |

**TABLE 4-2: AC TEMPERATURE AND VOLTAGE SPECIFICATIONS**

| | |
|---|---|
| **AC CHARACTERISTICS** | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature: –40°C ≤ TA ≤ +125°C (Extended)<br>Operating voltage VDD range as described in DC spec,<br>**Section 4.1 "DC Characteristics"**. |

**FIGURE 4-2: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS**




CL = 50 pF for all output pins
7 pF (typical) for all input pins

## 4.3 Timing Diagrams and Specifications

**FIGURE 4-3: EXTERNAL CLOCK TIMING**

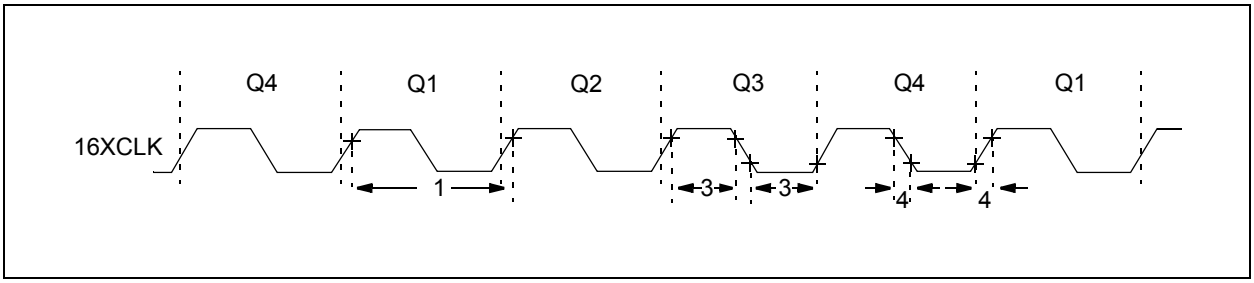



**TABLE 4-3: EXTERNAL CLOCK TIMING REQUIREMENTS**

| AC Characteristics | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature: –40°C ≤ TA ≤ +125°C (Extended)<br>Operating Voltage VDD range is described in<br>**Section 4.1 "DC Characteristics"** | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Sym** | **Characteristic** | **Min** | **Typ(1)** | **Max** | **Units** | **Conditions** |
| 1 | TXCLK | External 16XCLK Period (2, 3) | 542.5 | — | — | ns | |
| 1A | FXCLK | External 16XCLK Frequency (2, 3) | DC | — | 1.8432 | MHz | |
| 1C | EXCLK | Clock Error (4, 5) | — | — | ±2 | % | **Note 5** |
| 3 | TXCLKL, TXCLKH | Clock in (16XCLK) Low or High Time | 50 | — | — | ns | |
| 4 | TXCLKR, TXCLKF | Clock in (16XCLK) Rise or Fall Time (5) | — | — | 7.5 | ns | **Note 5** |

**Note 1:** Data in the Typical ("Typ") column is at 5V, +25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

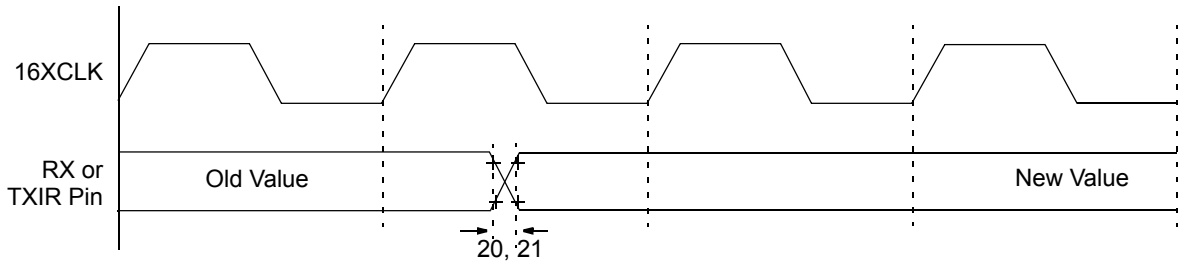
**2:** All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

**3:** A duty cycle of no more than 60/40 (High-Time/Low-Time or Low-Time/High-Time) is recommended for external clock inputs.

**4:** This is the clock error from the desired clock frequency. The total system clock error includes the error from the transmitter and the error of receiver (from the desired clock frequency). If the transmitter is 2% fast from the target frequency, and the receiver is 2% slow from the target frequency, the total error is 4%.

**5:** These parameters (shaded) are characterized but are not tested. These values should be used for design guidance only.

**FIGURE 4-4: I/O WAVEFORM**




**Note:** Refer to Figure 4-2 for load conditions.

**TABLE 4-4: I/O TIMING REQUIREMENTS**

| **AC Characteristics** | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature: –40°C ≤ TA ≤ +125°C (Extended)<br>Operating Voltage VDD range is described in<br>**Section 4.1 "DC Characteristics"** | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Sym** | **Characteristic** | **Min** | **Typ (1)** | **Max** | **Units** | **Conditions** |
| 20A | ToR | RX pin rise time (2, 3) | — | 10 | 25 | ns | VDD ≥ 2.7V **(Note 3)** |
| 20B | | | — | 10 | 60 | ns | VDD = 1.8V **(Note 3)** |
| 20C | | TXIR pin rise time (2, 3) | — | 10 | 25 | ns | VDD ≥ 2.7V **(Note 3)** |
| 20D | | | — | 10 | 60 | ns | VDD = 1.8V **(Note 3)** |
| 21A | ToF | RX pin fall time (2, 3) | — | 10 | 35 | ns | **Note 3** |
| 21C | | TXIR pin fall time (2, 3) | — | 10 | 25 | ns | **Note 3** |

**Note 1:** Data in the Typical ("Typ") column is at 5V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**2:** See Figure 4-2 for loading conditions.

**3:** These parameters (shaded) are characterized but are not tested. These values should be used for design guidance only.

**FIGURE 4-5: $\overline{\text{RESET}}$ AND DEVICE RESET TIMER TIMING**

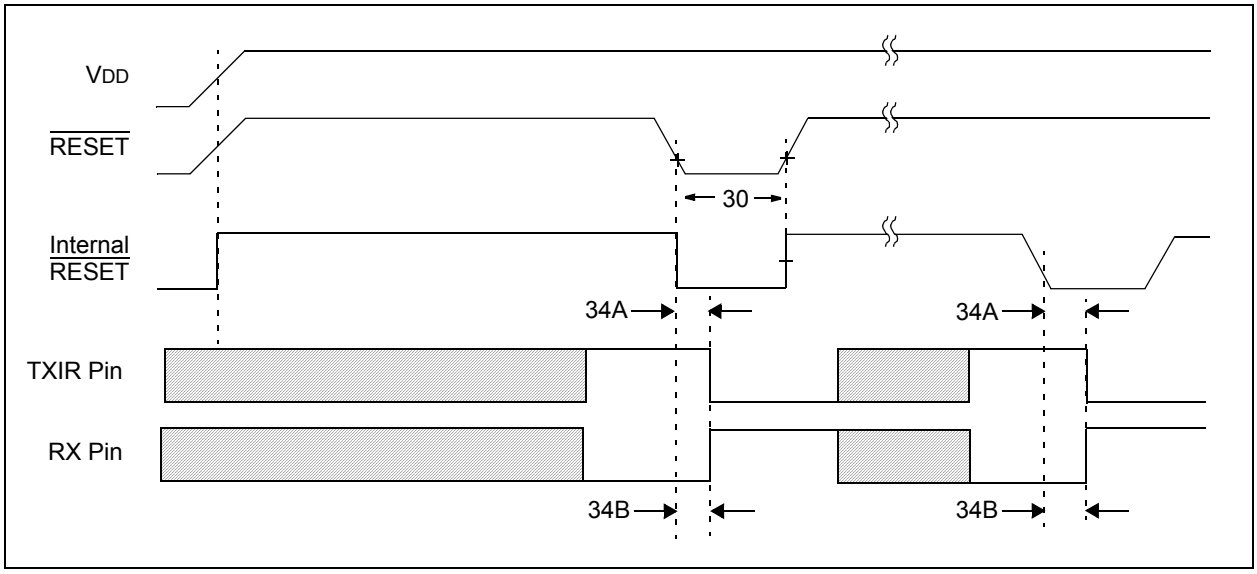



**TABLE 4-5: $\overline{\text{RESET}}$ AND DEVICE RESET TIMER REQUIREMENTS**

| **AC Characteristics** | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature: –40°C ≤ TA ≤ +125°C (Extended)<br>Operating Voltage VDD range is described in<br>**Section 4.1 "DC Characteristics"**. | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Sym** | **Characteristic** | **Min** | **Typ (1)** | **Max** | **Units** | **Conditions** |
| 30 | TRSTL | $\overline{\text{RESET}}$ Pulse Width (low) | 2000 | — | — | ns | VDD = 5.0 V |
| 34A | TOD | Default output state of TXIR pin from $\overline{\text{RESET}}$ Low | — | — | 2 | µs | |
| 34B | TOD | Default output state of RX pins from $\overline{\text{RESET}}$ Low | — | — | 2 | µs | |

**Note 1:** Data in the Typical ("Typ") column is at 5V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**FIGURE 4-6: TX AND TXIR WAVEFORMS**

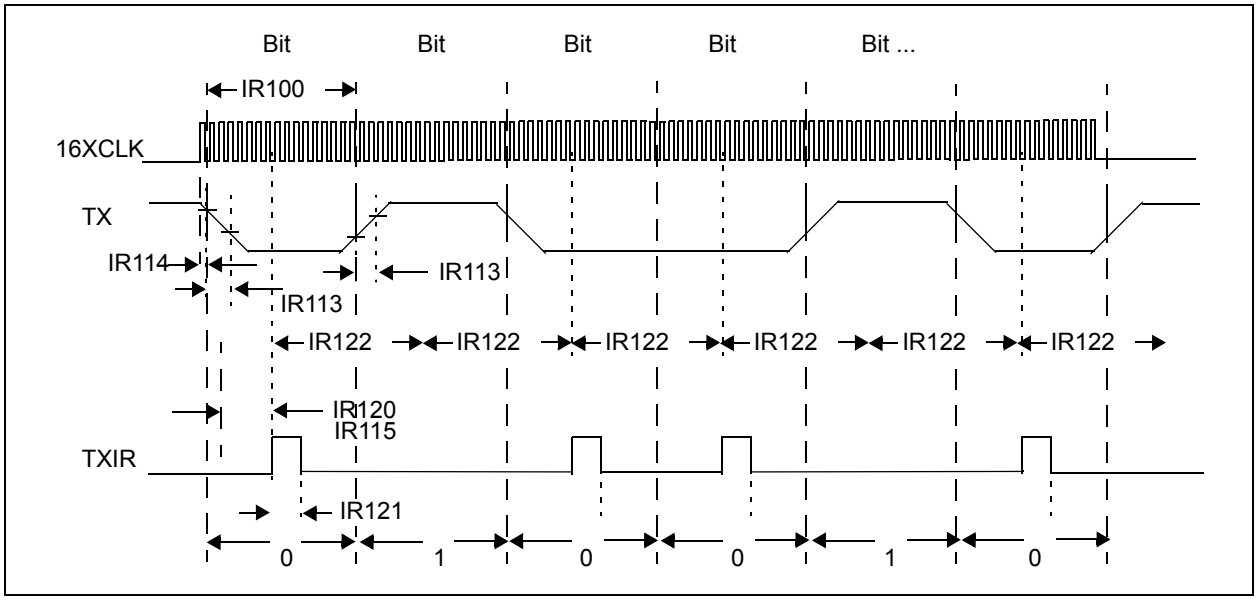



**TABLE 4-6: TX AND TXIR REQUIREMENTS**

| **AC Characteristics** | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature: –40°C ≤ TA ≤ +125°C (Extended)<br>Operating Voltage VDD range is described in<br>**Section 4.1 "DC Characteristics"**. | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Sym** | **Characteristic** | **Min** | **Typ (1)** | **Max** | **Units** | **Conditions** |
| IR100A | TTXBIT | Transmit Baud Rate | — | 16 | — | TXCLK | |
| IR100B | TTXIRBIT | Transmit Baud Rate | 16 | — | 16 | TXCLK | |
| IR102A | ETXBIT | Host UART TX Error | — | — | ± 2 | % | **Note 2**, **3** |
| IR102B | ETXIRBIT | TXIR Error from 16XCLK | — | 0 | — | % | **Note 2**, **4** |
| IR113 | TTXRF | TX pin rise time and fall time | — | — | 25 | ns | **Note 2** |
| IR114 | TTXPDIRJ | 16XCLK to TX jitter | — | — | 1 | TXCLK | **Note 2** |
| IR120 | TTXL2TXIRH | TX falling edge (↓) to TXIR rising edge (↑) **(1)** | 7 | — | 8 | TXCLK | |
| IR121A | TTXIRPW | TXIR pulse width | 3 | — | 3 | TXCLK | At 115200 baud |
| IR121B | | | 1.41 | 3.5 | 5 | µs | At 9600 baud **(Note 5)** |
| IR122 | TTXIRP | TXIR bit period **(1)** | — | 16 | — | TXCLK | |
| IR123 | TTXIRRF | TXIR pin rise time and fall time | — | — | 10 | ns | 50 pF load **(Note 2)** |

**Note 1:** Data in the Typical ("Typ") column is at 5V, +25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

**2:** These parameters (shaded) are characterized but are not tested. These values should be used for design guidance only.

**3:** The TX pin operation may be asynchronous to the 16XCLK pin. This is the error from the desired baud rate for the system.

**4:** The TXIR pin operation is synchronous to the 16XCLK pin. Any error present on the 16XCLK pin (Parameter 1C) will be refelected on the TXIR pin.

**5:** This specification is not tested. This value is from the design target.

**FIGURE 4-7: 16XCLK AND THE TX AND TXIR WAVEFORMS**

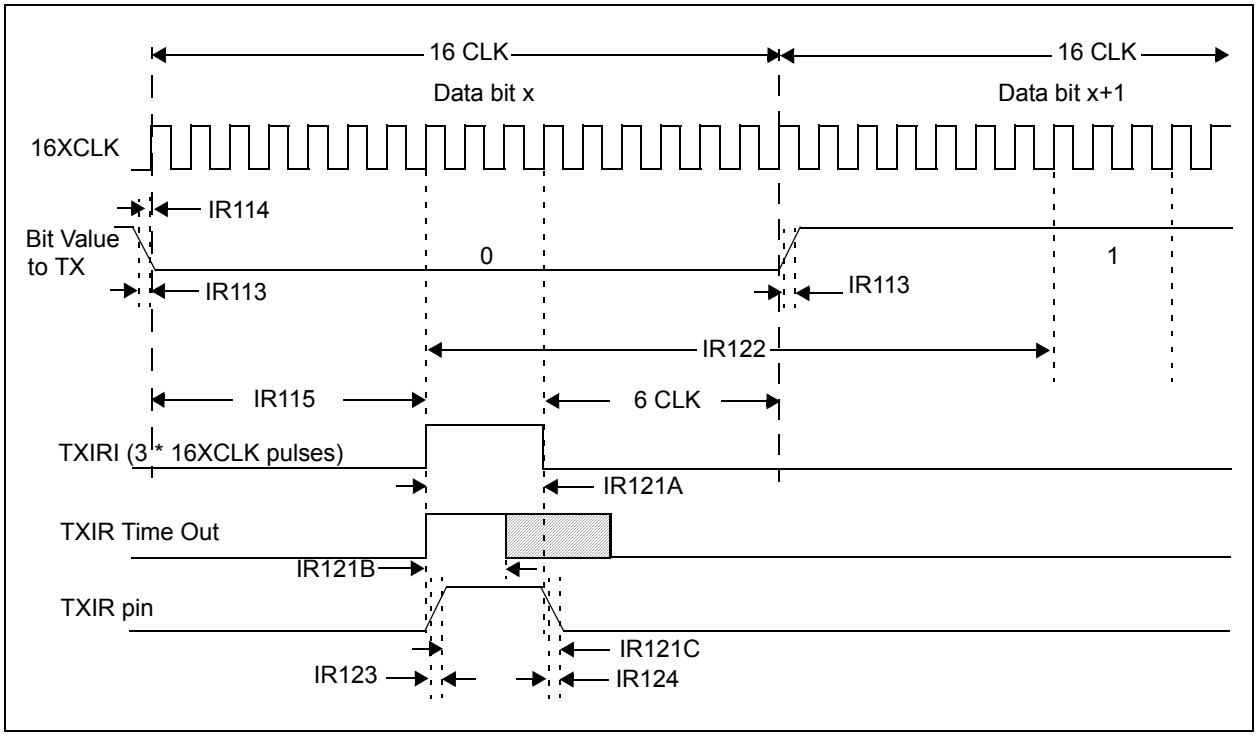



**TABLE 4-7: TX AND TXIR REQUIREMENTS**

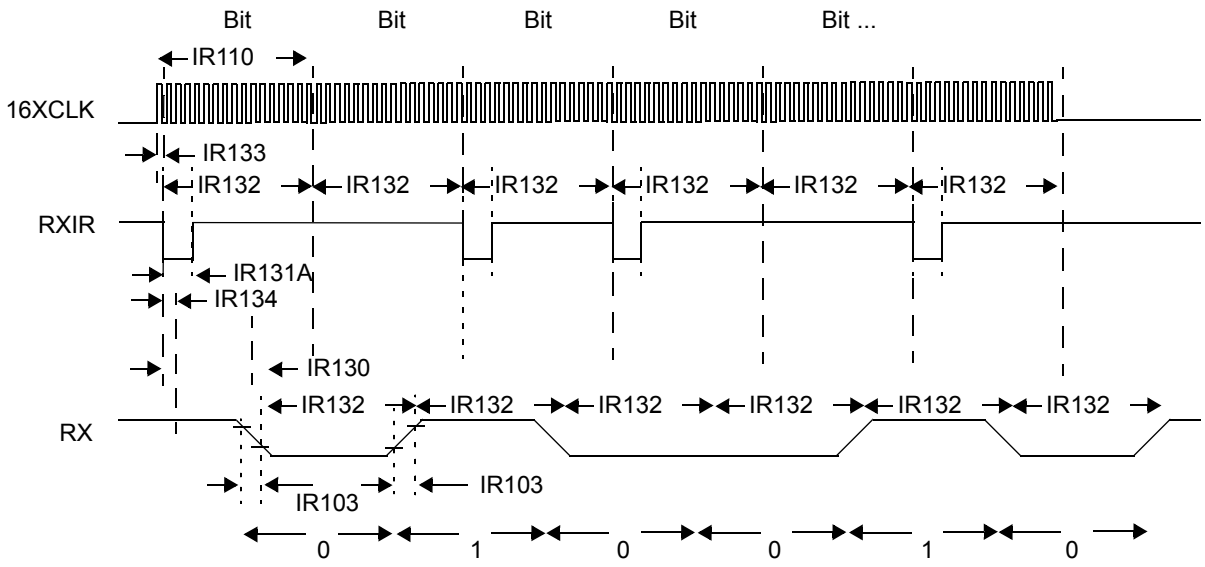
| **AC Characteristics** | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature: –40°C ≤ TA ≤ +125°C (Extended)<br>Operating Voltage VDD range is described in<br>**Section 4.1 "DC Characteristics"**. | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristic** | **Min** | **Typ (1)** | **Max** | **Units** | **Conditions** |
| IR113 | TTXRF | TX pin rise time and fall time | — | — | 25 | ns | **Note 2** |
| IR114 | TTXJ | TX to 16XCLK jitter | — | — | 1 | TXCLK | **Note 2** |
| IR120 | TTXL2TXIRH | TX falling edge (↓) to TXIR rising edge (↑) **(1)** | 7 | — | 8 | TXCLK | |
| | TTXIRPW | TXIR pulse width | Smaller of | | Smaller of | | |
| IR121A | | | 3 | — | 3 | TXCLK | At 115200 baud |
| IR121B | | | 1.41 | 3.5 | 5 | µs | At 9600 baud **(Note 3)** |
| IR122 | TTXIRP | TXIR bit period | — | 16 | — | TXCLK | |
| 20C | TTXIRR | TXIR pin rise time | — | 10 | 25 | ns | VDD ≥ 2.7V **(Note 2)** |
| 20D | | | — | 10 | 60 | ns | VDD = 1.8V **(Note 2)** |
| 21C | TTXIRF | TXIR pin fall time | — | 10 | 25 | ns | **Note 2** |

**Note 1:** Data in the Typical ("Typ") column is at 5V, +25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

**2:** These parameters (shaded) are characterized but are not tested. These values should be used for design guidance only.

**3:** This specification is not tested. This value is from the design target

**FIGURE 4-8: RXIR AND RX WAVEFORMS**




**Note:** Refer to Figure 4-2 for load conditions.

**TABLE 4-8: RXIR REQUIREMENTS**

| **AC Characteristics** | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature: –40°C ≤ TA ≤ +125°C (Extended)<br>Operating Voltage VDD range is described in **Section 4.1 "DC Characteristics"**. | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Sym** | **Characteristic** | **Min** | **Typ (1)** | **Max** | **Units** | **Conditions** |
| IR101A | ERXIRBIT | RXIR Error | — | — | ± 2 | % | **Note 2, 3** |
| IR101B | ERXBIT | Host UART RX Error | — | 0 | — | % | **Note 2, 4** |
| IR103 | TTXRF | RX pin rise time and fall time | — | — | 25 | ns | |
| IR110 | TRXBIT | Receive (RX pin) Bit Rate | 16 | — | 16 | TXCLK | |
| IR130 | TRXIRL2RXH | RXIR Low AND 16XCLK edge (↓ or ↑) to RX falling edge (↓) | — | 4 | — | TXCLK | At 115,200 baud |
| | | | — | 3 | — | TXCLK | At 9600 baud |
| IR131A | TRXIRPW | RXIR pulse width | 1.41 | — | 3 TXCLK | µs | |
| IR132 | TRXIRP | RXIR bit period (1) | — | 16 | — | TXCLK | |
| IR133 | TRXIRJ | 16XCLK to RXIR jitter | — | — | 1 | TXCLK | **Note 2** |
| IR134 | TRXSKW | 16XCLK to RX skew | — | — | 2.5 | µs | |
| IR135 | TRXPDFIL | RXIR Filter | 0.7 | — | 1.4 | µs | **Note 5** |

**Note 1:** Data in the Typical ("Typ") column is at 5V, +25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

**2:** These parameters (shaded) are characterized but are not tested. These values should be used for design guidance only.

**3:** The RXIR pin operation is asynchronous to the 16XCLK pin. This is the error from the desired baud rate for the system.

**4:** The RX pin operation is synchronous to the 16XCLK pin. Any error present on the 16XCLK pin (Parameter 1C) will be refelected on the RX pin.

**5:** The minimum specification ensures that ALL pulses less then this pulse width are rejected, the maximum specification ensures that ALL pulses greater than this pulse width are never rejected, and pulse widths between these may or may not be rejected.

## 5.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

The graphs and tables are not available at this time

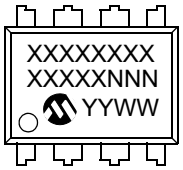
**NOTES:**

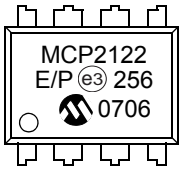
## 6.0 PACKAGING INFORMATION

### 6.1 Package Marking Information

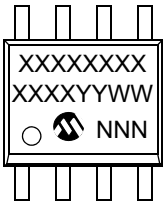
8-Lead PDIP (300 mil)



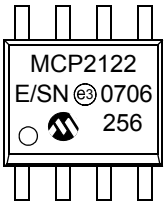

Example:




8-Lead SOIC (150 mil)




Example:

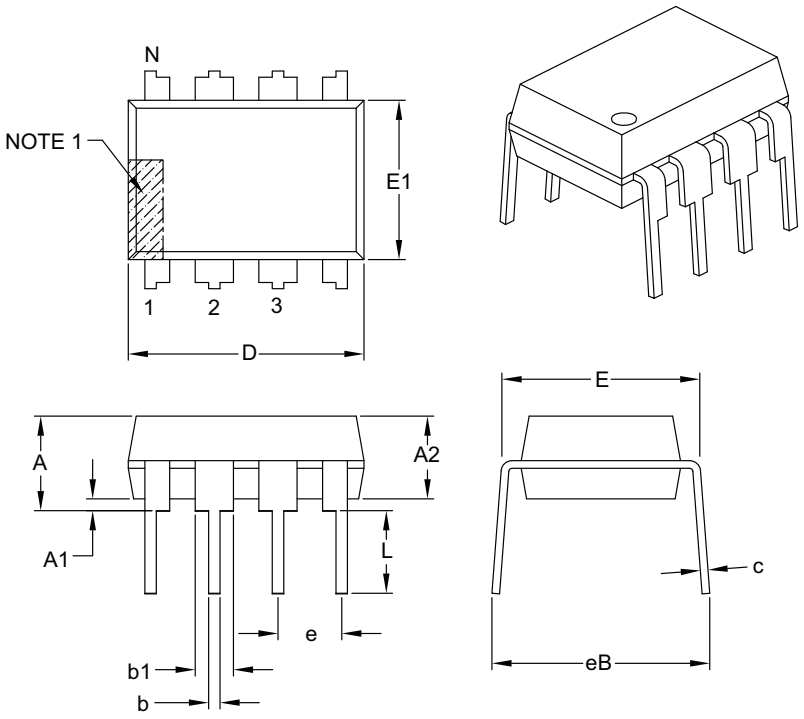



| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

## 8-Lead Plastic Dual In-Line (P or PA) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | .100 BSC | |
| Top to Seating Plane | A | – | – | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 |
| Base to Seating Plane | A1 | .015 | – | – |
| Shoulder to Shoulder Width | E | .290 | .310 | .325 |
| Molded Package Width | E1 | .240 | .250 | .280 |
| Overall Length | D | .348 | .365 | .400 |
| Tip to Seating Plane | L | .115 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .040 | .060 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | – | – | .430 |

**Notes:**

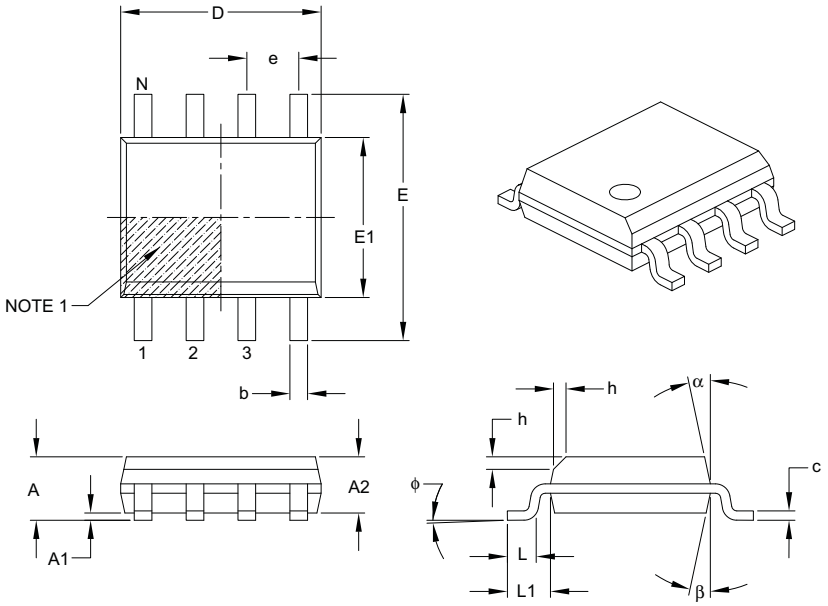
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

## 8-Lead Plastic Small Outline (SN or OA) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | – | – | 1.75 |
| Molded Package Thickness | A2 | 1.25 | – | – |
| Standoff § | A1 | 0.10 | – | 0.25 |
| Overall Width | E | | 6.00 BSC | |
| Molded Package Width | E1 | | 3.90 BSC | |
| Overall Length | D | | 4.90 BSC | |
| Chamfer (optional) | h | 0.25 | – | 0.50 |
| Foot Length | L | 0.40 | – | 1.27 |
| Footprint | L1 | | 1.04 REF | |
| Foot Angle | φ | 0° | – | 8° |
| Lead Thickness | c | 0.17 | – | 0.25 |
| Lead Width | b | 0.31 | – | 0.51 |
| Mold Draft Angle Top | α | 5° | – | 15° |
| Mold Draft Angle Bottom | β | 5° | – | 15° |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

**FIGURE 6-1: EMBOSSED CARRIER DIMENSIONS (12 MM TAPE)**

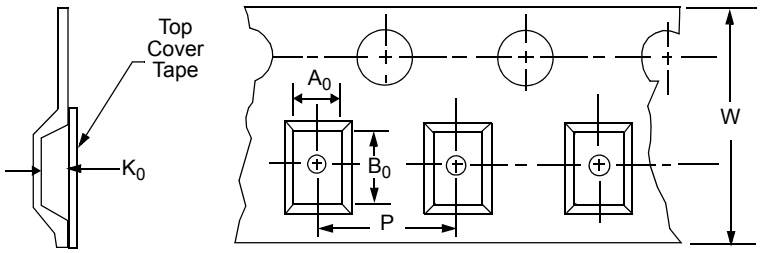
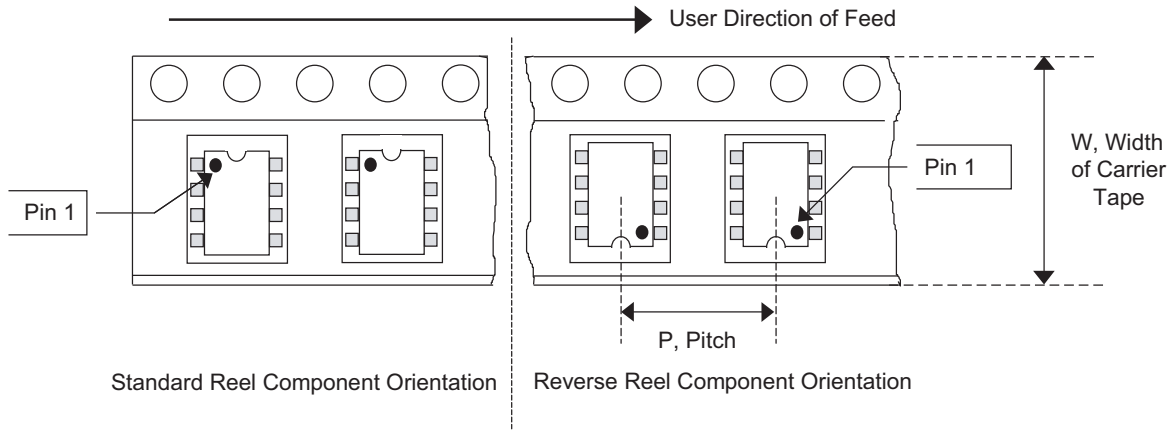



**TABLE 6-1: CARRIER TAPE/CAVITY DIMENSIONS**

| Case Outline | Package Type | Carrier Dimensions | | Cavity Dimensions | | | Output Quantity Units | Reel Diameter in mm |
|---|---|---|---|---|---|---|---|---|
| | | W mm | P mm | A0 mm | B0 mm | K0 mm | | |
| SN | SOIC .150" 8L | 12 | 8 | 6.4 | 5.2 | 2.1 | 3300 | 330 |

**FIGURE 6-2: SOIC DEVICE**



# APPENDIX A: REVISION HISTORY

## Revision C (February 2007)

- Updated Development Tools section
- Update packaging outline drawings
- Updates Product Identification System section.

## Revision B (September 2004)

- Undocumented changes

## Revision A (June 2004)

- Original release of this document

**NOTES:**

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | – | X | /XX |
|---|---|---|---|
| Device | | Temperature Range | Package |

| | | |
|---|---|---|
| Device | MCP2122: | Infrared Encoder/Decoder |
| | MCP2122T: | Infrared Encoder/Decoder, Tape and Reel |
| Temperature Range | E = | -40°C to +125°C |
| Package | P = | Plastic DIP (300 mil, Body), 8-lead |
| | SN = | Plastic SOIC (150 mil, Body), 8-lead |

**Examples:**

a) MCP2122-E/P: Extended Temperature, 8L-PDIP package

b) MCP2122-E/SN: Extended Temperature, 8L-SOIC package

c) MCP2122T-E/SN: Tape and Reel, Extended Temperature, 8L-SOIC package

**NOTES:**

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.



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